National Semiconductor

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ADC121S101/ADC101S101/ADC081S101 1MSPS, 12-/10-/8-Bit A/D Converters in SOT-23 & LLP

General Description

The ADC121S101, ADC101S101, and ADC081S101 are low power, monolithic CMOS 12-, 10- and 8-bit analog-to-digital converters that operate at 1 MSPS. Each device is based on a successive approximation register architecture with internal track-and-hold. The serial interface is compatible with several standards, such as SPI™, QSPI™, MICROWIRE™, and many common DSP serial interfaces.

The ADC121S101/101S101/081S101 uses the supply voltage as a reference. This enables the devices to operate with a full-scale input range of 0 to V_{DD}. The conversion rate is determined from the serial clock (SCLK) speed. These converters offer a shutdown mode, which can be used to trade throughput for power consumption. The ADC121S101/101S101/081S101 are operated with a single supply that can range from +2.7V to +5.25V. Normal power consumption during continuous conversion, using a +3V or +5V supply, is 2 mW or 10 mW, respectively. The power down feature, which is enabled by a chip select ($\overline{CS}$) pin, reduces the power consumption to under 5 µW using a +5V supply. All three converters are available in a 6-lead SOT-23 package, which provides an extremely small footprint for applications where space is a critical consideration. The ADC081S101 is also available in a 6-lead LLP package. These products are designed for operation over the industrial temperature range of −40˚C to +85˚C, with some parameters specified to +125˚C for the ADC121S101.

Features

- Variable power management
- Packaged in 6-lead SOT-23 (ADC081S101 also available in a 6-Lead LLP package)
- Power supply used as reference
- Single +2.7V to +5.25V supply operation
- SPI™/QSPI™/MICROWIRE™/DSP compatible

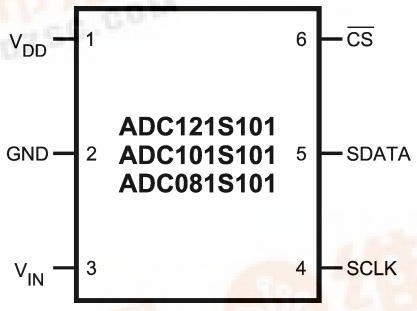
Key Specifications

- Resolution with no Missing Codes 12/10/8 bits
- Conversion Rate 1 MSPS
- DNL (ADC121S101) +0.5, -0.3 LSB (typ)
- INL (ADC121S101) ± 0.4 LSB (typ)
- Power Consumption
  - — 3V Supply 2 mW (typ)
  - — 5V Supply 10 mW (typ)

Applications

- Automotive Navigation
- FA/ATM Equipment
- Portable Systems
- Medical Instruments
- Mobile Communications
- Instrumentation and Control Systems

Connection Diagram



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ADC121S101/ADC101S101/ADC081S101 1MSPS, 12-/10-/8-Bit A/D Converters in SOT-23 & LLP

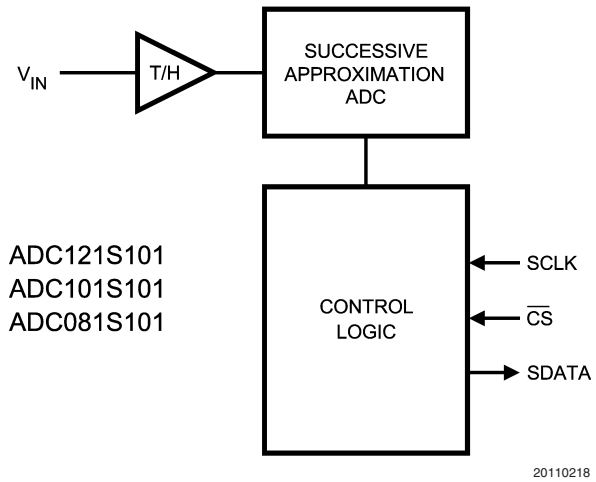
Ordering Information

Order Code	Temperature Range	Description	Top Mark
ADC121S101CIMF	−40˚C to +125˚C	6-Lead SOT-23 Package	X01C
ADC101S101CIMF	−40˚C to +85˚C	6-Lead SOT-23 Package	X02C
ADC081S101CIMF	−40˚C to +85˚C	6-Lead SOT-23 Package	X03C
ADC121S101CIMFX	−40˚C to +125˚C	6-Lead SOT-23 Package, Tape & Reel	X01C
ADC101S101CIMFX	−40˚C to +85˚C	6-Lead SOT-23 Package, Tape & Reel	X02C
ADC081S101CIMFX	−40˚C to +85˚C	6-Lead SOT-23 Package, Tape & Reel	X03C
ADC081S101CISDX	−40˚C to +85˚C	6-Lead LLP Package, Tape & Reel	X3C
ADC081S101CISD	−40˚C to +85˚C	6-Lead LLP Package, Tape & Partial Reel	X3C
ADC121S101EVAL		SOT-23 Evaluation Board	
ADC101S101EVAL		SOT-23 Evaluation Board	
ADC081S101EVAL		SOT-23 Evaluation Board	

Pin Descriptions

Pin No.	Symbol	Description
ANALOG I/O		
3	V_{IN}	Analog input. This signal can range from 0V to V_{DD}.
DIGITAL I/O		
4	SCLK	Digital clock input. The range of frequencies for this input is 10 kHz to 20 MHz, with guaranteed performance at 20 MHz. This clock directly controls the conversion and readout processes.
5	SDATA	Digital data output. The output words are clocked out of this pin by the SCLK pin.
6	$\overline{CS}$	Chip select. A conversion process begins on the falling edge of $\overline{CS}$.
POWER SUPPLY		
1	V_{DD}	Positive supply pin. These pins should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with 0.1 µF and 1 µF monolithic capacitors located within 1 cm of the power pin. The ADC121S101/101S101/081S101 uses this power supply as a reference, so it should be thoroughly bypassed.
2	GND	The ground return for the supply.

Block Diagram



Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{DD}	−0.3V to +6.5V
Voltage on Any Analog Pin to GND	−0.3V to V_{DD} +0.3V
Voltage on Any Digital Pin to GND	-0.3V to 6.5V
Input Current at Any Pin (Note 5)	±10 mA
ESD Susceptibility	
Human Body Model	3500V
Machine Model	200V
Soldering Temperature, Infrared, 10 seconds	215˚C
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 4)

Operating Ratings (Note 2)

Operating Temperature Range	
ADC121S101	−40˚C ≤ T_A ≤ +125˚C
ADC101S101 & ADC081S101	−40˚C ≤ T_A ≤ +85˚C
V_{DD} Supply Voltage	+2.7V to +5.25V
Digital Input Pins Voltage Range (Note 6)	+2.7V to +5.25V

Package Thermal Resistance

Package	θ_{JA}
6-Lead SOT-23	265˚C / W
6-Lead LLP	94˚C / W

ADC121S101 Converter Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS (V_{DD} = 2.7V to 3.6V)					
	Resolution with No Missing Codes	−40˚C ≤ T_A ≤ 125˚C		**12**	Bits
INL	Integral Non-Linearity	−40˚C ≤ T_A ≤ 85˚C	±0.4	**±1**	LSB (max)
		T_A = 125˚C		+1 -1.1	LSB (min) LSB (max)
DNL	Differential Non-Linearity	−40˚C ≤ T_A ≤ 85˚C	+0.5 -0.3	**+1** **-0.9**	LSB (max) LSB (min)
		T_A = 125˚C		±1	LSB (max)
V_{OFF}	Offset Error	−40˚C ≤ T_A ≤ 125˚C	±0.1	**±1.2**	LSB (max)
GE	Gain Error	−40˚C ≤ T_A ≤ 125˚C	±0.2	**±1.2**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS (f_{IN} = 100 kHz, -0.02 dBFS sine wave unless otherwise noted)					
SINAD	Signal-to-Noise Plus Distortion Ratio	−40˚C ≤ T_A ≤ 125˚C	72	**70**	dB (min)
SNR	Signal-to-Noise Ratio	−40˚C ≤ T_A ≤ 85˚C	72.5	**70.8**	dB (min)
		T_A = 125˚C		70.6	dB (min)
THD	Total Harmonic Distortion		-80		dB
SFDR	Spurious-Free Dynamic Range		82		dB
IMD	Intermodulation Distortion, Second Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
	Intermodulation Distortion, Third Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
FPBW	-3 dB Full Power Bandwidth	+5V Supply	11		MHz
		+3V Supply	8		MHz
POWER SUPPLY CHARACTERISTICS					
V_{DD}	Supply Voltage	−40˚C ≤ T_A ≤ 125˚C		**2.7** **5.25**	V (min) V (max)

ADC121S101 Converter Electrical Characteristics (Continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = –40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
POWER SUPPLY CHARACTERISTICS					
I_{DD}	Normal Mode (Static)	V_{DD} = +4.75V to +5.25V, SCLK On or Off	2		mA
		V_{DD} = +2.7V to +3.6V, SCLK On or Off	1		mA
	Normal Mode (Operational)	V_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS	2.0	**3.2**	mA (max)
		V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS	0.6	**1.5**	mA (max)
	Shutdown Mode	V_{DD} = +5V, SCLK Off	0.5		µA
		V_{DD} = +5V, SCLK On	60		µA
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5V, f_{SAMPLE} = 1 MSPS	10	**16**	mW (max)
		V_{DD} = +3V, f_{SAMPLE} = 1 MSPS	2	**4.5**	mW (max)
	Power Consumption, Shutdown Mode	V_{DD} = +5V, SCLK Off	2.5		µW
		V_{DD} = +3V, SCLK Off	1.5		µW
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_{DD}		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Input Capacitance (Note 3)		30		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage			**2.4**	V (min)
V_{IL}	Input Low Voltage	V_{DD} = +5V		**0.8**	V (max)
		V_{DD} = +3V		**0.4**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_{DD}	±10 nA	**±1**	µA (max)
C_{IND}	Input Capacitance (Note 3)		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, V_{DD} = +2.7V to +5.25V		**V_{DD} –0.2**	V (min)
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OL}	TRI-STATE Leakage Current			**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency			**20**	MHz (max)
DC	SCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{TH}	Track/Hold Acquisition Time			**400**	ns (max)
f_{RATE}	Throughput Rate	See Serial Interface Section		**1**	MSPS (max)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

ADC101S101 Converter Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = –40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10**	Bits
INL	Integral Non-Linearity		±0.2	**±0.7**	LSB (max)
DNL	Differential Non-Linearity		+0.3 -0.2	**±0.7**	LSB (max) LSB (max)
V_{OFF}	Offset Error		±0.1	**±0.7**	LSB (max)
GE	Gain Error		±0.2	**±1**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz	61.7	**61**	dBFS (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz	62		dB
THD	Total Harmonic Distortion	f_{IN} = 100 kHz	-77	**-73**	dB (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz	78	**74**	dB (min)
IMD	Intermodulation Distortion, Second Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
	Intermodulation Distortion, Third Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
FPBW	-3 dB Full Power Bandwidth	+5V Supply	11		MHz
		+3V Supply	8		MHz
POWER SUPPLY CHARACTERISTICS					
V_{DD}	Supply Voltage			**2.7** **5.25**	V (min) V (max)
I_{DD}	Normal Mode (Static)	V_{DD} = +4.75V to +5.25V, SCLK On or Off	2		mA
		V_{DD} = +2.7V to +3.6V, SCLK On or Off	1		mA
	Normal Mode (Operational)	V_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS	2.0	**3.2**	mA (max)
		V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS	0.6	**1.5**	mA (max)
	Shutdown Mode	V_{DD} = +5V, SCLK Off	0.5		µA (max)
		V_{DD} = +5V, SCLK On	60		µA (max)
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5V, f_{SAMPLE} = 1 MSPS	10	**16**	mW (max)
		V_{DD} = +3V, f_{SAMPLE} = 1 MSPS	2	**4.5**	mW (max)
	Power Consumption, Shutdown Mode	V_{DD} = +5V, SCLK Off	2.5		µW (max)
		V_{DD} = +3V, SCLK Off	1.5		µW (max)
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_{DD}		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Input Capacitance (Note 3)		30		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage			**2.4**	V (min)
V_{IL}	Input Low Voltage	V_{DD} = +5V		**0.8**	V (max)
		V_{DD} = +3V		**0.4**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_{DD}	±10 nA	**±1**	µA (max)
C_{IND}	Input Capacitance (Note 3)		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, V_{DD} = +2.7V to +5.25V		**V_{DD} –0.2**	V (min)

ADC101S101 Converter Electrical Characteristics (Continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = –40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
DIGITAL OUTPUT CHARACTERISTICS					
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OL}	TRI-STATE Leakage Current			**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance (Note 3)		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency			**20**	MHz (max)
DC	SCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{TH}	Track/Hold Acquisition Time			**400**	ns (max)
f_{RATE}	Throughput Rate	See Serial Interface Section		**1**	MSPS (max)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

ADC081S101 Converter Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = –40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted.

Symbol	Parameter	Conditions		Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**8**	Bits
INL	Integral Non-Linearity			±0.05	**±0.3**	LSB (max)
DNL	Differential Non-Linearity			±0.07	**±0.3**	LSB (max)
V_{OFF}	Offset Error			±0.03	**±0.3**	LSB (max)
GE	Gain Error			±0.08	**±0.4**	LSB (max)
	Total Unadjusted Error			±0.07	**±0.3**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz		49.7	**49**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz		49.7		dB
THD	Total Harmonic Distortion	f_{IN} = 100 kHz		-77	**-65**	dB (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz		69	**65**	dB (min)
IMD	Intermodulation Distortion, Second Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz		-68		dB
	Intermodulation Distortion, Third Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz		-68		dB
FPBW	-3 dB Full Power Bandwidth	+5V Supply		11		MHz
		+3V Supply		8		MHz
POWER SUPPLY CHARACTERISTICS						
V_{DD}	Supply Voltage				**2.7** **5.25**	V (min) V (max)
I_{DD}	Normal Mode (Static)	V_{DD} = +4.75V to +5.25V, SCLK On or Off		2		mA
		V_{DD} = +2.7V to +3.6V, SCLK On or Off		1		mA
	Normal Mode (Operational)	V_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS	SOT-23	2.0	**3.2**	mA (max)
			LLP		**2.6**	
		V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS	SOT-23	0.6	**1.5**	mA (max)
			LLP		**1.1**	
	Shutdown Mode	V_{DD} = +5V, SCLK Off		0.5		µA (max)
		V_{DD} = +5V, SCLK On		60		µA (max)
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5V, f_{SAMPLE} = 1 MSPS	SOT-23	10	**16**	mW (max)
			LLP		**13**	
		V_{DD} = +3V, f_{SAMPLE} = 1 MSPS		2	**4.5**	mW (max)
	Power Consumption, Shutdown Mode	V_{DD} = +5V, SCLK Off		2.5		µW (max)
		V_{DD} = +3V, SCLK Off		1.5		µW (max)
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input Range			0 to V_{DD}		V
I_{DCL}	DC Leakage Current				**±1**	µA (max)
C_{INA}	Input Capacitance			30		pF
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage				**2.4**	V (min)
V_{IL}	Input Low Voltage	V_{DD} = +5V			**0.8**	V (max)
		V_{DD} = +3V			**0.4**	V (max)
I_{IN}	Digital Input Current	V_{IN} = 0V or V_{DD}		±10 nA	**±1**	µA (max)
C_{IND}	Input Capacitance(Note 3)			2	**4**	pF (max)

ADC081S101 Converter Electrical Characteristics (Continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = –40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, V_{DD} = +2.7V to +5.25V		**V_{DD} – 0.2**	V (min)
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OL}	TRI-STATE Leakage Current			**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance (Note 3)		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency			**20**	MHz (max)
DC	SCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{TH}	Track/Hold Acquisition Time			**400**	ns (max)
f_{RATE}	Throughput Rate	See Applications Section		**1**	MSPS (min)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

ADC121S101/ADC101S101/ADC081S101 Timing Specifications

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, **Boldface limits apply for T_A = −40˚C to +85˚C**: all other limits T_A = 25˚C, unless otherwise noted. (Note 11)

Symbol	Parameter	Conditions	Typical	Limits	Units
$t_{CONVERT}$			16 x t_{SCLK}		
t_{QUIET}	(Note 7)			**50**	ns (min)
t_1	Minimum $\overline{CS}$ Pulse Width			**10**	ns (min)
t_2	$\overline{CS}$ to SCLK Setup Time			**10**	ns (min)
t_3	Delay from $\overline{CS}$ Until SDATA TRI-STATE® Disabled (Note 8)			**20**	ns (max)
t_4	Data Access Time after SCLK Falling Edge(Note 9)	V_{DD} = +2.7 to +3.6		**40**	ns (max)
		V_{DD} = +4.75 to +5.25		**20**	ns (max)
t_5	SCLK Low Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_6	SCLK High Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_7	SCLK to Data Valid Hold Time	V_{DD} = +2.7 to +3.6		**7**	ns (min)
		V_{DD} = +4.75 to +5.25		**5**	ns (min)
t_8	SCLK Falling Edge to SDATA High Impedance (Note 10)	V_{DD} = +2.7 to +3.6		**25** **6**	ns (max) ns (min)
		V_{DD} = +4.75 to +5.25		**25** **5**	ns (max) ns (min)
$t_{POWER-UP}$	Power-Up Time from Full Power-Down		1		µs

Note 1: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 2: All voltages are measured with respect to GND = 0V, unless otherwise specified

Note 3: Specification limit guaranteed by design.

Note 4: See the section titled "Surface Mount" found in a current National Semiconductor Linear Databook for other methods of soldering suface mount devices.

Note 5: Except power supply pins.

Note 6: Independent of supply voltage.

Note 7: Minimum Quiet Time Required Between Bus Relinquish and Start of Next Conversion

Note 8: Measured with the load circuit shown above, and defined as the time taken by the output to cross 1.0V.

Note 9: Measured with the load circuit shown above, and defined as the time taken by the output to cross 1.0V or 2.0V.

Note 10: t_8 is derived from the time taken by the outputs to change by 0.5V with the loading circuit shown above. The measured number is then adjusted to remove the effects of charging or discharging the 25pF capacitor. This means t_8 is the true bus relinquish time, independent of the bus loading.

Note 11: All input signals are specified as $t_r = t_f$ = 5 ns (10% to 90% V_{DD}) and timed from 1.6V.

Specification Definitions

APERTURE DELAY is the time after the falling edge of $\overline{CS}$ to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB for ADC121S101 and ADC101S101, V_{REF} - 1 LSB for ADC081S101), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the either the two second order or all four third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC121S101/101S101/081S101 is guaranteed not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB for the ADC121S101 and ADC101S101, and GND + 1 LSB for the ADC081S101).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

where Af_1 is the RMS power of the fundamental (output) frequency and Af_2 through Af_6 are the RMS power in the first 5 harmonic frequencies.

TOTAL UNADJUSTED ERROR is the worst deviation found from the ideal transfer function. As such, it is a comprehensive specification which includes full scale error, linearity error, and offset error.

Timing Diagrams

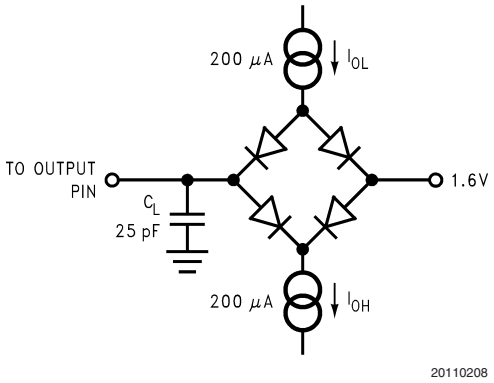


FIGURE 1. Timing Test Circuit

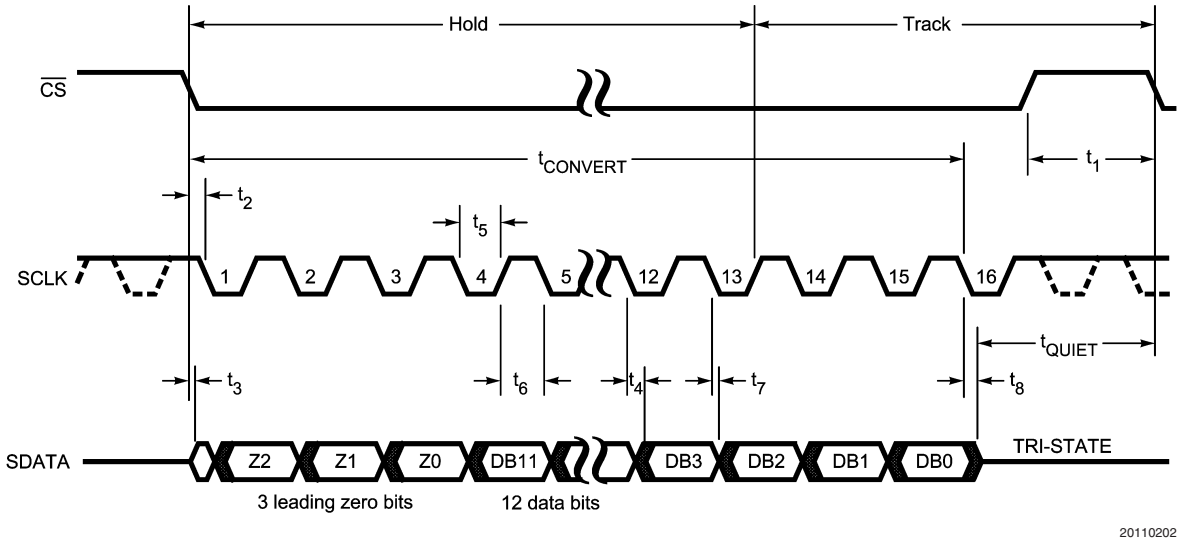


FIGURE 2. ADC121S101 Serial Interface Timing Diagram

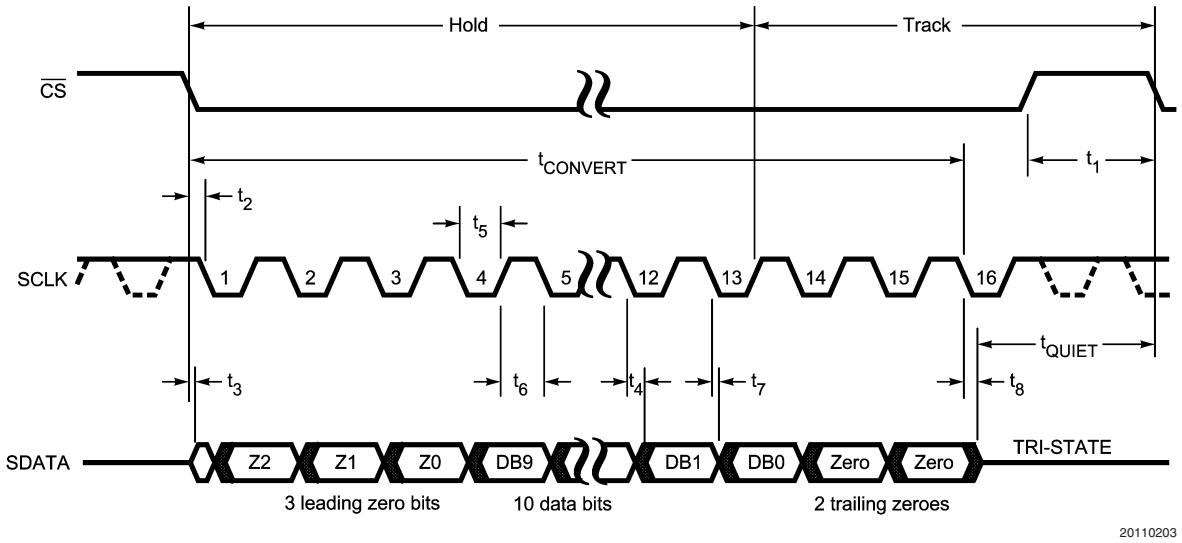


FIGURE 3. ADC101S101 Serial Interface Timing Diagram

Timing Diagrams (Continued)

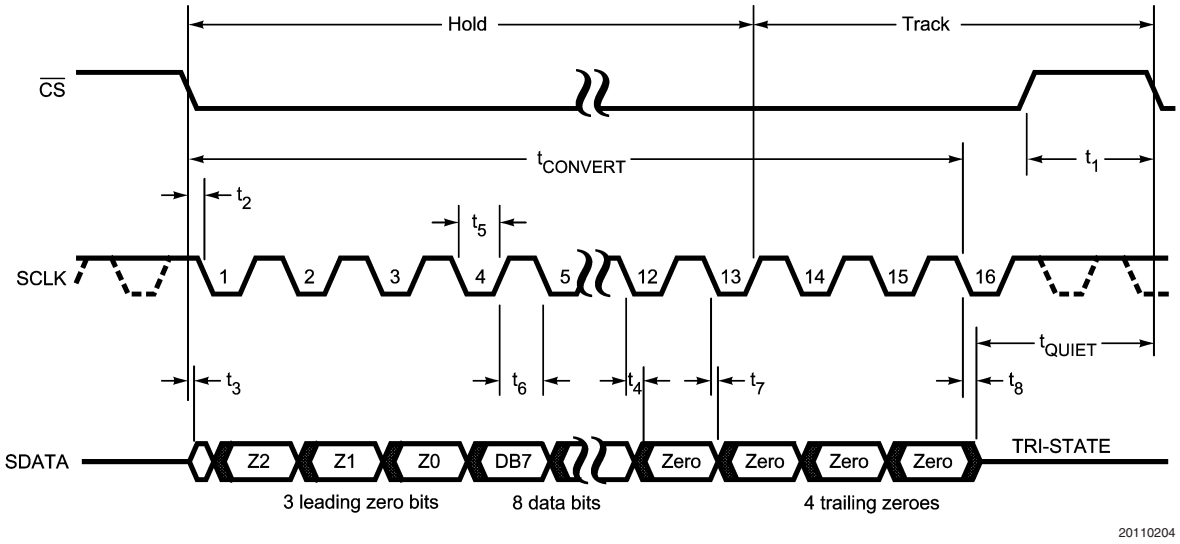


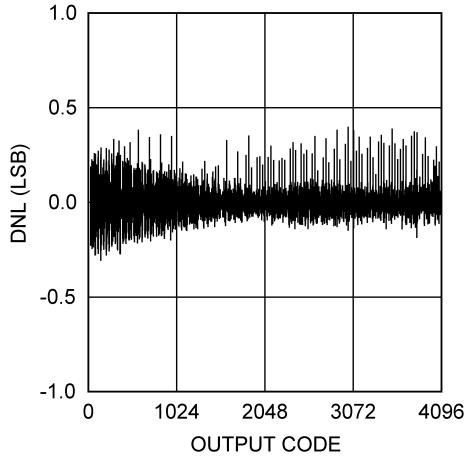
FIGURE 4. ADC081S101 Serial Interface Timing Diagram

Typical Performance Characteristics

T_A = +25˚C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

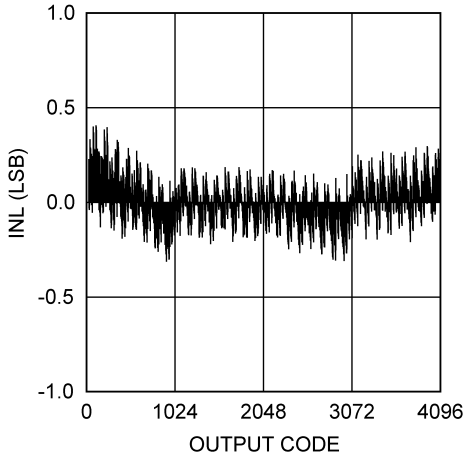
ADC121S101

ADC121S101 DNL



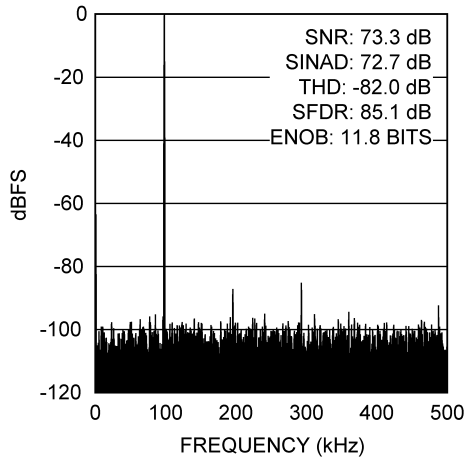
20110206

ADC121S101 INL



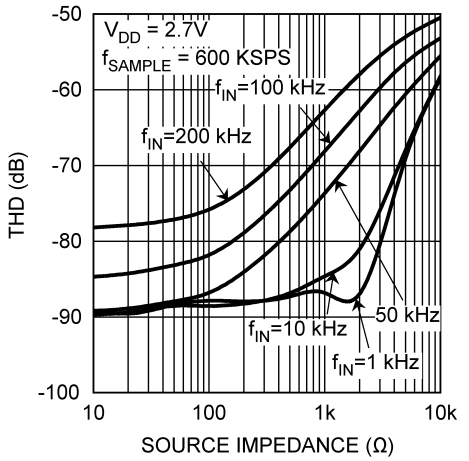
20110205

ADC121S101 Spectral Response @ 100 kHz Input



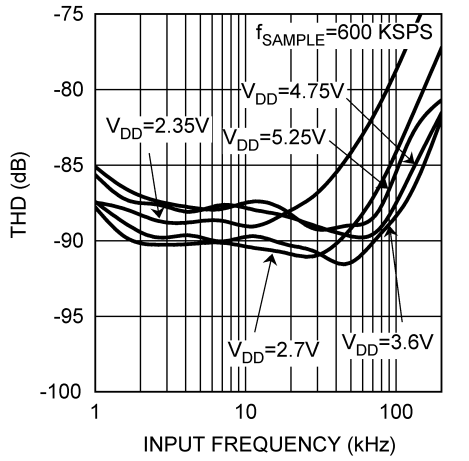
20110207

ADC121S101 THD vs. Source Impedance



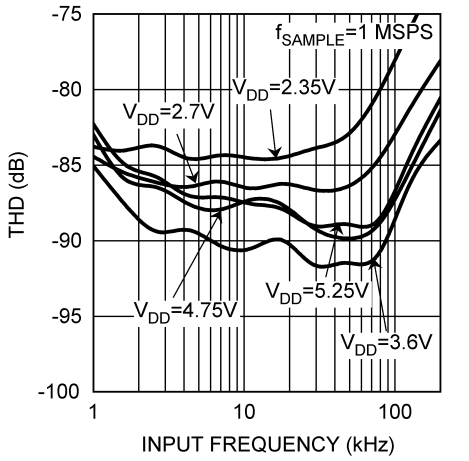
20110250

ADC121S101 THD vs. Input Frequency, 600 kSPS



20110251

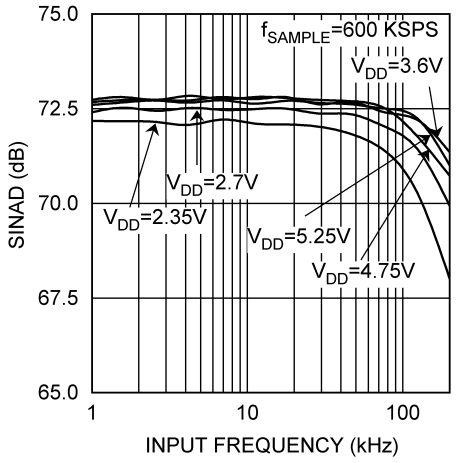
ADC121S101 THD vs. Input Frequency, 1 MSPS



20110252

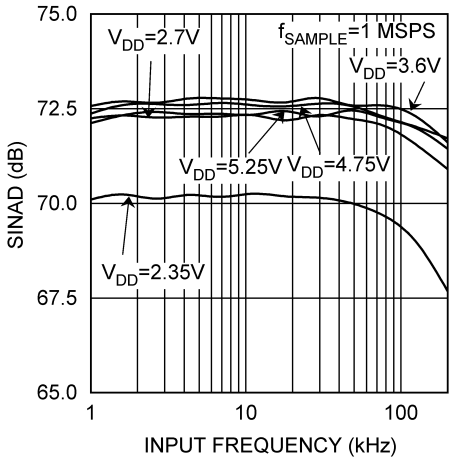
Typical Performance Characteristics T_A = +25˚C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated. (Continued)

ADC121S101 SINAD vs. Input Frequency, 600 kSPS



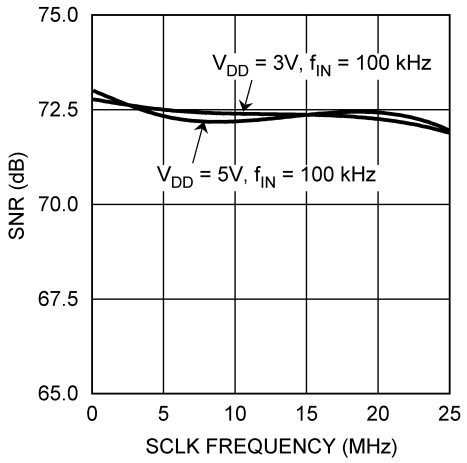
20110253

ADC121S101 SINAD vs. Input Frequency, 1 MSPS



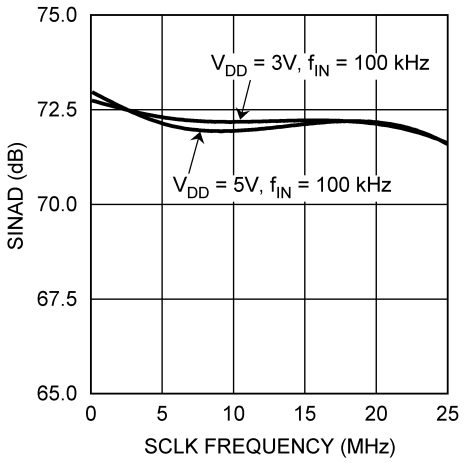
20110254

ADC121S101 SNR vs. f_{SCLK}



20110256

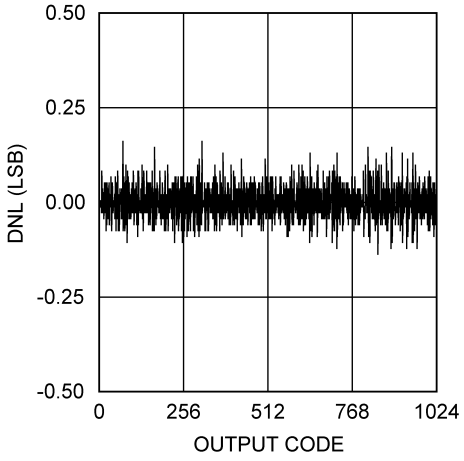
ADC121S101 SINAD vs. f_{SCLK}



20110257

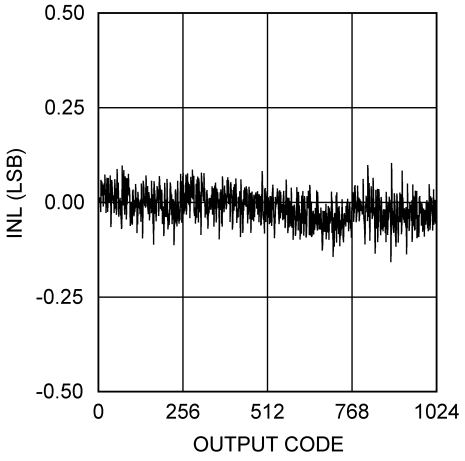
Typical Performance Characteristics T_A = +25˚C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated. (Continued)

ADC101S101 DNL



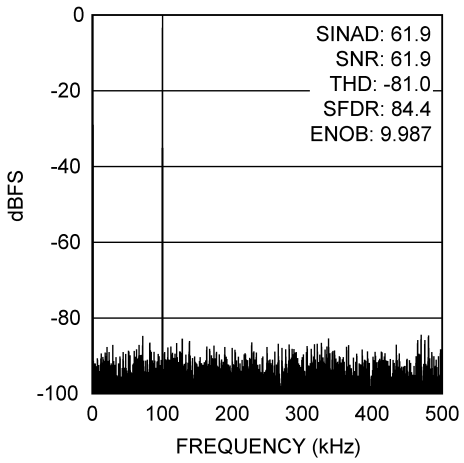
20110270

ADC101S101 INL



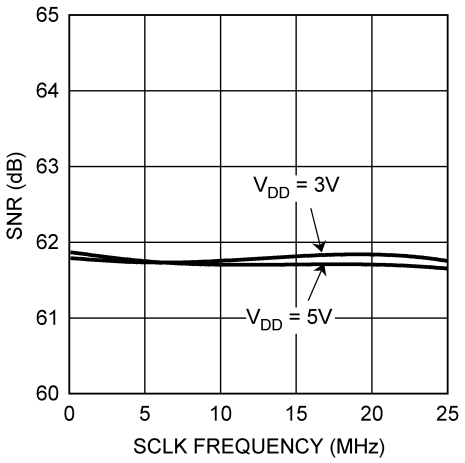
20110271

ADC101S101 Spectral Response @ 100 kHz Input



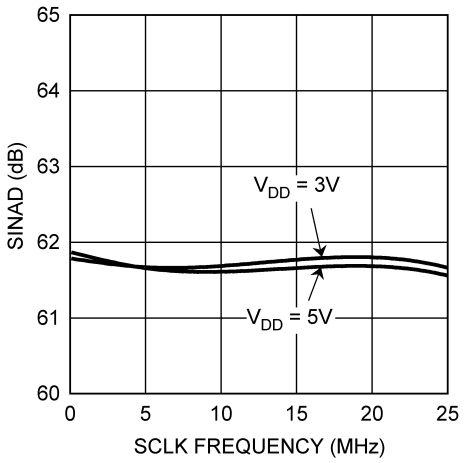
20110272

ADC101S101 SNR vs. f_{SCLK}



20110273

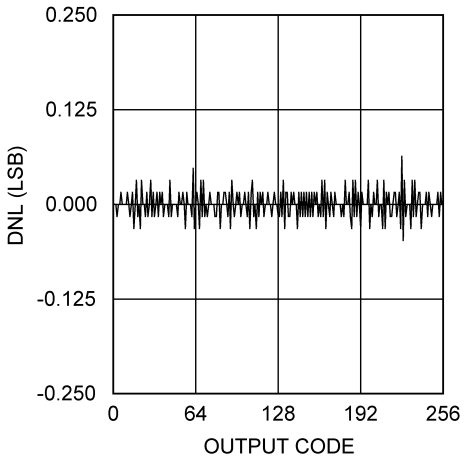
ADC101S101 SINAD vs. f_{SCLK}



20110274

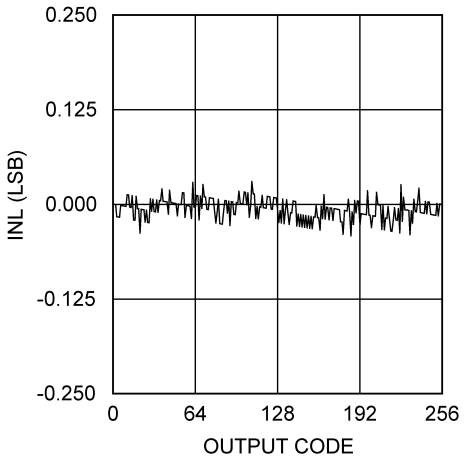
Typical Performance Characteristics T_A = +25˚C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated. (Continued)

ADC081S101 DNL



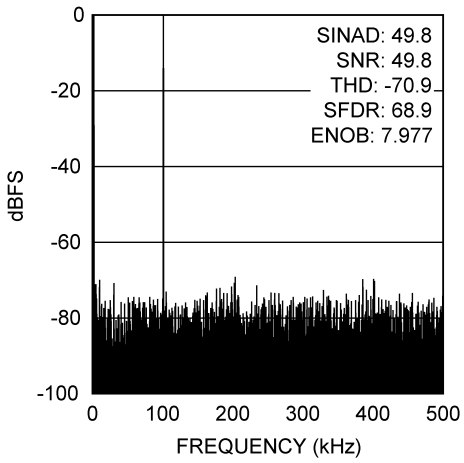
20110260

ADC081S101 INL



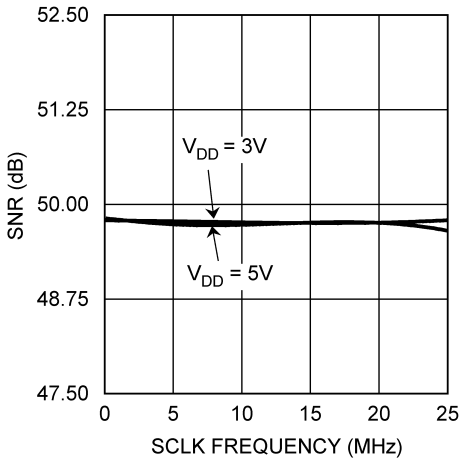
20110261

ADC081S101 Spectral Response @ 100 kHz Input



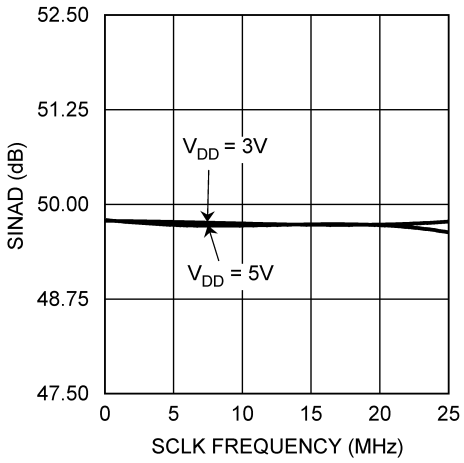
20110262

ADC081S101 SNR vs. f_{SCLK}



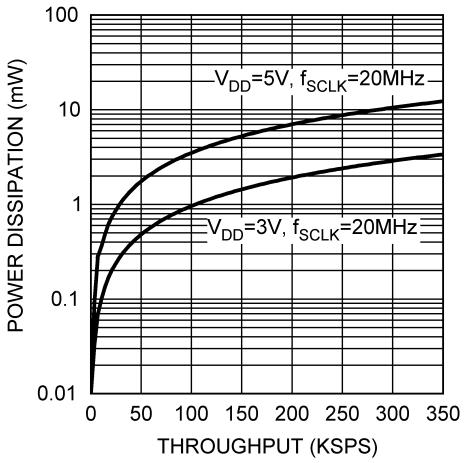
20110263

ADC081S101 SINAD vs. f_{SCLK}



20110264

Power Consumption vs. Throughput



20110255

Applications Information

1.0 ADC121S101/101S101/081S101 OPERATION

The ADC121S101/101S101/081S101 are successive-approximation analog-to-digital converters designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADC121S101/101S101/081S101 in both track and hold operation are shown in Figures 4 and 5, respectively. In Figure 4, the device is in track mode: switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

Figure 5 shows the device in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode on the 13th rising edge of SCLK.

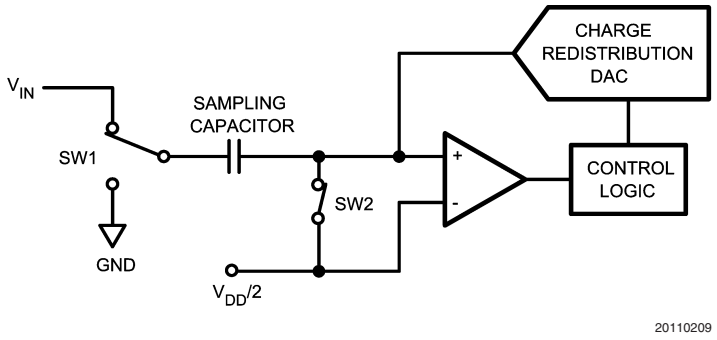


FIGURE 5. ADC121S101/101S101/081S101 in Track Mode

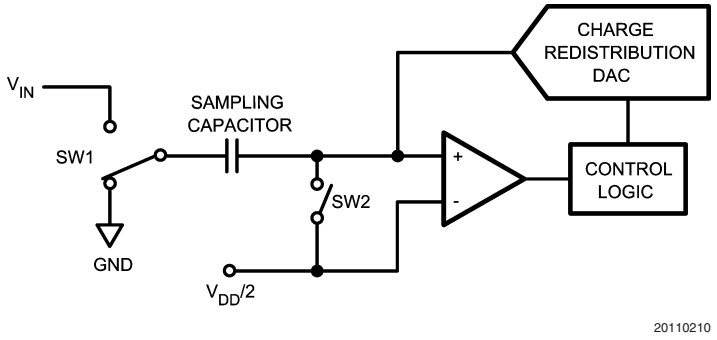


FIGURE 6. ADC121S101/101S101/081S101 in Hold Mode

2.0 USING THE ADC121S101/101S101/081S101

Serial interface timing diagrams for the ADC121S101/101S101/081S101 are shown in Figures 1, 2, and 3. $\overline{CS}$ is chip select, which initiates conversions on the ADC121S101/101S101/081S101 and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found as a serial data stream.

Basic operation of the ADC121S101/101S101/081S101 begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labelled with reference to the falling edge of $\overline{CS}$; for example, "the third falling edge of SCLK" shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion on the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 1, 2, or 3). The SDATA pin will be placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time t_{QUIET} must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADC121S101/101S101/081S101. The sample bits (including any leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. The ADC121S101/101S101/081S101 will produce three leading zero bits on SDATA, followed by twelve, ten, or eight data bits, most significant first. After the data bits, the ADC101S101 will clock out two trailing zeros, and the ADC081S101 will clock out four trailing zeros. The ADC121S101 will not clock out any trailing zeros; the least significant data bit will be valid on the 16th falling edge of SCLK.

Applications Information (Continued)

If $\overline{CS}$ goes low before the rising edge of SCLK, an additional (fourth) zero bit may be captured by the next falling edge of SCLK.

3.0 ADC121S101/101S101/081S101 TRANSFER FUNCTION

The output format of the ADC121S101/101S101/081S101 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB widths for the ADC121S101 is V_{DD} / 4096; for the ADC101S101 the LSB width is V_{DD} / 1024; for the ADC081S101, the LSB width is V_{DD} / 256. The ideal transfer characteristic for the ADC121S101 and ADC101S101 is shown in Figure 6, while the ideal transfer characteristic for the ADC081S101 is shown in Figure 7.

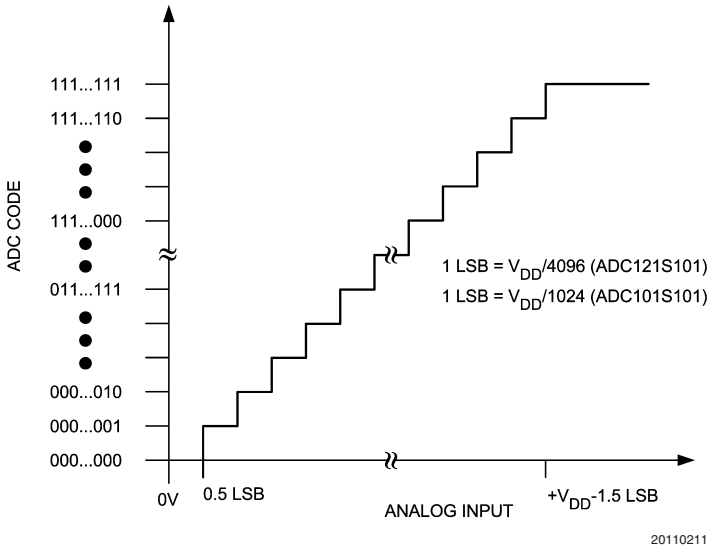


FIGURE 7. ADC121S101/101S101 Ideal Transfer Characteristic

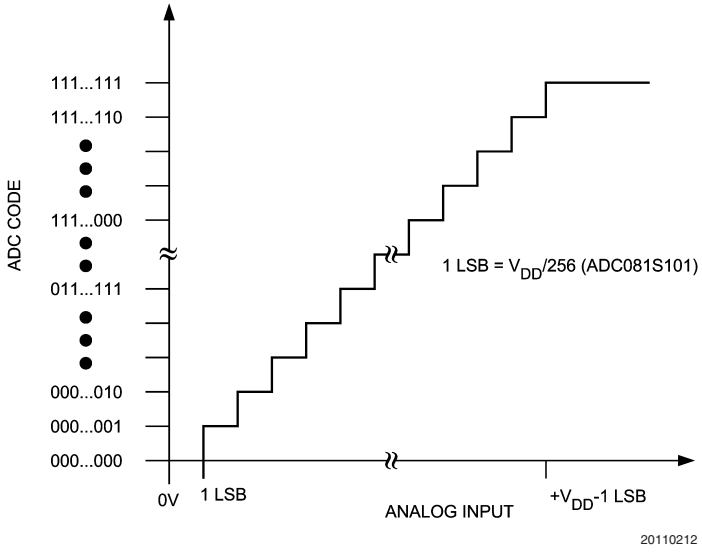


FIGURE 8. ADC081S101 Ideal Transfer Characteristic

Applications Information (Continued)

4.0 SAMPLE CIRCUIT

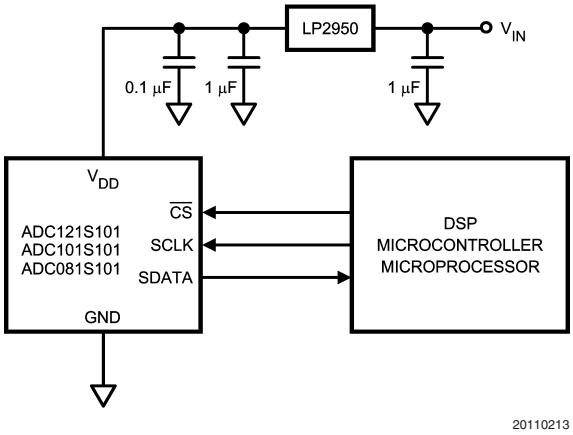


FIGURE 9. Sample Circuit

A typical application of the ADC121S101/101S101/081S101 is shown in Figure 8. The combined analog and digital supplies are provided in this example by the National LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The supply is bypassed with a capacitor network located close to the device. The three-wire interface is also shown connected to a microprocessor or DSP.

5.0 ANALOG INPUTS

An equivalent circuit for the ADC121S101/101S101/081S101 input channel is shown in Figure 9. The diodes D1 and D2 provide ESD protection for the analog inputs. At no time should an analog input exceed V_{DD} + 300 mV or GND - 300 mV, as these ESD diodes will begin conducting current into the substrate and affect ADC operation.

The capacitor C1 in Figure 9 typically has a value of 4 pF, and is mainly due to pin capacitance. The resistor R1 represents the on resistance of the multiplexer and track / hold switch, and is typically 100 ohms. The capacitor C2 is the ADC121S101/101S101/081S101 sampling capacitor, and is typically 26 pF.

The sampling nature of the analog input causes input current pulses that result in voltage spikes at the input. The ADC121S101/101S101/081S101 will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. In applications where dynamic performance is critical, the input might need to be driven with a low output-impedance amplifier. In addition, when using the ADC121S101/101S101/081S101 to sample AC signals, a band-pass or low-pass filter will reduce harmonics and noise and thus improve THD and SNR.

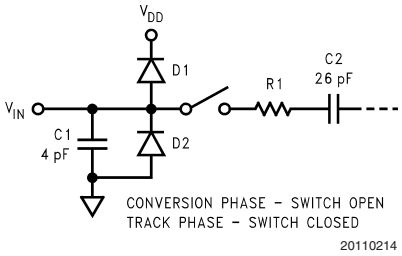


FIGURE 10. Equivalent Input Circuit

6.0 DIGITAL INPUTS AND OUTPUTS

The ADC121S101/101S101/081S101 digital inputs (SCLK and $\overline{CS}$) are not limited by the same absolute maximum ratings as the analog inputs. The digital input pins are instead limited to +6.5V with respect to GND, regardless of V_{DD}, the supply voltage. This allows the ADC121S101/101S101/081S101 to be interfaced with a wide range of logic levels, independent of the supply voltage.

Note that, even though the digital inputs are tolerant of up to +6.5V above GND, the digital outputs are only capable of driving V_{DD} out. In addition, the digital input pins are not prone to latch-up; SCLK and $\overline{CS}$ may be asserted before V_{DD} without any risk.

7.0 MODES OF OPERATION

The ADC121S101/101S101/081S101 has two possible modes of operation: normal mode, and shutdown mode. The ADC121S101/101S101/081S101 enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device will enter shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or will stay in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device will stay there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade-off throughput for power consumption.

8.0 NORMAL MODE

The best possible throughput is obtained by leaving the ADC121S101/101S101/081S101 in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device will remain in normal mode, but the current conversion will be aborted, and SDATA will return to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

Applications Information (Continued)

9.0 SHUTDOWN MODE

Shutdown mode is appropriate for applications that either do not sample continuously, or are willing to trade throughput for power consumption. When the ADC121S101/101S101/081S101 is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ back high anytime between the second and tenth falling edges of SCLK, as shown in Figure 10. Once $\overline{CS}$ has been brought high in this manner, the device will enter shutdown mode; the current conversion will be aborted and SDATA will enter TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device will not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.

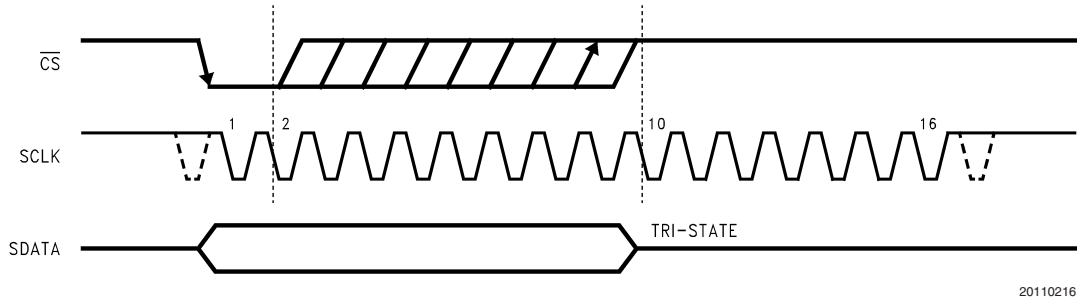


FIGURE 11. Entering Shutdown Mode

10.0 EXITING SHUTDOWN MODE

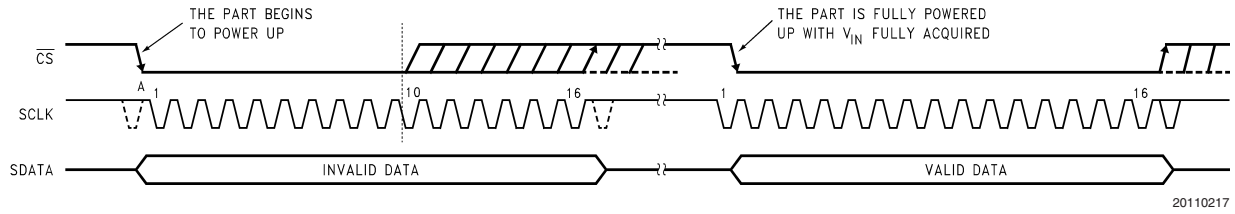


FIGURE 12. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADC121S101/101S101/081S101 will begin powering up. Power up typically takes 1 µs. This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 11.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device will return to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The ADC121S101/101S101/081S101 will be fully powered-up after 16 SCLK cycles.

11.0 POWER-UP TIMING

The ADC121S101/101S101/081S101 typically requires 1 µs to power up, either after first applying V_{DD}, or after returning to normal mode from shutdown mode. This corresponds to one "dummy" conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADC121S101/101S101/081S101 will perform conversions properly. Note that the t_{QUIET} time must still be included between the first dummy conversion and the second valid conversion.

12.0 STARTUP MODE

When the V_{DD} supply is first applied, the ADC121S101/101S101/081S101 may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, exactly as described in Section 11.0. The part may then be placed into either normal mode or the shutdown mode, as described in Sections 8.0 and 9.0.

13.0 POWER MANAGEMENT

When the ADC121S101/101S101/081S101 is operated continuously in normal mode, throughput up to 1 MSPS can be achieved. The user may trade throughput for power consumption by simply performing fewer conversions per unit time, and putting the ADC121S101/101S101/081S101 into shutdown mode between conversions. This method is not advantageous beyond 350 kSPS throughput.

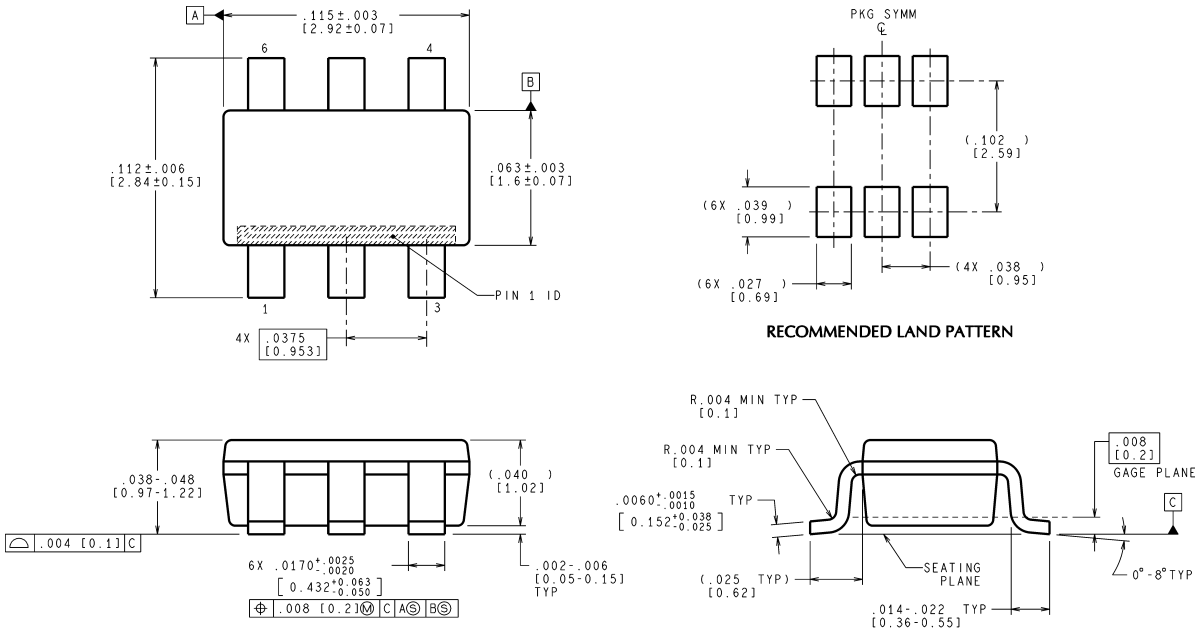
A plot of maximum power consumption versus throughput is shown in Figure 12 below. To calculate the power consumption for a given throughput, remember that each time the part exits shutdown mode and enters normal mode, one dummy conversion is required. Generally, the user will put the part into normal mode, execute one dummy conversion followed by one valid conversion, and then put the part back into shutdown mode. When this is done, the fraction of time

Applications Information (Continued)

spent in normal mode may be calculated by multiplying the throughput (in samples per second) by 2 µs, the time taken to perform one dummy and one valid conversion. The power consumption can then be found by multiplying the fraction of time spent in normal mode by the normal mode power consumption figure. The power dissipated while the part is in shutdown mode is negligible.

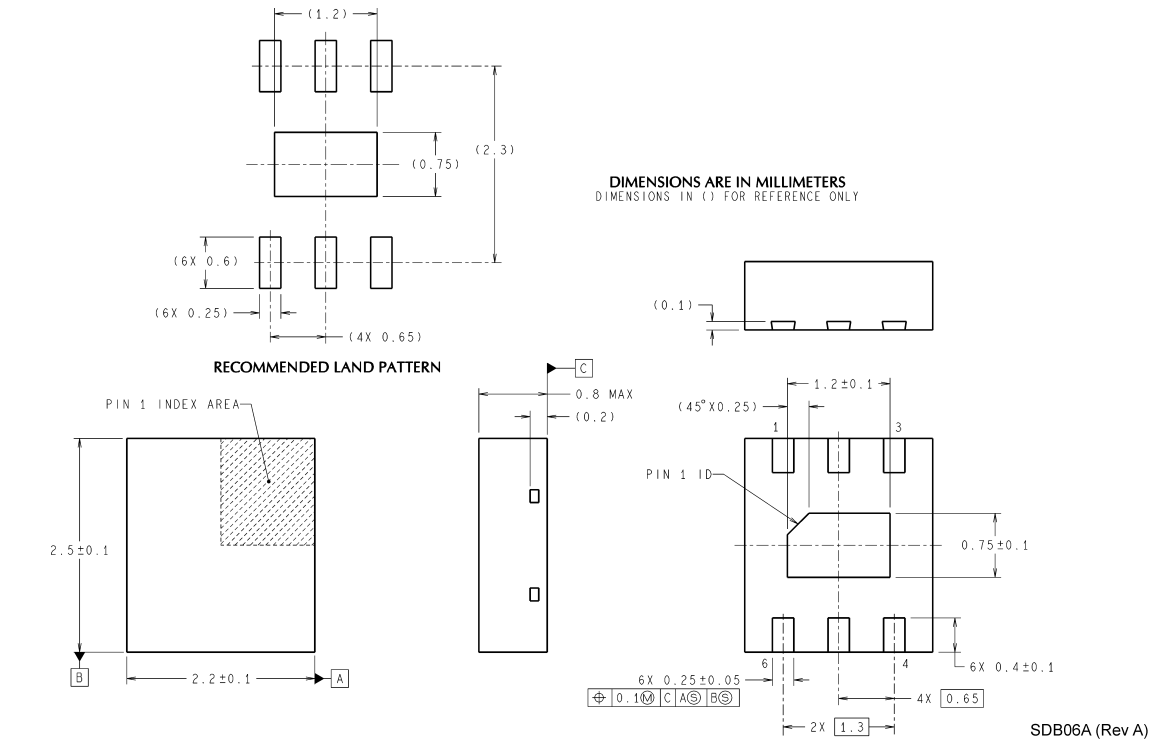
For example, to calculate the power consumption at 300 kSPS with V_{DD} = 5V, begin by calculating the fraction of time spent in normal mode: 300,000 samples/second · 2 µs = 0.6, or 60%. The power consumption at 300 kSPS is then 60% of 17.5 mW (the maximum power consumption at V_{DD} = 5V) or 10.5 mW.

Physical Dimensions inches (millimeters) unless otherwise noted



MF06A (Rev B)

6-Lead SOT-23
Order Number ADC121S101CIMF, ADC121S101CIMFX, ADC101S101CIMF, ADC101S101CIMFX, ADC081S101CIMF or ADC081S101CIMFX
NS Package Number MF06A



SDB06A (Rev A)

6-Lead LLP
Order Number ADC081S101CISD or ADC081S101CISDX
NS Package Number SDB06A

Notes

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