

FAIRCHILD
SEMICONDUCTOR™

February 1990
Revised August 2000

100331 Low Power Triple D-Type Flip-Flop

General Description

The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

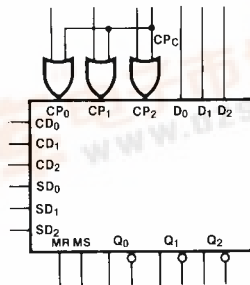
- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range

Ordering Code:

Order Number	Package Number	Package Description
100331SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100331PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100331QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100331QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

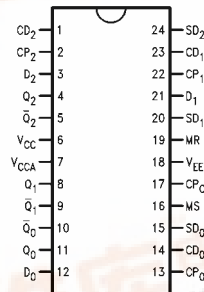
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

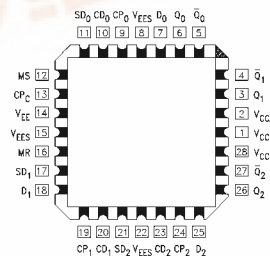


Connection Diagrams

24-Pin DIP/SOIC



28-Pin PLCC



Pin Descriptions

Pin Names	Description
CP ₀ -CP ₂	Individual Clock Inputs
CP _C	Common Clock Input
D ₀ -D ₂	Data Inputs
CD ₀ -CD ₂	Individual Direct Clear Inputs
SD _n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q ₀ -Q ₂	Data Outputs
Q ₀ -Q ₂	Complementary Data Outputs

100331 Low Power Triple D-Type Flip-Flop



Truth Tables

Synchronous Operation (Each Flip-Flop)

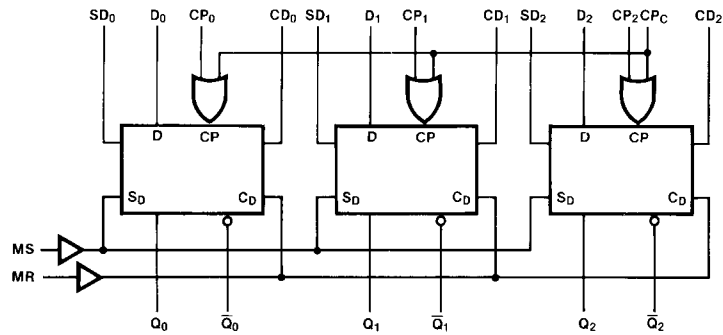
Inputs					Outputs
D _n	CP _n	CP _C	MS SD _n	MR CD _n	Q _n (t + 1)
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	Q _n (t)
X	H	X	L	L	Q _n (t)
X	X	H	L	L	Q _n (t)

Asynchronous Operation (Each Flip-Flop)

Inputs					Outputs
D _n	CP _n	CP _C	MS SD _n	MR CD _n	Q _n (t + 1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 U = Undefined
 t = Time before CP Positive Transition
 t + 1 = Time after CP Positive Transition
 ↗ = LOW-to-HIGH Transition

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Pin Potential to Ground Pin (V_{EE})	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≤ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	Commercial	0°C to +85°C
	Industrial	-40°C to +85°C
Supply Voltage (V_{EE})		-5.7V to -4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version**DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610	mV		
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL}$ (Min)	
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH}$ (Max)	
I_{EE}	Power Supply Current	-122		-65	mA	Inputs OPEN	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued) DIP AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{MAX}	Toggle Frequency	375		375		375		MHz	Figures 2, 3	
t_{PLH} t_{PHL}	Propagation Delay CP _C to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	Figures 1, 3	
t_{PLH} t_{PHL}	Propagation Delay CP _n to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns		
t_{PLH} t_{PHL}	Propagation Delay CD _n , SD _n to Output	0.70	1.70	0.70	1.70	0.70	1.80	ns	CP _n , CP _C = L	Figures 1, 4
t_{PLH} t_{PHL}		0.70	2.00	0.70	2.00	0.70	2.00			
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.60	1.10	2.60	1.10	2.60	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		1.10	2.80	1.10	2.80	1.10	2.80		CP _n , CP _C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	Figures 1, 3, 4	
t_S	Setup Time							ns	Figure 5	
	D _n	0.40		0.40		0.40			Figure 4	
	CD _n , SD _n (Release Time) MS, MR (Release Time)	1.30 2.30		1.30 2.30		1.30 2.30				
t_H	Hold Time D _n	0.5		0.5		0.7		ns	Figure 5	
$t_{PW(H)}$	Pulse Width HIGH CP _n , CP _C , CD _n , SD _n , MR, MS	2.00		2.00		2.00		ns	Figures 3, 4	

SOIC and PLCC AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{MAX}	Toggle Frequency	400		400		400		MHz	Figures 2, 3	
t_{PLH} t_{PHL}	Propagation Delay CP _C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	Figures 1, 3	
t_{PLH} t_{PHL}	Propagation Delay CP _n to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH} t_{PHL}	Propagation Delay CD _n , SD _n to Output	0.70	1.50	0.70	1.50	0.70	1.60	ns	CP _n , CP _C = L	Figures 1, 4
t_{PLH} t_{PHL}		0.80	1.80	0.70	1.80	0.70	1.80			
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		1.10	2.60	1.10	2.60	1.10	2.60		CP _n , CP _C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	Figures 1, 3, 4	
t_S	Setup Time							ns	Figure 5	
	D _n	0.30		0.30		0.30			Figure 4	
	CD _n , SD _n (Release Time) MS, MR (Release Time)	1.20 2.20		1.20 2.20		1.20 2.20				
t_H	Hold Time D _n	0.5		0.5		0.7		ns	Figure 5	
$t_{PW(H)}$	Pulse Width HIGH CP _n , CP _C , CD _n , SD _n , MR, MS	2.00		2.00		2.00		ns	Figures 3, 4	

Commercial Version (Continued)										
Symbol	Parameter	T _C = 0°C		T _C = +25°C		T _C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
t _{PLH} t _{PHL}	Propagation Delay CP _C to Output	0.75	1.40	0.75	1.40	0.80	1.50	ns	Figures 1, 3 PLCC Only	
t _{PLH} t _{PHL}	Propagation Delay CP _n to Output	0.70	1.40	0.75	1.40	0.80	1.50	ns		
t _{PLH} t _{PHL}	Propagation Delay CD _n , SD _n to Output	0.70	1.50	0.70	1.50	0.80	1.60	ns	CP _n , CP _C = L PLCC Only	Figures 1, 4
t _{PLH} t _{PHL}		0.80	1.70	0.80	1.70	0.80	1.80			
t _{PLH} t _{PHL}	Propagation Delay MS, MR to Output	1.10	2.00	1.10	2.00	1.20	2.10	ns	CP _n , CP _C = L PLCC Only	
t _{PLH} t _{PHL}		1.20	2.10	1.20	2.10	1.30	2.20		CP _n , CP _C = H PLCC Only	
t _{OSSL}	Maximum Skew Common Edge Output-to-Output Variation Common Clock to Output Path	100		100		100		ps	PLCC Only (Note 4)	
t _{OSSL}	Maximum Skew Common Edge Output-to-Output Variation CP _n to Output Path	235		235		235		ps	PLCC Only (Note 4)	
t _{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Common Clock to Output Path	120		120		120		ps	PLCC Only (Note 4)	
t _{OSLH}	Maximum Skew Common Edge Output-to-Output Variation CP _n to Output Path	275		275		275		ps	PLCC Only (Note 4)	
t _{OOST}	Maximum Skew Opposite Edge Output-to-Output Variation Common Clock to Output Path	125		125		125		ps	PLCC Only (Note 4)	
t _{OOST}	Maximum Skew Opposite Edge Output-to-Output Variation CP _n to Output Path	265		265		265		ps	PLCC Only (Note 4)	
t _{PS}	Maximum Skew Pin (Signal) Transition Variation Common Clock to Output Path	90		90		90		ps	PLCC Only (Note 4)	
t _{PS}	Maximum Skew Pin (Signal) Transition Variation CP _n to Output Path	90		90		90		ps	PLCC Only (Note 4)	
<p>Note 4: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSSL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OOST}). Parameters t_{OOST} and t_{PS} guaranteed by design.</p>										

Industrial Version

PLCC DC Electrical Characteristics (Note 5)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage		-1565		-1610	mV		
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		0.5		μA	$V_{IN} = V_{IL}$ (Min)	
I_{IH}	Input HIGH Current	300		240		μA	$V_{IN} = V_{IH}$ (Max)	
I_{EE}	Power Supply Current	-122	-60	-122	-65	mA	Inputs Open	

Note 5: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{MAX}	Toggle Frequency	375		400		400		MHz	Figures 2, 3	
t_{PLH}	Propagation Delay CP _C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	Figures 1, 3	
t_{PHL}	Propagation Delay CP _n to Output	0.70	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH}	Propagation Delay CD _n , SD _n to Output	0.60	1.50	0.70	1.50	0.70	1.60	ns	CP _n , CP _C = L	Figures 1, 4
t_{PHL}	Propagation Delay CD _n , SD _n to Output								0.70	
t_{PLH}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	CP _n , CP _C = L	
t_{PHL}	Propagation Delay MS, MR to Output								1.10	
t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.35	1.10	0.35	1.10	ns	Figures 1, 3, 4	
t_S	Setup Time	1.00		0.30		0.30		ns	Figure 5	
	CD _n , SD _n (Release Time)	1.50		1.20		1.20			Figure 4	
	MS, MR (Release Time)	2.50		2.20		2.20				
t_H	Hold Time D _n	0.7		0.5		0.7		ns	Figure 5	
$t_{PW(H)}$	Pulse Width HIGH CP _n , CP _C , CD _n , SD _n , MR, MS	2.00		2.00		2.00		ns	Figures 3, 4	

Switching Waveforms

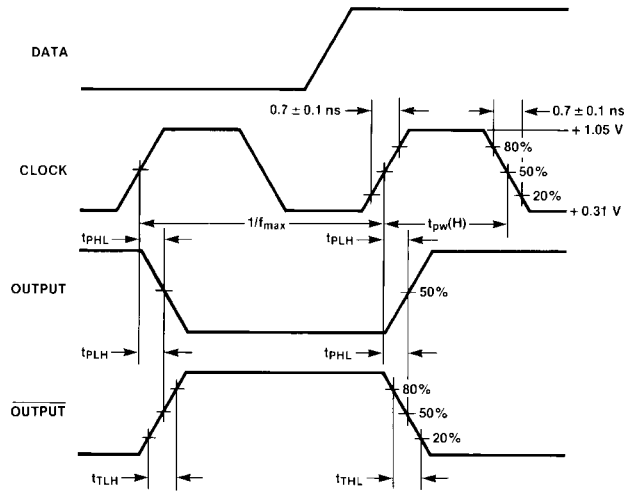


FIGURE 3. Propagation Delay (Clock) and Transition Times

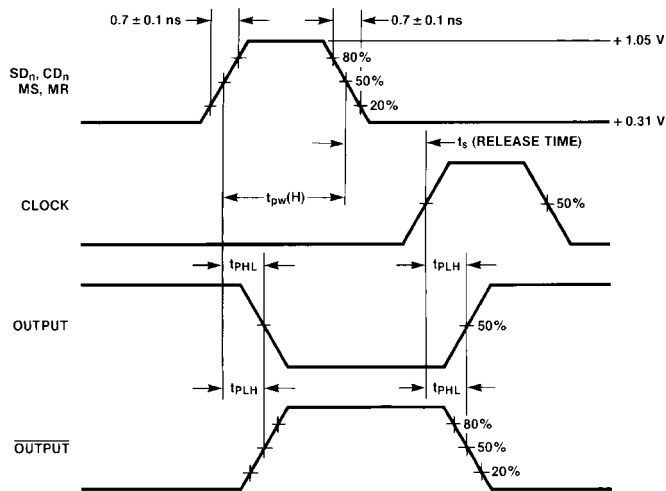


FIGURE 4. Propagation Delay (Resets)

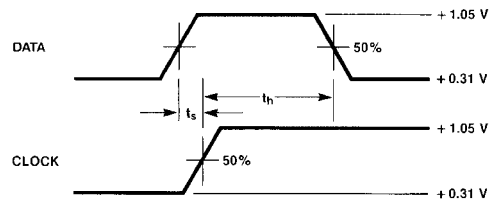


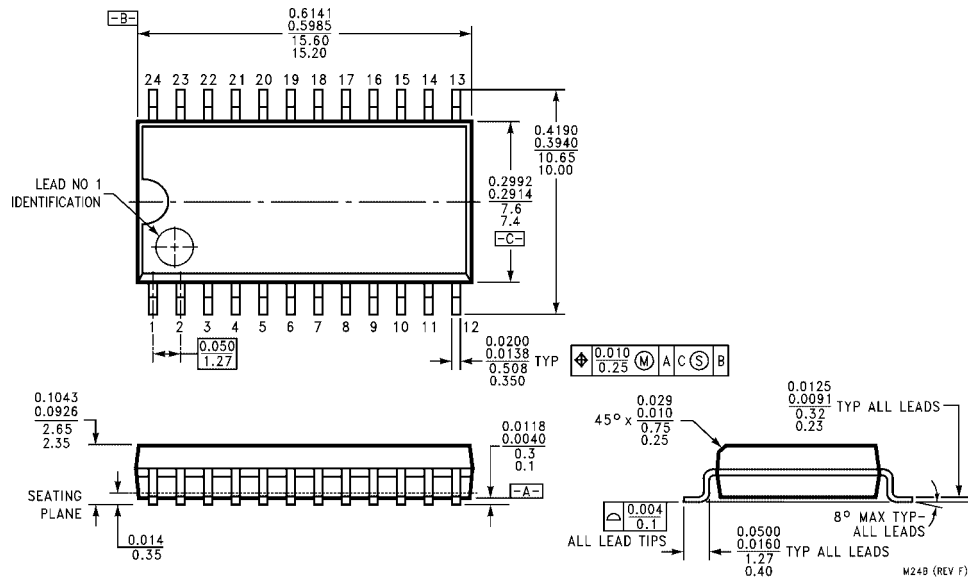
FIGURE 5. Data Setup and Hold Time

Note:

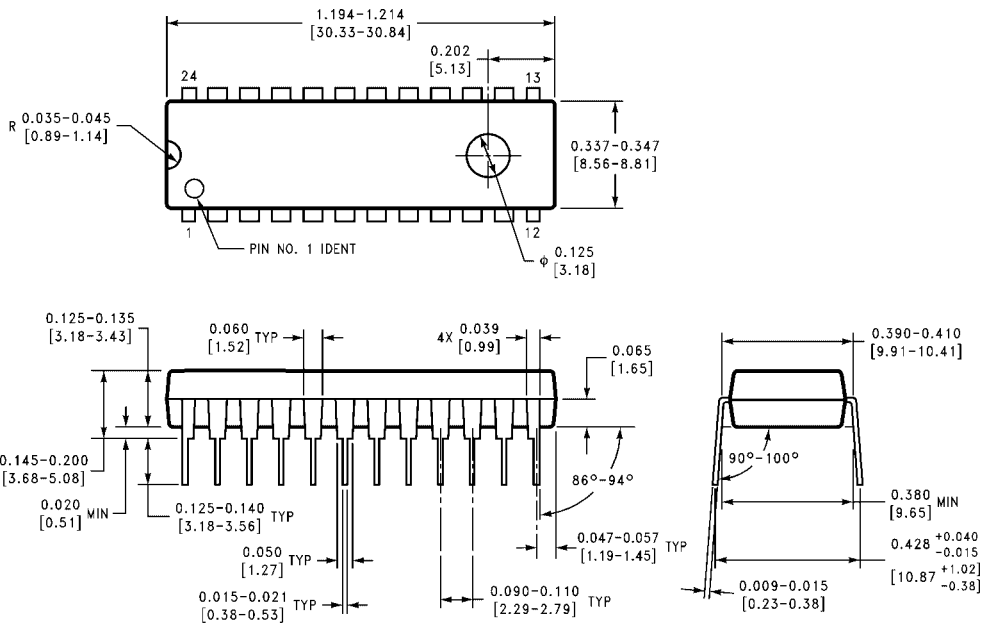
t_S is the minimum time before the transition of the clock that information must be present at the data input.

t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

Physical Dimensions inches (millimeters) unless otherwise noted

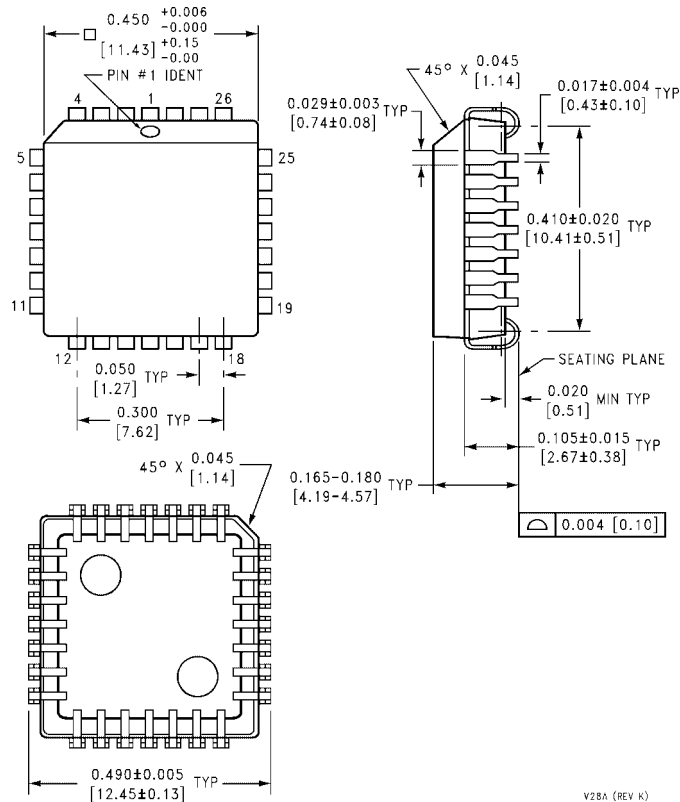


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

V28A (REV K)

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