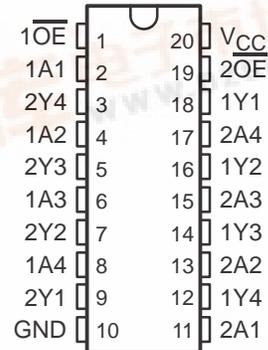


SN54ABT240 SN74ABT240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

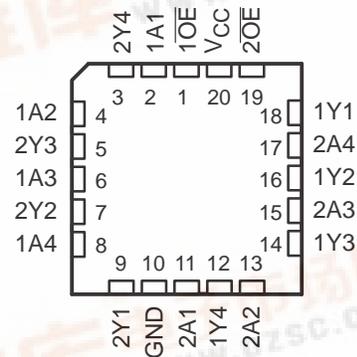
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- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

SN54ABT240 . . . J OR W PACKAGE
SN74ABT240A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT241, SN74ABT241A, SN54ABT244, and SN74ABT244A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs.

The SN54ABT240 and SN74ABT240A are organized as two 4-bit buffers/line drivers with separate \overline{OE} inputs. When \overline{OE} is low, the devices pass inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT240A is characterized for operation from -40°C to 85°C .

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54ABT240, SN74ABT240A

OCTAL BUFFERS/DRIVERS

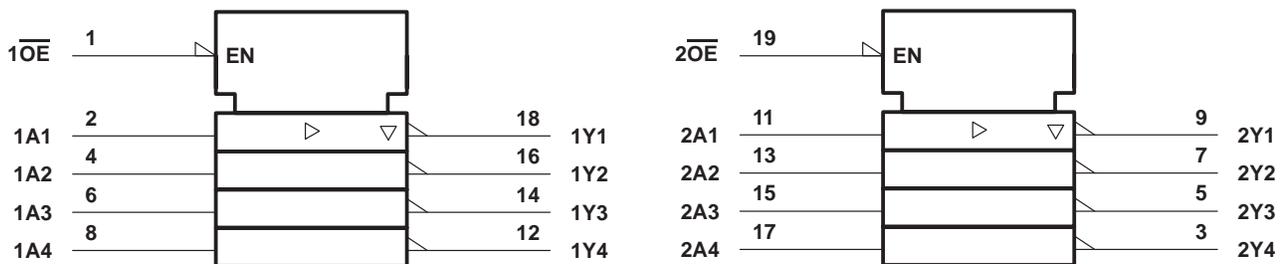
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

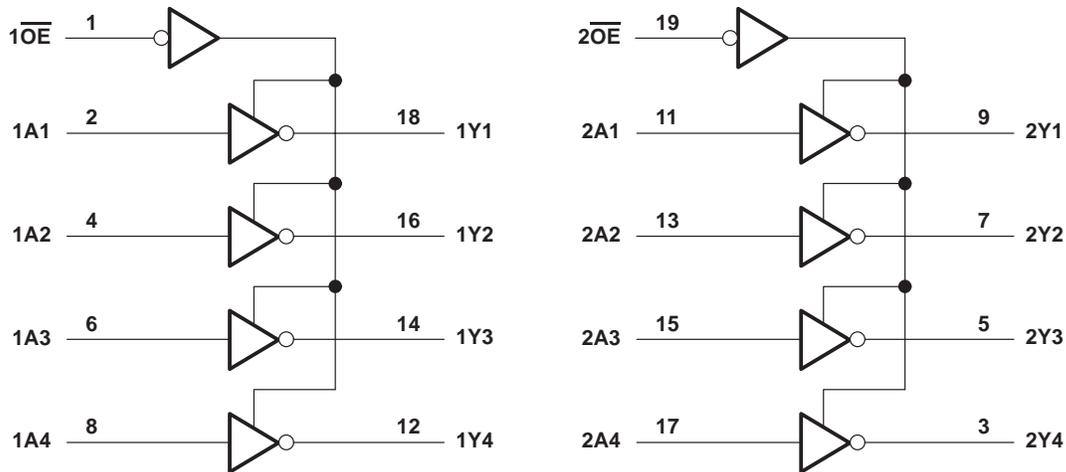
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54ABT240, SN74ABT240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT240	96 mA
SN74ABT240A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT240		SN74ABT240A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

SN54ABT240, SN74ABT240A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT240		SN74ABT240A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				
I _{OH} = -32 mA		2*					2			
V _{OL}	V _{CC} = 4.5 V		I _{OL} = 48 mA		0.55			0.55		V
			I _{OL} = 64 mA		0.55*			0.55		
V _{hys}			100							mV
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		µA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		10			10		10		µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V		-10			-10		-10		µA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		µA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high		50			50		µA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		1	250	250	250	250	µA
			Outputs low		24	30	30	30	30	mA
			Outputs disabled		0.5	250	250	250	250	µA
ΔI _{CC} §	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		Outputs enabled		1.5	1.5	1.5	mA	
				Outputs disabled		0.05	0.05	0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				1.5	1.5	1.5		
C _I	V _I = 2.5 V or 0.5 V		4							pF
C _O	V _O = 2.5 V or 0.5 V		7.5							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ABT240, SN74ABT240A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT240					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.9	4.3	0.8	5.5	ns
t_{PHL}			1.6	3.1	4.5	1	5.5	
t_{PZH}	\overline{OE}	Y	1.1	3.1	5.8	0.8	7.5	ns
t_{PZL}			1.1	2.7	6.2	0.8	7.7	
t_{PHZ}	\overline{OE}	Y	1.8	4.6	5.9	1.7	7	ns
t_{PLZ}			1.6	4	5.9	1.3	7.2	

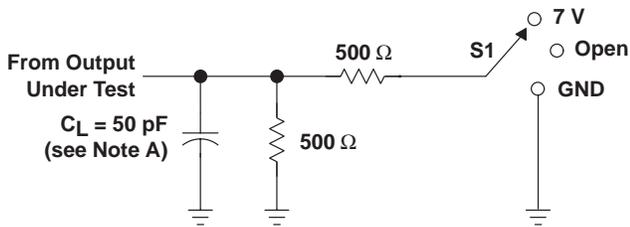
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT240A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.9	4.1	1	4.8	ns
t_{PHL}			1.6	3.1	4.6	1.6	4.8	
t_{PZH}	\overline{OE}	Y	1.1	3.1	4.7	1.1	5.2	ns
t_{PZL}			1.1	2.7	5.8	1.1	6.2	
t_{PHZ}	\overline{OE}	Y	1.8	4.6	5.7	1.8	6.4	ns
t_{PLZ}			1.6	4	5.4	1.6	5.8	

SN54ABT240, SN74ABT240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

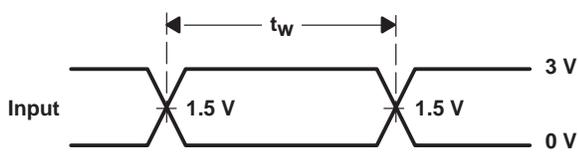
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PARAMETER MEASUREMENT INFORMATION

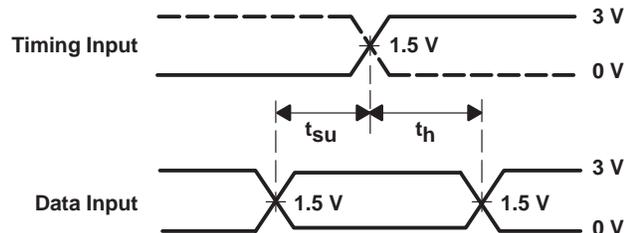


LOAD CIRCUIT

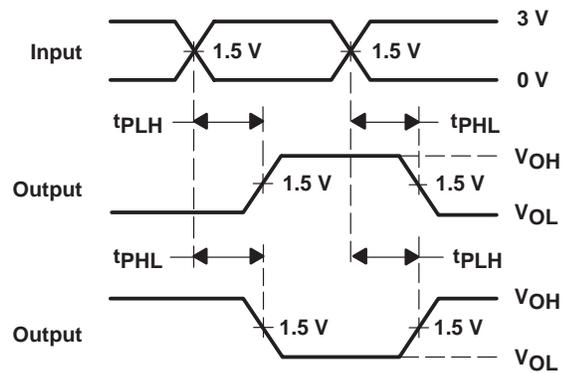
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



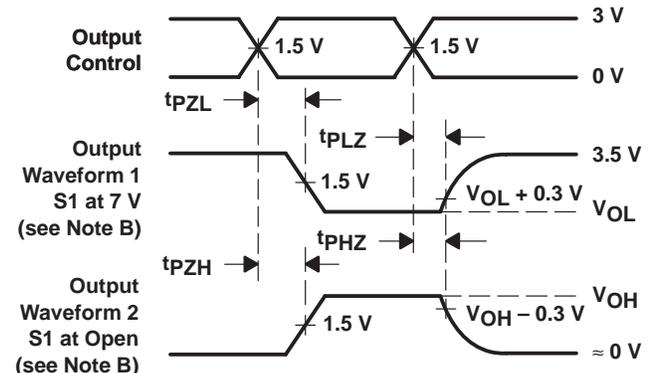
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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