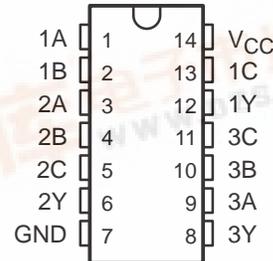


- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This triple 3-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC10A performs the Boolean function $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC10A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

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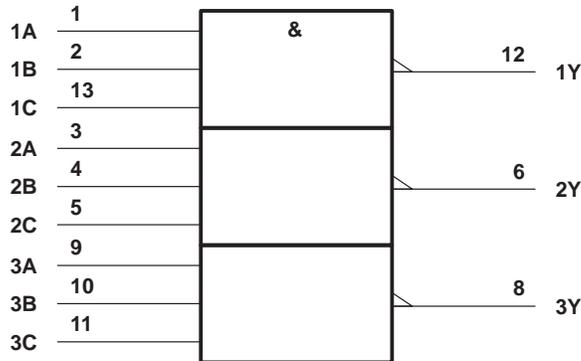
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

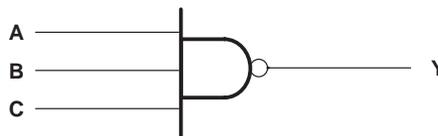
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 6.5 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 6.5 V |
| Output voltage range, V_O (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Continuous output current, I_O | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 127°C/W |
| DB package | 158°C/W |
| PW package | 170°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT | |
|-----------------|--------------------------------|------------------------------------|------------------------|------|----|
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | -4 | | mA |
| | | V _{CC} = 2.3 V | -8 | | |
| | | V _{CC} = 2.7 V | -12 | | |
| | | V _{CC} = 3 V | -24 | | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | | mA |
| | | V _{CC} = 2.3 V | 8 | | |
| | | V _{CC} = 2.7 V | 12 | | |
| | | V _{CC} = 3 V | 24 | | |
| T _A | Operating free-air temperature | -40 | 85 | °C | |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP† | MAX | UNIT |
|------------------|--|-----------------|----------------------|------|-----|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} -0.2 | | V | |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.7 | | | |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | 3 V | 2.2 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.2 | | V | |
| | I _{OL} = 4 mA | 1.65 V | 0.45 | | | |
| | I _{OL} = 8 mA | 2.3 V | 0.7 | | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±5 | | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 10 | | μA | |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | μA | |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | pF | |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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TRIPLE 3-INPUT POSITIVE-NAND GATE

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|---------------------------------|--------------|-------------|-------------------------|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 13.8 | 1 | 7.8 | 5.8 | | 1 | 4.9 | ns |
| t _{sk(o)} [†] | | | | | | | | 1 | | ns |

[†] Skew between any two outputs of the same package switching in the same direction

operating characteristics, T_A = 25°C

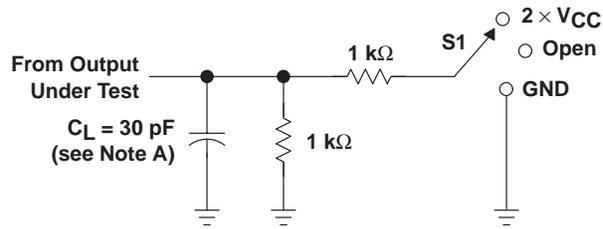
| PARAMETER | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|--|-----------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per gate | f = 10 MHz | 9 | 10 | 11 | pF |

SN74LVC10A TRIPLE 3-INPUT POSITIVE-NAND GATE

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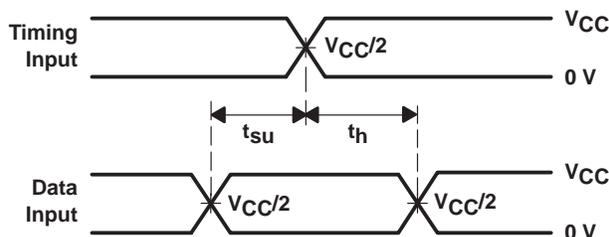
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

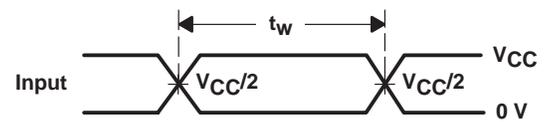


LOAD CIRCUIT

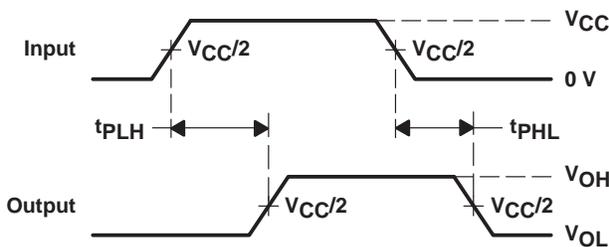
| TEST | S1 |
|-------------------|--------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZH} | 2 x V_{CC} |
| t_{PHZ}/t_{PHZ} | Open |



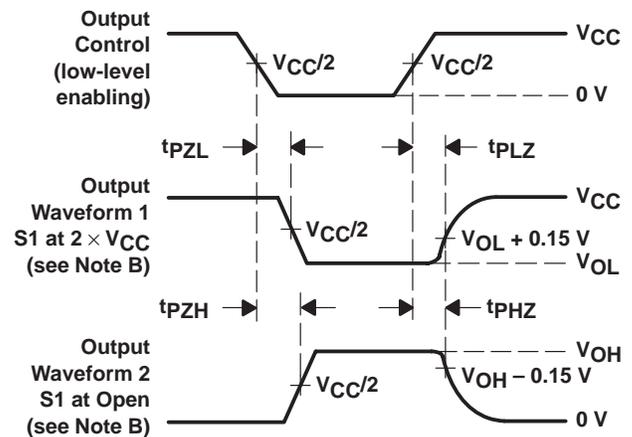
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

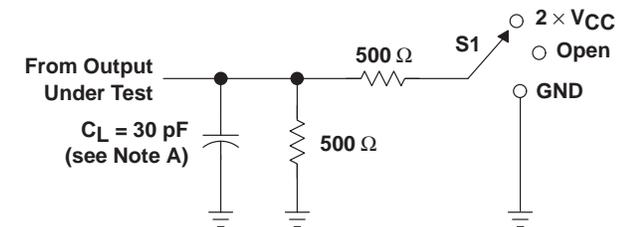
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC10A TRIPLE 3-INPUT POSITIVE-NAND GATE

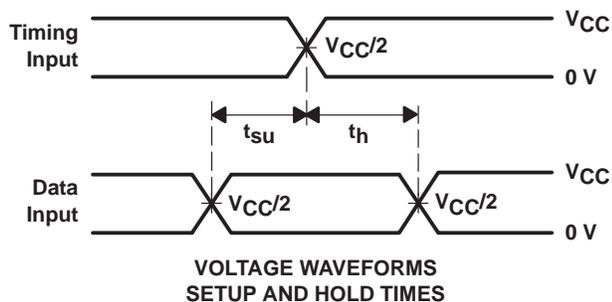
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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

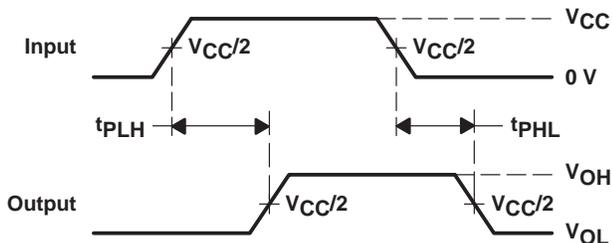


LOAD CIRCUIT

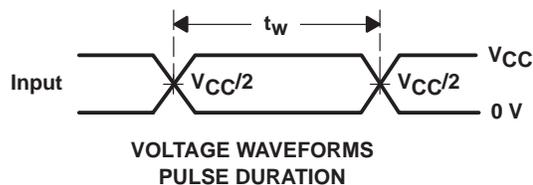
| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



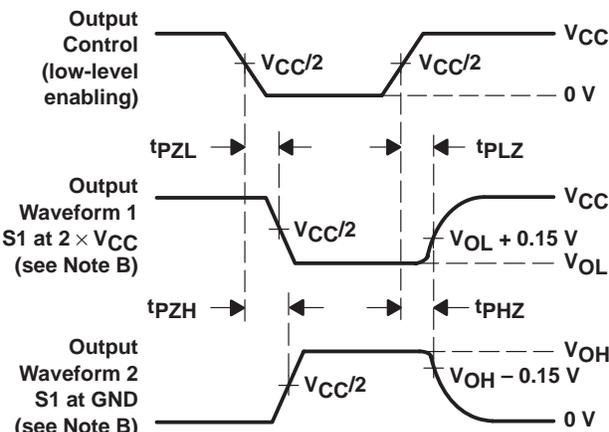
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

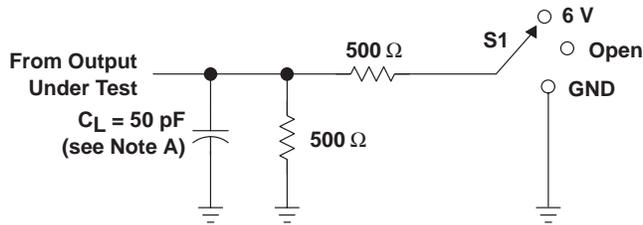
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVC10A TRIPLE 3-INPUT POSITIVE-NAND GATE

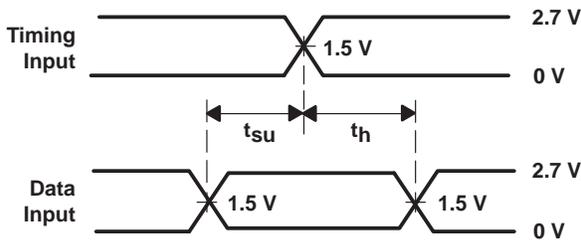
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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

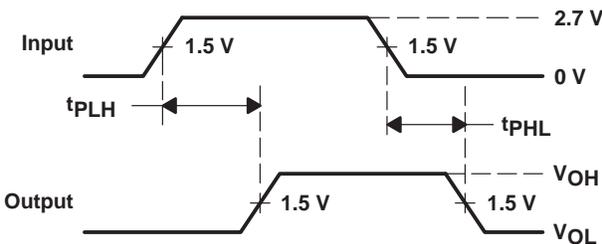


LOAD CIRCUIT

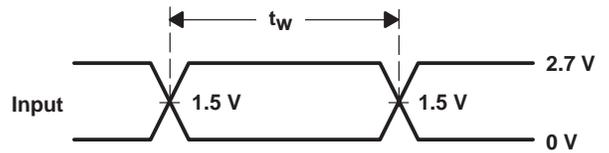
| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



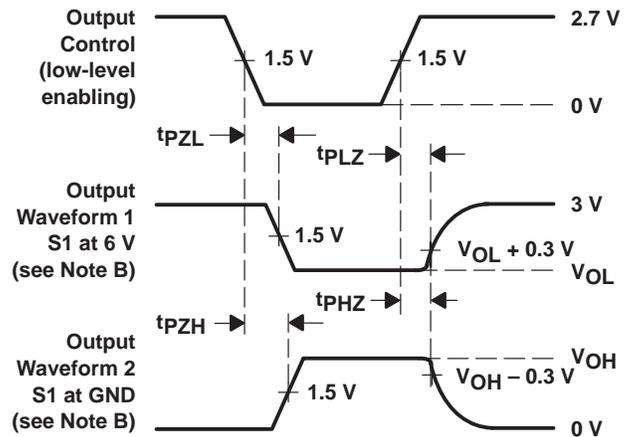
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
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 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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