捷多邦,专业PCB打样工厂,24小时加急**\$N74LVT240A**3.3-V ABT OCTAL BUFFER/DRIVER

SCBS134K - SEPTEMBER 1992 - REVISED JANUARY 2004

- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down To 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE (TOP VIEW)

1 2 3	20 19 18	V _{CC} 2OE 1Y1
 3 4 5 6		

description/ordering information

This octal buffer and line driver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT240A is organized as two 4-bit buffer/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using loff and power-up 3-state. The loff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0010 DW	Tube	SN74LVT240ADW	1)/T0404
	SOIC - DW	Tape and reel	SN74LVT240ADWR	LVT240A
	SOP – NS	Tape and reel	SN74LVT240ANSR	LVT240A
–40°C to 85°C	SSOP – DB	Tape and reel	SN74LVT240ADBR	LX240A
	TOOOD DW	Tube	SN74LVT240APW	1.70404
	TSSOP – PW	Tape and reel	SN74LVT240APWR	LX240A
100	TVSOP - DGV	Tape and reel	SN74LVT240ADGVR	LX240A

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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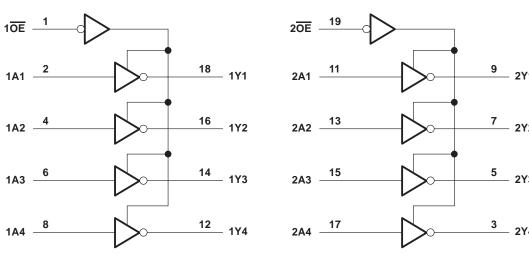


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FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
OE	Α	Υ
L	Н	L
L	L	Н
Н	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high	n-impedance	
or power-off state, VO (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high		
Current into any output in the low state, IO		128 mA
Current into any output in the high state, IO (see	ee Note 2)	64 mA
Input clamp current, I _{IK} (V _I < 0)		
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Package thermal impedance, θ _{JA} (see Note 3)): DB package	70°C/W
	DGV package	92°C/W
	DW package	
	NS package	
	PW package	83°C/W
Storage temperature range, T _{stg}	. •	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage				V
V _{IL}	Low-level input voltage				V
VI	Input voltage				V
ЮН	High-level output current				mA
loL	Low-level output current	_		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		μs/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT		
VIK	V _{CC} = 2.7 V,	I _I = -18 mA	$I_{I} = -18 \text{ mA}$			-1.2	V	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	I _{OH} = -100 μA		V _{CC} -0.2			V	
Vон	$V_{CC} = 2.7 \text{ V},$	IOH = -8 mA		2.4				
	V _{CC} = 3 V,	$I_{OH} = -32 \text{ mA}$		2				
	V 27V	I _{OL} = 100 μA				0.2		
	V _{CC} = 2.7 V	$I_{OL} = 24 \text{ mA}$				0.5		
V_{OL}		$I_{OL} = 16 \text{ mA}$				0.4	V	
	V _{CC} = 3 V	$I_{OL} = 32 \text{ mA}$				0.5		
		$I_{OL} = 64 \text{ mA}$				0.55	55	
	$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	V _I = 5.5 V				10		
1.		$V_I = V_{CC}$ or GND	Control inputs			±1	μА	
V _{CC} = 3.6 V	V _{CC} = 3.6 V	V _I = V _{CC}		1			μπ	
		V _I = 0	Data inputs			-5	5	
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V	V_I or $V_O = 0$ to 4.5 V			±100	μΑ	
IOZH	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				5	μΑ	
lozL	$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$				-5	μΑ	
lozpu	$V_{CC} = 0 \text{ to } 1.5 \text{ V},$	$V_0 = 0.5 V \text{ to } 3 V,$	OE = don't care			±100	μΑ	
I _{OZPD}	$V_{CC} = 1.5 \text{ V to } 0,$	$V_0 = 0.5 \text{ V to 3 V},$	OE = don't care			±100	μΑ	
			Outputs high	0.19		0.19		
ICC	$V_{CC} = 3.6 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0,$	Outputs low		5		mA	
AL = AGG OL GIAD		Outputs disabled				0.19	<u> </u>	
∆l _{CC} ‡	$V_{CC} = 3 \text{ V to } 3.6 \text{ V, One}$	input at V _{CC} - 0.6 V, Othe	er inputs at V _{CC} or GND			0.2	mA	
Ci	V _I = 3 V or 0	V _I = 3 V or 0			4		pF	
Co	V _O = 3 V or 0				7		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

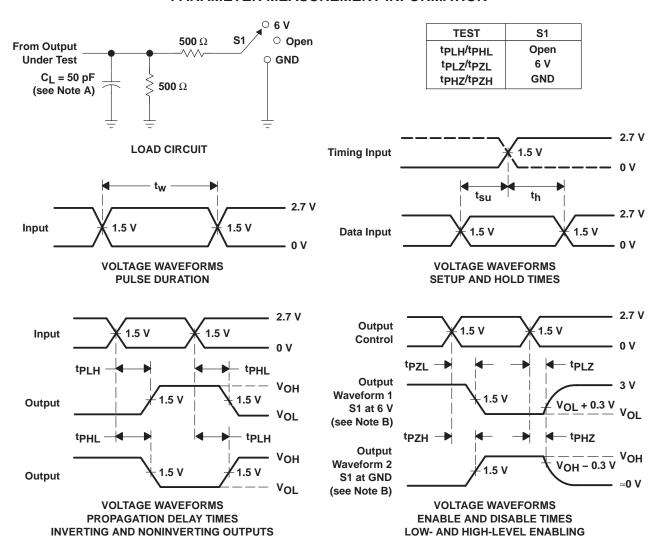
SN74LVT240A 3.3-V ABT OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS SCBS134K - SEPTEMBER 1992 - REVISED JANUARY 2004

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	VCC = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
	(INPUT)	(001P01)	MIN	TYP†	MAX	MIN	MAX	
^t PLH		V	1.1	2.2	3.8		4.6	
^t PHL	А	Y	1.3	2.6	4		4.2	ns
^t PZH		V	1.1	2.6	4.6		5.6	
^t PZL	ŌĒ	Y	1.4	2.7	4.4		5	ns
^t PHZ	ŌĒ	V	2	2.9	4.4		4.6	
t _{PLZ}	OE OE	Y	1.8	3	4.3		4.3	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







com 13-Sep-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVT240ADBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT240APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): Ti's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

13-Sep-2005

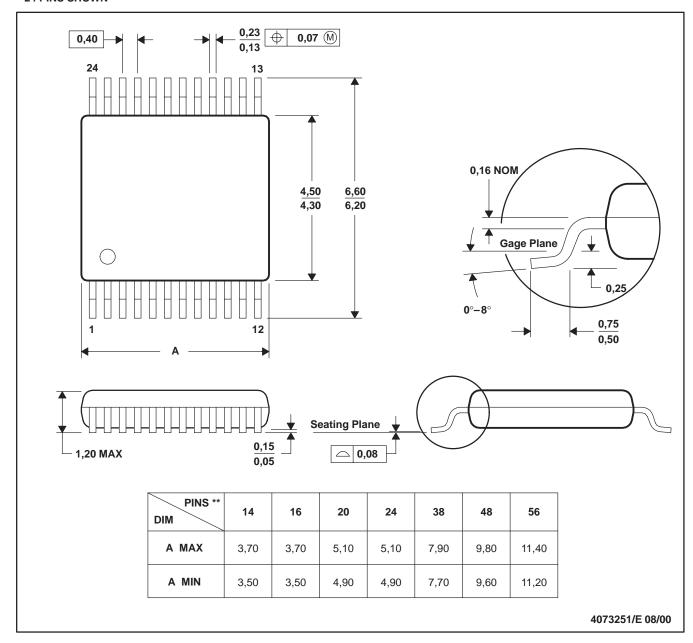
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DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



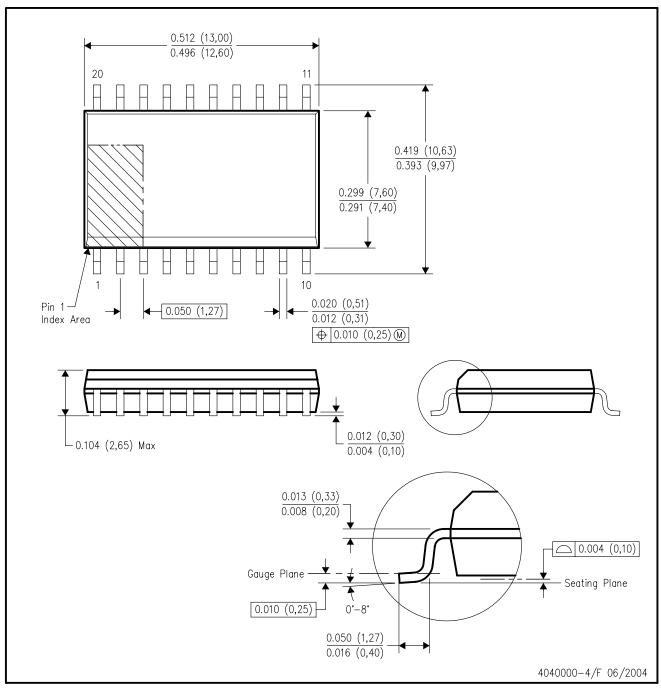
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153 14/16/20/56 Pins – MO-194



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- . All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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