



IEEE 802.3af PD Interface Controller For Power-Over-Ethernet

MAX5940A/MAX5940B

General Description

The MAX5940A/MAX5940B provide complete interface function for a powered device (PD) to comply with the IEEE 802.3af standard in a power-over-ethernet system. MAX5940A/MAX5940B provide the PD with a detection signature, a classification signature, and an integrated isolation switch with programmable inrush current control. These devices also feature power-mode undervoltage lockout (UVLO) with wide hysteresis, and power-good outputs.

An integrated MOSFET provides PD isolation during detection and classification. The MAX5940A/MAX5940B guarantee a leakage current offset of less than 10 μ A during the detection phase. A programmable current limit prevents high inrush current during power-on. The device features power-mode UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition between detection, classification, and power-on/off phases.

The MAX5940A provides an active-high (PGOOD) open-drain output and a fixed UVLO threshold. The MAX5940B provides both active-high (PGOOD) and active-low ($\overline{\text{PGOOD}}$) outputs and has an adjustable UVLO threshold with the default value compliant to the 802.3af standard. The MAX5940A/MAX5940B are designed to work with or without an external diode bridge.

The MAX5940A/MAX5940B are available in 8-pin SO packages and are rated over the extended temperature range of -40°C to +85°C.

Applications

- IP Phones
- Security Cameras
- Wireless Access Nodes
- IEEE 802.3af Power Devices
- Computer Telephony

Features

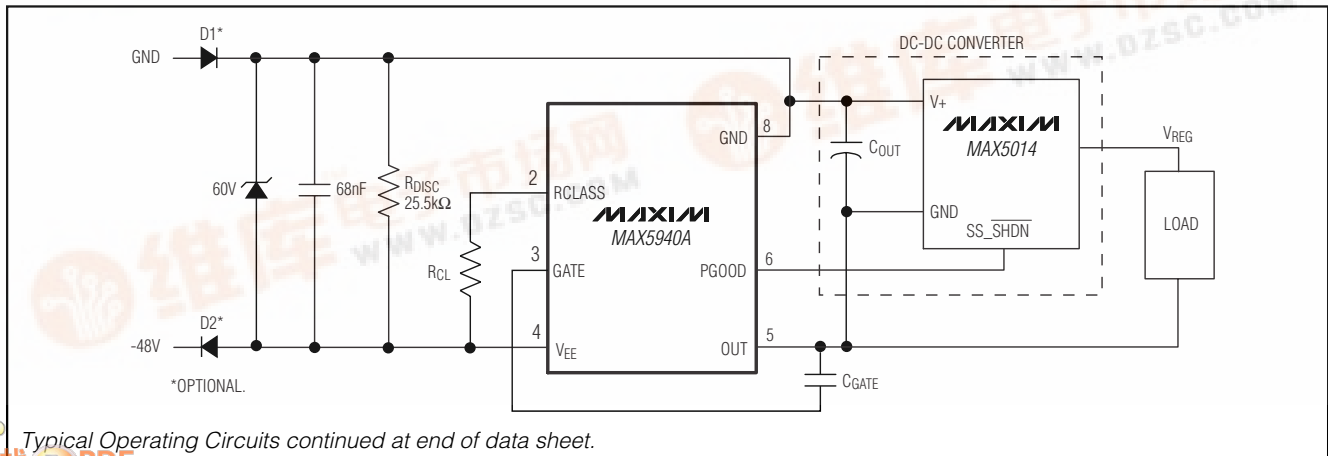
- ◆ Fully Integrated IEEE 802.3af-Compliant PD Interface
- ◆ PD Detection and Programmable Classification Signatures
- ◆ Less than 10 μ A Leakage Current Offset During Detection
- ◆ Integrated MOSFET For Isolation and Inrush Current Limiting
- ◆ Gate Output Allows External Control of the Internal Isolation MOSFET
- ◆ Programmable Inrush Current Control
- ◆ Programmable Undervoltage Lockout (MAX5940B Only)
- ◆ Wide UVLO Hysteresis Accommodates Twisted-Pair Cable Voltage Drop
- ◆ PGOOD/ $\overline{\text{PGOOD}}$ Outputs to Enable Downstream DC-DC Converters
- ◆ -40°C to +85°C Operating Temperature Range

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | UVLO |
|-------------|----------------|-------------|------------|
| MAX5940AESA | -40°C to +85°C | 8 SO | Fixed |
| MAX5940BESA | -40°C to +85°C | 8 SO | Adjustable |

Pin Configurations appear at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to V_{EE} , unless otherwise noted.)

| | |
|---|-----------------------|
| GND | -0.3V to +80V |
| OUT, $\overline{\text{PGOOD}}$ | -0.3V to (GND + 0.3V) |
| RCLASS, GATE | -0.3V to +12V |
| UVLO | -0.3V to +8V |
| PGOOD to OUT | -0.3V to (GND + 0.3V) |
| Maximum Input/Output Current (continuous) | |
| OUT to V_{EE} | 500mA |
| GND, RCLASS to V_{EE} | 70mA |

| | |
|--|---|
| UVLO, $\overline{\text{PGOOD}}$, PGOOD to V_{EE} | 20mA |
| GATE to V_{EE} | 80mA |
| Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) | |
| 8-Pin SO (derate 5.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) | 470mW |
| Operating Temperature Range | -40°C to $+85^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature | $+150^\circ\text{C}$ |
| Lead Temperature (soldering, 10s) | $+300^\circ\text{C}$ |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = (\text{GND} - V_{EE}) = 48\text{V}$, GATE = $\overline{\text{PGOOD}}$ = PGOOD = OUT = OPEN, UVLO = V_{EE} , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$. All voltages are referenced to V_{EE} , unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|-------------------------|--|---|-------|-------|------------------|---|
| DETECTION MODE | | | | | | | |
| Input Offset Current (Note 2) | I_{OFFSET} | $V_{IN} = 1.4\text{V}$ to 10.1V | | | 10 | μA | |
| Effective Differential Input Resistance (Note 3) | dR | $V_{IN} = 1.4\text{V}$ up to 10.1V with 1V step, OUT = PGOOD = GND | 550 | | | $\text{k}\Omega$ | |
| CLASSIFICATION MODE | | | | | | | |
| Classification Current Turn-Off Threshold (Note 4) | $V_{\text{TH,CLSS}}$ | V_{IN} rising | 20.8 | 21.8 | 22.5 | V | |
| Classification Current (Notes 5, 6) | I_{CLASS} | $V_{IN} = 12.6\text{V}$ to 20V , $R_{\text{DISC}} = 25.5\text{k}\Omega$ | Class 0, $R_{\text{CL}} = 10\text{k}\Omega$ | 0 | 2 | mA | |
| | | | Class 1, $R_{\text{CL}} = 732\Omega$ | 9.17 | 11.83 | | |
| | | | Class 2, $R_{\text{CL}} = 392\Omega$ | 17.29 | 19.71 | | |
| | | | Class 3, $R_{\text{CL}} = 255\Omega$ | 26.45 | 29.55 | | |
| | | | Class 4, $R_{\text{CL}} = 178\Omega$ | 36.6 | 41.4 | | |
| POWER MODE | | | | | | | |
| Operating Supply Voltage | V_{IN} | $V_{IN} = (\text{GND} - V_{EE})$ | | | 67 | V | |
| Operating Supply Current | I_{IN} | Measure at GND, not including R_{DISC} | | 0.4 | 1 | mA | |
| Default Power Turn-On Voltage | $V_{\text{UVLO, ON}}$ | V_{IN} increasing | MAX5940A | 34.3 | 35.4 | 36.6 | V |
| | | | MAX5940B, UVLO = V_{EE} | 37.4 | 38.6 | 39.9 | |
| Default Power Turn-Off Voltage | $V_{\text{UVLO, OFF}}$ | V_{IN} decreasing, UVLO = V_{EE} for MAX5940B | 30 | | | V | |
| Default Power Turn-On/Off Hysteresis | $V_{\text{HYST, UVLO}}$ | MAX5940A | 4.2 | | | V | |
| | | MAX5940B, UVLO = V_{EE} | 7.4 | | | | |
| External UVLO Programming Range | $V_{\text{IN, EX}}$ | Set UVLO externally (MAX5940B only) (Note 7) | 12 | | 67 | V | |
| UVLO External Reference Voltage | $V_{\text{REF, UVLO}}$ | | 2.400 | 2.460 | 2.522 | V | |
| UVLO External Reference Voltage Hysteresis | HYST | Ratio to $V_{\text{REF, UVLO}}$ | 19.2 | 20 | 20.9 | % | |
| UVLO Bias Current | I_{UVLO} | UVLO = 2.460V | -1.5 | | +1.5 | μA | |

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MAX5940A/MAX5940B

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = (GND - V_{EE}) = 48V$, $GATE = \overline{PGOOD} = PGOOD = OUT = OPEN$, $UVLO = V_{EE}$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$. All voltages are referenced to V_{EE} , unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|-----------------|---|--------------------------------|------|------|----------|----------|
| UVLO Input Ground-Sense Threshold (Note 8) | $V_{TH,G,UVLO}$ | | 50 | | 440 | mV | |
| UVLO Input Ground-Sense Glitch Rejection | | $UVLO = V_{EE}$ | | 7 | | μs | |
| Power Turn-Off Voltage, Undervoltage Lockout Deglitch Time (Note 9) | t_{OFF_DLY} | V_{IN} , V_{UVLO} falling | 0.32 | | | ms | |
| Isolation Switch N-Channel MOSFET On-Resistance | R_{ON} | Output current = 300mA, $V_{GATE} = 6V$, measured between OUT and V_{EE} | $T_A = +25^{\circ}C$ (Note 10) | | 0.6 | 1.1 | Ω |
| | | | $T_A = +85^{\circ}C$ | | 0.8 | 1.5 | |
| Isolation Switch N-Channel MOSFET Off-Threshold Voltage | V_{GSTH} | $OUT = GND$, $V_{GATE} - V_{EE}$, output current < $1\mu A$ | 0.5 | | | V | |
| GATE Pulldown Switch Resistance | R_G | Power-off mode, $V_{IN} = 12V$, $UVLO = V_{EE}$ for MAX5940B | | 38 | 80 | Ω | |
| GATE Charging Current | I_G | $V_{GATE} = 2V$ | 5 | 10 | 15 | μA | |
| GATE High Voltage | V_{GATE} | $I_{GATE} = 1\mu A$ | 5.59 | 5.76 | 5.93 | V | |
| PGOOD, \overline{PGOOD} Assertion V_{OUT} Threshold | V_{OUTEN} | $V_{OUT} - V_{EE}$, $I_{V_{OUT}} - V_{EE}$ decreasing, $V_{GATE} = 5.75V$ | 1.16 | 1.23 | 1.31 | V | |
| | | Hysteresis | | 70 | | mV | |
| PGOOD, \overline{PGOOD} Assertion V_{GATE} Threshold | V_{GSEN} | $(GATE - V_{EE})$ increasing, $OUT = V_{EE}$ | 4.62 | 4.76 | 4.91 | V | |
| | | Hysteresis | | 80 | | mV | |
| PGOOD, \overline{PGOOD} Output Low Voltage (Note 11) | $V_{OLDCCDC}$ | $I_{SINK} = 2mA$; for PGOOD, $OUT \leq (GND - 5V)$ | | | 0.4 | V | |
| PGOOD Leakage Current (Note 11) | | $GATE = high$, $GND - V_{OUT} = 67V$ | | | 1 | μA | |
| \overline{PGOOD} Leakage Current (Note 11) | | $GATE = V_{EE}$, $\overline{PGOOD} - V_{EE} = 67V$ | | | 1 | μA | |

Note 1: All min/max limits are production tested at $+85^{\circ}C$. Limits at $+25^{\circ}C$ and $-40^{\circ}C$ are guaranteed by design.

Note 2: The input offset current is illustrated in Figure 1.

Note 3: Effective differential input resistance is defined as the differential resistance between GND and V_{EE} without any external resistance. See Figure 1.

Note 4: Classification current is turned off whenever the IC is in power mode.

Note 5: See Table 2 in the *PD Classification Mode* section. R_{DISC} and R_{CL} must be $\pm 1\%$, 100ppm or better. I_{CLASS} includes the IC bias current and the current drawn by R_{DISC} .

Note 6: See the *Thermal Dissipation* section for details.

Note 7: When UVLO is connected to the midpoint of an external resistor-divider with a series resistance of $25.5k\Omega$ ($\pm 1\%$), the turn-on threshold set-point for the power mode is defined by the external resistor-divider. Make sure the voltage on the UVLO pin does not exceed its maximum rating of 8V when V_{IN} is at the maximum voltage (MAX5940B only).

Note 8: When the UVLO input voltage is below $V_{TH,G,UVLO}$, the MAX5940B sets the UVLO threshold internally.

Note 9: An input voltage or V_{UVLO} glitch below their respective thresholds shorter than or equal to t_{OFF_DLY} does not cause the MAX5940A/MAX5940B to exit power-on mode (as long as the input voltage remains above an operable voltage level of 12V).

Note 10: Guaranteed by design.

Note 11: PGOOD references to OUT while \overline{PGOOD} references to V_{EE} .

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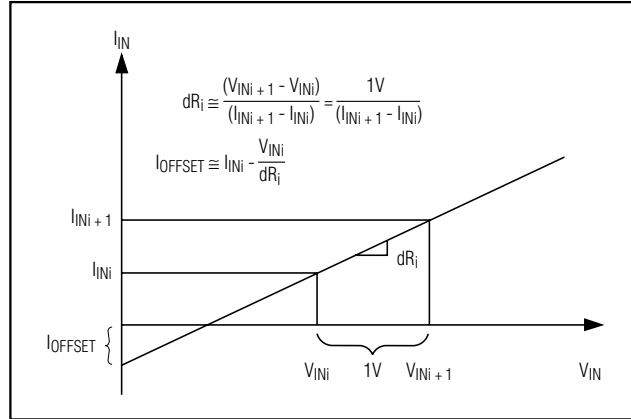
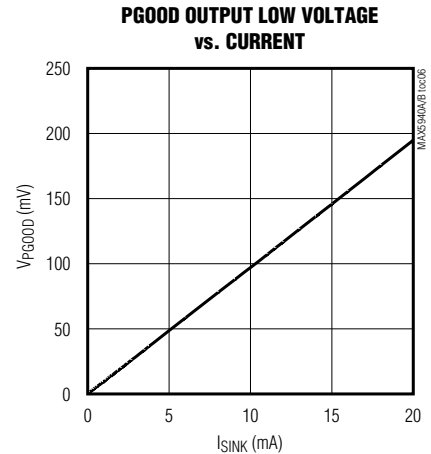
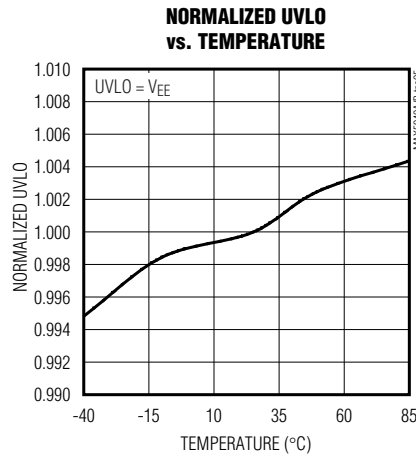
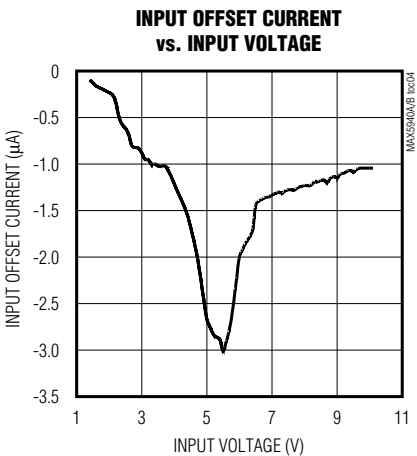
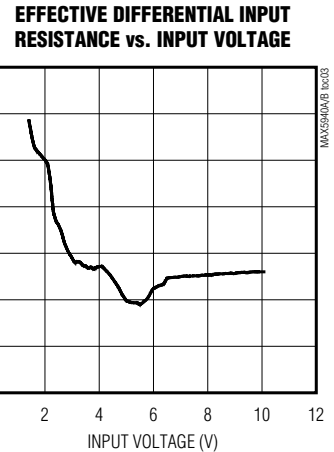
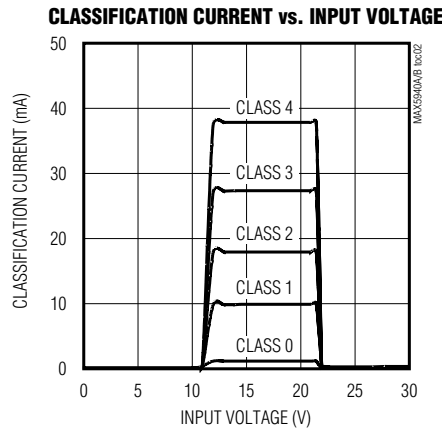
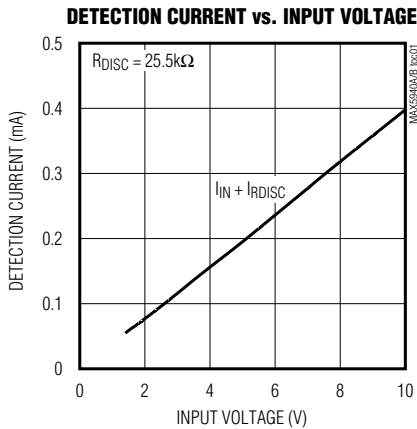


Figure 1. Effective Differential Input Resistance/Offset Current

Typical Operating Characteristics

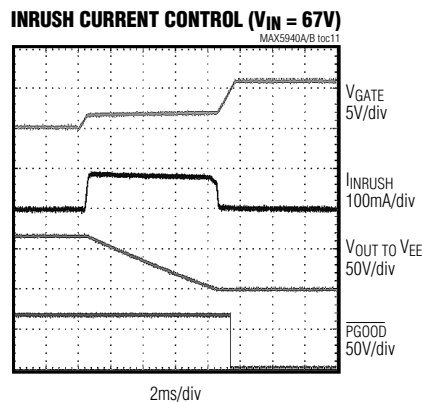
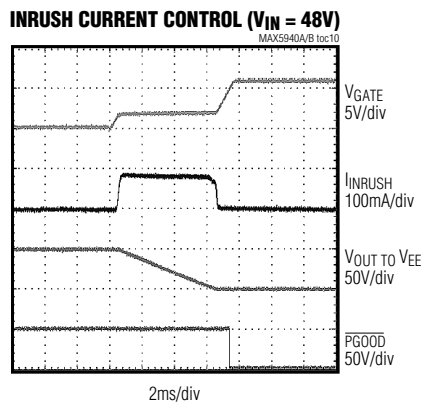
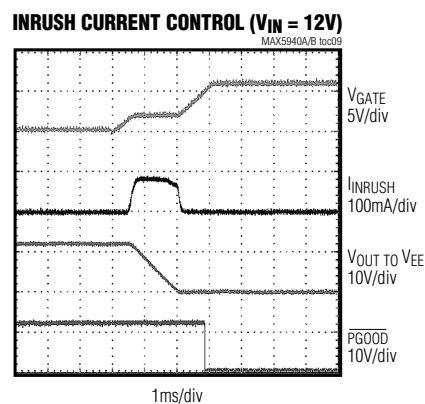
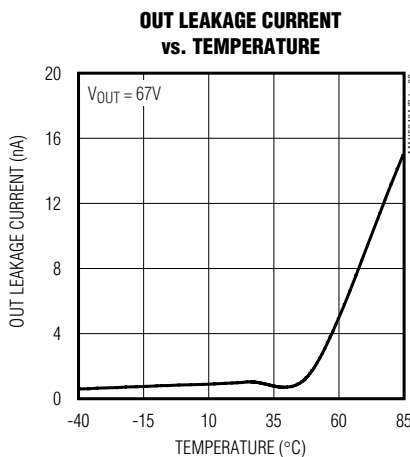
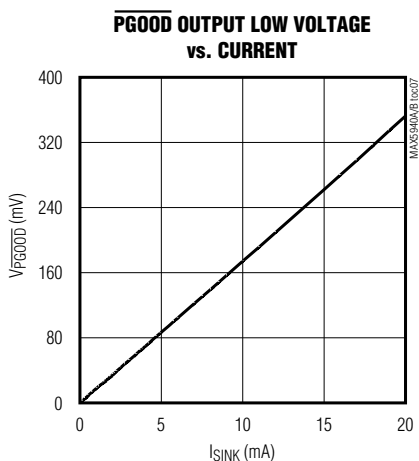
($V_{IN} = (GND - V_{EE}) = 48V$, GATE = \overline{PGOOD} = PGOOD = OUT = OPEN, UVLO = V_{EE} (MAX5940B), $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $T_A = +25^{\circ}C$. All voltages are referenced to V_{EE} , unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{IN} = (GND - V_{EE}) = 48V$, $GATE = \overline{PGOOD} = PGOOD = OUT = OPEN$, $UVLO = V_{EE}$ (MAX5940B), $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $T_A = +25^{\circ}C$. All voltages are referenced to V_{EE} , unless otherwise noted.)



MAX5940A/MAX5940B

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Pin Description

| PIN | | NAME | FUNCTION |
|----------|----------|--------------------|--|
| MAX5940A | MAX5940B | | |
| 1, 7 | — | N.C. | No Connection. Not internally connected. |
| — | 1 | UVLO | Undervoltage Lockout Programming Input for Power Mode. When UVLO is above its threshold, the device enters power mode. Connect UVLO to V_{EE} to use the default undervoltage lockout threshold. Connect UVLO to an external resistor-divider to define a threshold externally. The series resistance value of the external resistors must add to $25.5k\Omega$ ($\pm 1\%$) and replaces the detection resistor. To keep the device in undervoltage lockout, pull UVLO to between $V_{TH,G,UVLO}$ and $V_{REF,UVLO}$. |
| 2 | 2 | RCLASS | Classification Setting. Add a resistor from RCLASS to V_{EE} to set a PD class (see Tables 1 and 2). |
| 3 | 3 | GATE | Gate of Internal N-Channel Power MOSFET. GATE sources $10\mu A$ when the device enters power mode. Connect an external $100V$ ceramic capacitor (C_{GATE}) from GATE to OUT to program the inrush current. Pull GATE to V_{EE} to turn off the internal MOSFET. The detection and classification functions operate normally when GATE is pulled to V_{EE} . |
| 4 | 4 | V_{EE} | Negative Input Power. Source of the integrated isolation N-channel power MOSFET. Connect V_{EE} to $-48V$. |
| 5 | 5 | OUT | Output Voltage. Drain of the integrated isolation N-channel power MOSFET. |
| 6 | 6 | PGOOD | Power-Good Indicator Output, Active-High, Open-Drain. PGOOD is referenced to OUT. PGOOD goes high impedance when V_{OUT} is within $1.2V$ of V_{EE} and when GATE is $5V$ above V_{EE} . Otherwise, PGOOD is pulled to OUT (given that V_{OUT} is at least $5V$ below GND). Connect PGOOD to the ON pin of a downstream DC-DC converter. |
| — | 7 | \overline{PGOOD} | Power-Good Indicator Output, Active-Low, Open-Drain. \overline{PGOOD} is referenced to V_{EE} . \overline{PGOOD} is pulled to V_{EE} when V_{OUT} is within $1.2V$ of V_{EE} and when GATE is $5V$ above V_{EE} . Otherwise, \overline{PGOOD} goes high impedance. Connect \overline{PGOOD} to the ON pin of a downstream DC-DC converter. |
| 8 | 8 | GND | Ground. GND is the positive input terminal. |

Detailed Description

Operating Modes

The PD front-end section of the MAX5940A/MAX5940B operates in 3 different modes, PD detection signature, PD classification, and PD power, depending on its input voltage ($V_{IN} = GND - V_{EE}$). All voltage thresholds are designed to operate with or without the optional diode bridge while still complying with the IEEE 802.3af standard (see Figure 4).

Detection Mode ($1.4V \leq V_{IN} \leq 10.1V$)

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the range of $1.4V$ to $10.1V$ ($1V$ step minimum), and then records the current measurements at the two points. The PSE then computes $\Delta V/\Delta I$ to ensure the presence of the $25.5k\Omega$ signature resistor. In this mode, most of the MAX5940A/

MAX5940B internal circuitry is off and the offset current is less than $10\mu A$.

If the voltage applied to the PD is reversed, install protection diodes on the input terminal to prevent internal damage to the MAX5940A/MAX5940B (see the *Typical Application Circuits*). Since the PSE uses a slope technique ($\Delta V/\Delta I$) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode ($12.6V \leq V_{IN} \leq 20V$)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. The IEEE 802.3af standard defines five different classes as shown in Table 1. An external resistor (R_{CL}) connected from RCLASS to V_{EE} sets the classification current.

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Table 1. PD Power Classification/R_{CL} Selection

| CLASS | USAGE | R _{CL} (Ω) | MAXIMUM POWER USED BY PD (W) |
|-------|-------------|---------------------|------------------------------|
| 0 | Default | 10k | 0.44 to 12.95 |
| 1 | Optional | 732 | 0.44 to 3.84 |
| 2 | Optional | 392 | 3.84 to 6.49 |
| 3 | Optional | 255 | 6.49 to 12.95 |
| 4 | Not Allowed | 178 | Reserved* |

*Class 4 reserved for future use.

Table 2. Setting Classification Current

| CLASS | R _{CL} (Ω) | V _{IN} * (V) | CLASS CURRENT SEEN AT V _{IN} (mA) | | IEEE 802.3af PD CLASSIFICATION CURRENT SPECIFICATION (mA) | |
|-------|---------------------|-----------------------|--|-------|---|-----|
| | | | MIN | MAX | MIIN | MAX |
| 0 | 10k | 12.6 to 20 | 0 | 2 | 0 | 4 |
| 1 | 732 | 12.6 to 20 | 9.17 | 11.83 | 9 | 12 |
| 2 | 392 | 12.6 to 20 | 17.29 | 19.71 | 17 | 20 |
| 3 | 255 | 12.6 to 20 | 26.45 | 29.55 | 26 | 30 |
| 4 | 178 | 12.6 to 20 | 36.6 | 41.4 | 36 | 44 |

*V_{IN} is measured across the MAX5940 input pins, which does not include the diode bridge voltage drop.

The PSE determines the class of a PD by applying a voltage at the PD input and measures the current sourced out of the PSE. When the PSE applies a voltage between 12.6V and 20V, the MAX5940A/MAX5940B exhibit a current characteristic with values indicated in Table 2. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by the 25.5kΩ detection signature resistor and the supply current of the MAX5940A/MAX5940B so the total current drawn by the PD is within the IEEE 802.3af standard figures. The classification current is turned off whenever the device is in power mode.

Power Mode

During power mode, when V_{IN} rises above the undervoltage lockout threshold (V_{UVLO,ON}), the MAX5940A/MAX5940B gradually turn on the internal N-channel MOSFET Q1 (see Figure 2). The MAX5940A/MAX5940B charge the gate of Q1 with a constant current source (10μA, typ). The drain-to-gate capacitance of Q1 limits the voltage rise rate at the drain of the MOSFET, thereby

limiting the inrush current. To reduce the inrush current, add external drain-to-gate capacitance (see the *Inrush Current* section). When the drain of Q1 is within 1.2V of its source voltage and its gate-to-source voltage is above 5V, the MAX5940A/MAX5940B asserts the PGOOD/PGOOD outputs. The MAX5940A/MAX5940B have a wide UVLO hysteresis and turn-off deglitch time to compensate for the high impedance of the twisted-pair cable.

Undervoltage Lockout

The MAX5940A/MAX5940B operate up to a 67V supply voltage with a default UVLO turn-on (V_{UVLO,ON}) set at 35V (MAX5940A) or 39V (MAX5940B) and a UVLO turn-off (V_{UVLO,OFF}) set at 30V. The MAX5940B has an adjustable UVLO threshold using a resistor-divider connected to UVLO (see Figure 3). When the input voltage is above the UVLO threshold, the IC is in power mode and the MOSFET is on. When the input voltage goes below the UVLO threshold for more than t_{OFF_DLY}, the MOSFET turns off.

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Inrush Current Limit

The MAX5940A/MAX5940B charge the gate of the internal MOSFET with a constant current source (10 μ A, typ). The drain-to-gate capacitance of the MOSFET limits the voltage rise rate at the drain, thereby limiting the inrush current. Add an external capacitor from GATE to OUT to further reduce the inrush current. Use the following equation to calculate the inrush current:

$$I_{\text{INRUSH}} = I_G \times \frac{C_{\text{OUT}}}{C_{\text{GATE}}}$$

PGOOD/PGOOD Outputs

(MAX5940A/MAX5940B)

PGOOD is an open-drain, active-high logic output. PGOOD goes high impedance when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, PGOOD is pulled to V_{OUT} (given that V_{OUT} is at least 5V below GND). Connect PGOOD to the ON pin of a downstream DC-DC converter. Connect a 100k Ω pullup resistor from PGOOD to GND if needed.

(MAX5940B only)

PGOOD is an open-drain, active-low logic output. PGOOD is pulled to V_{EE} when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, PGOOD goes high impedance. Connect PGOOD to the ON pin of a downstream DC-DC converter. Connect a 100k Ω pullup resistor from PGOOD to GND if needed.

Thermal Dissipation

During classification mode, if the PSE applies the maximum DC voltage, the maximum voltage drop from GND to V_{RCLASS} will be 13V. If the maximum classification current of 42mA flows through the MAX5940A/MAX5940B, then the maximum DC power dissipation will be 546mW, which is slightly higher than the maximum DC power dissipation of the IC at maximum operating temperature. However, according to the IEEE 802.3af standard, the duration of the classification mode is limited to 75ms (max). The MAX5940A/MAX5940B handle the maximum classification power dissipation for the maximum duration time without sustaining any internal damage. If the PSE violates the IEEE 802.3af standard by exceeding the 75ms maximum classification duration, it may cause internal damage to the IC.

MAX5940A/MAX5940B

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Typical Application Circuits

Application Circuit 1

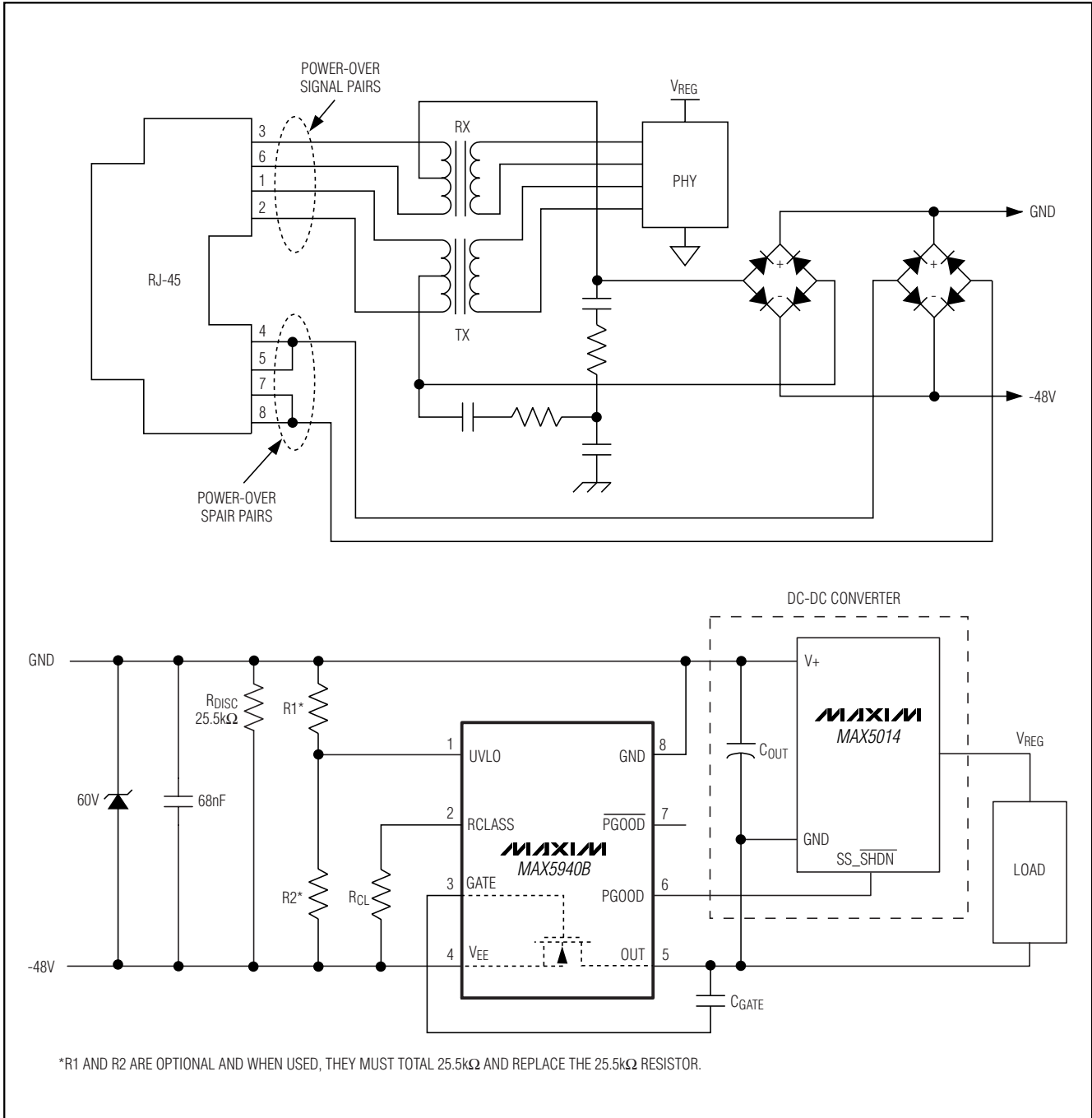


Figure 4. PD with Power-Over-Ethernet (Power is Provided by Either the Signal Pairs or the Spare Pairs)

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Typical Application Circuits (continued)

Application Circuit 2

Diode D1 prevents the power-over-ethernet to back drive the wall adapter. Whenever the wall adapter power is available, the GATE is pulled low to pinch off

the power-over-ethernet. R3 provides the GATE current flow path. The wall adapter power pollutes the discovery signature, preventing PSE from detecting this PD.

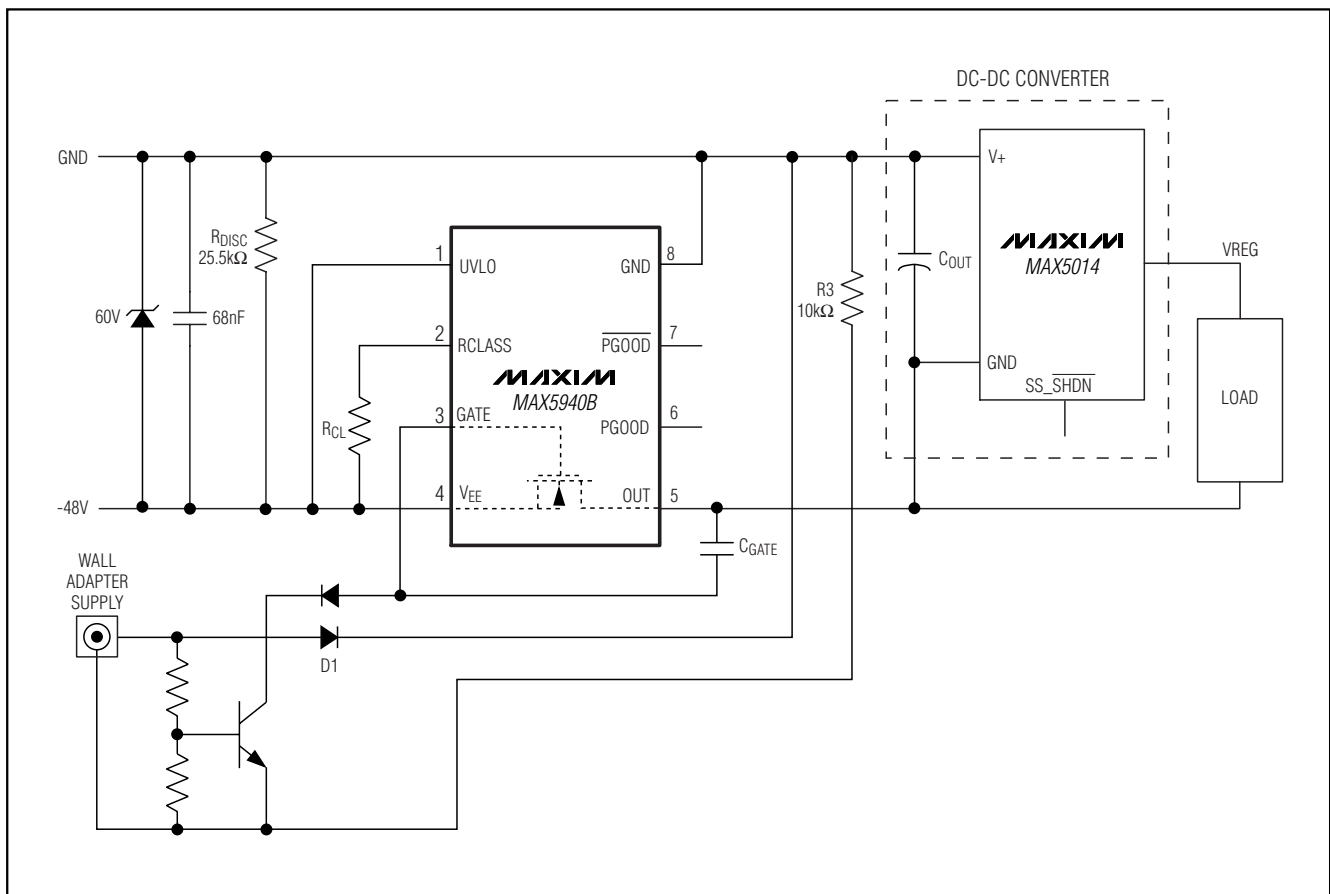


Figure 5. Adding Wall Adapter Input Supply (Wall Adapter Supply Takes Precedence Over Power-Over-Ethernet)

MAX5940A/MAX5940B

IEEE 802.3af PD Interface Controller For Power-Over-Ethernet

Typical Application Circuits (continued)

Application Circuit 3

D2 prevents the wall adapter power from polluting the discovery and classification signatures. The optional

R4 provides the 10mA minimum power maintenance signature to keep the power-over-ethernet from disconnecting.

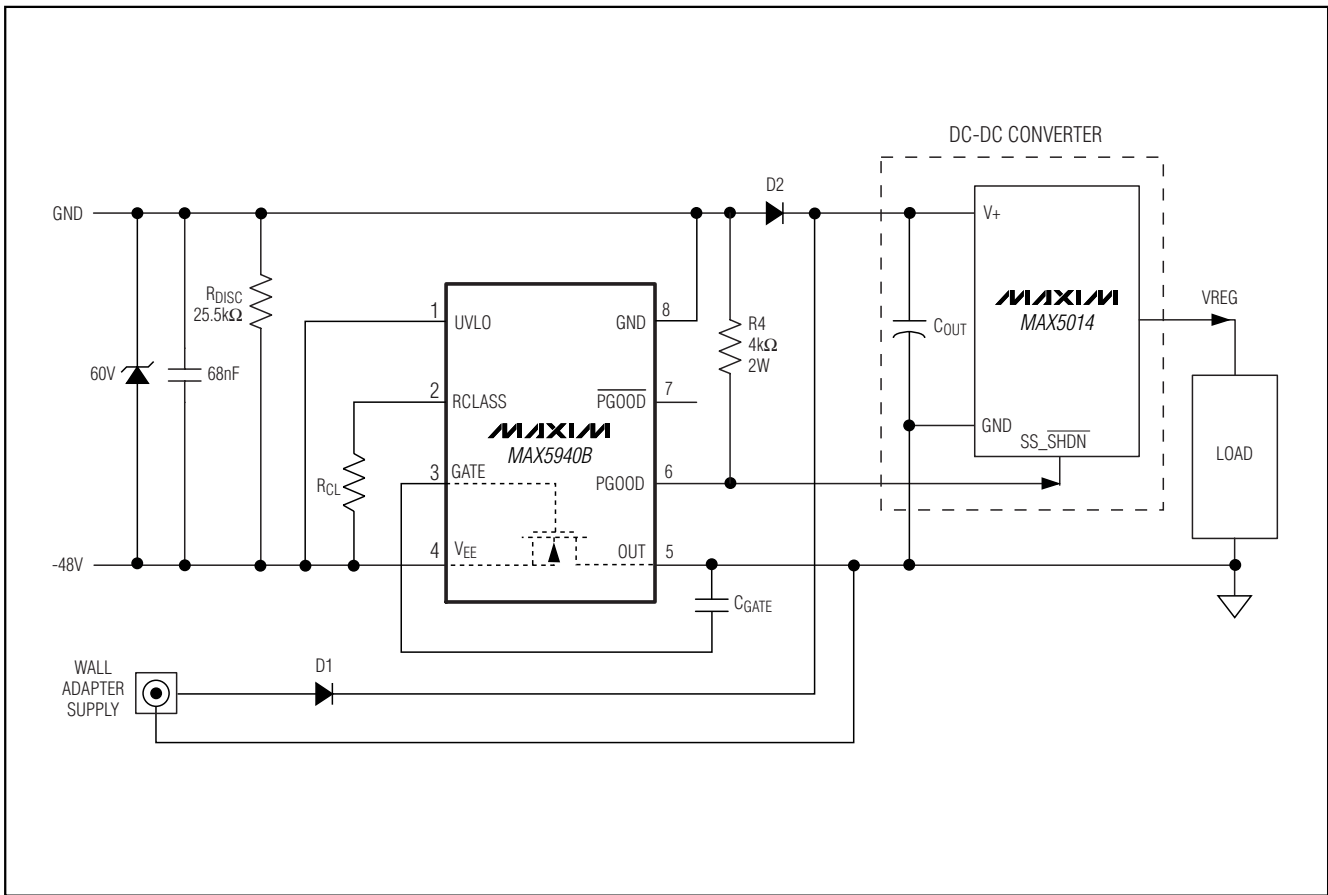


Figure 6. Adding Wall Adapter Input Supply (Wall Adapter Supply And Power-Over-Ethernet Co-Exist, the One with Higher Voltage Provides Power To The Load)

IEEE 802.3af PD Interface Controller For Power-Over-Ethernet

Typical Application Circuits (continued)

Application Circuit 4

If the wall adapter supply comes up first, it provides power to the load and pollute the discovery and classi-

fication signatures. If the power-over-ethernet comes up first, it powers the load until taken over by a wall adapter with higher output voltage.

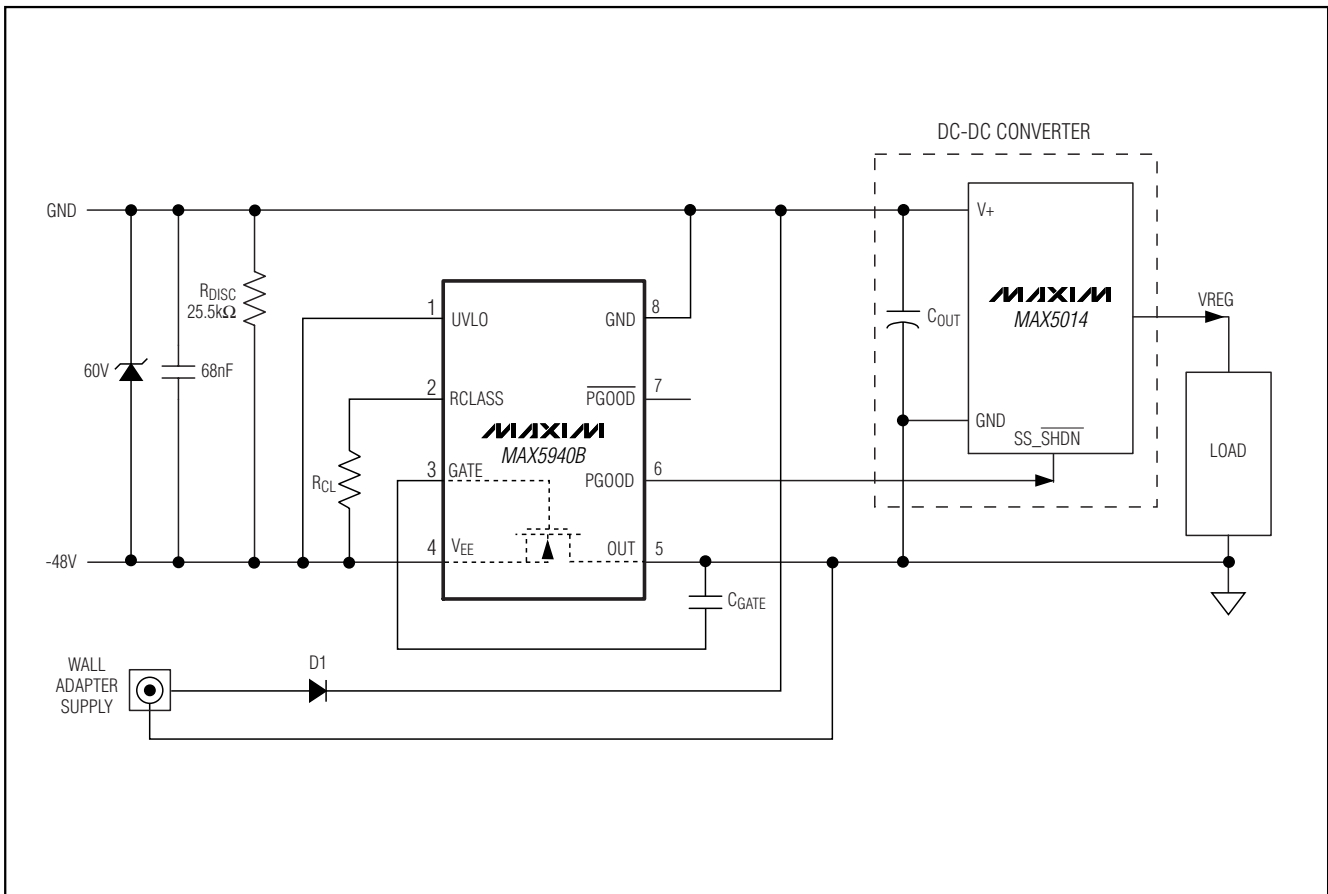
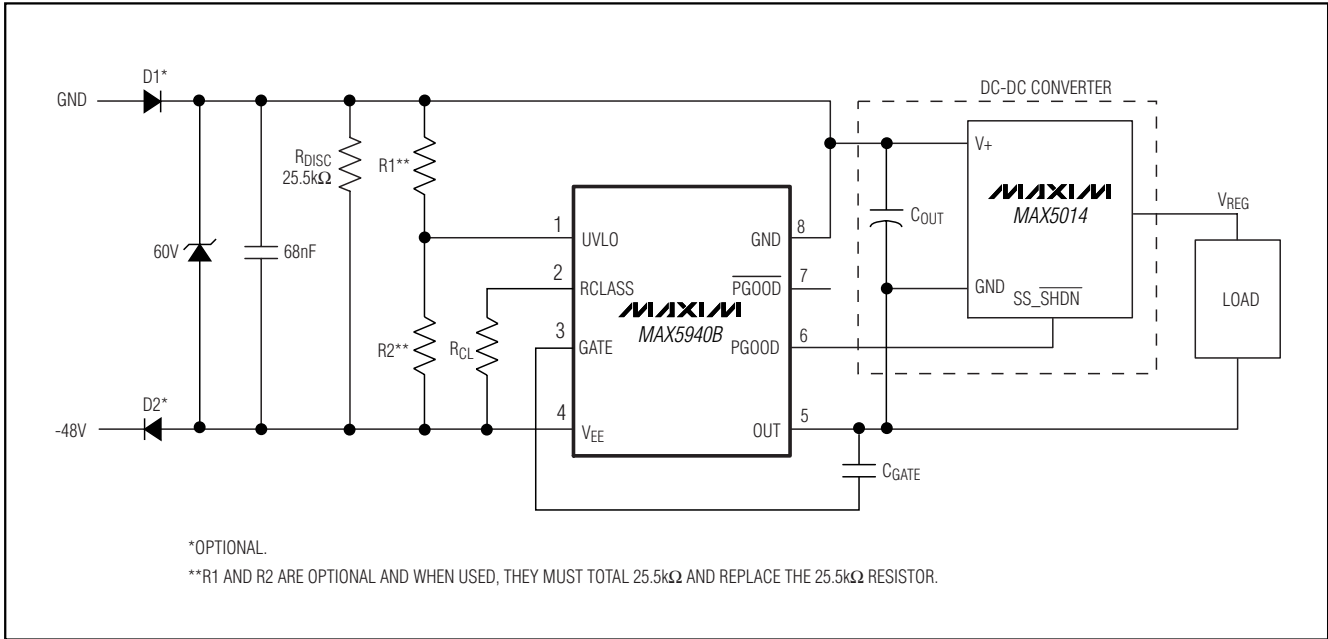


Figure 7. Adding Wall Adapter Input Supply (the One with Higher Voltage Provides Power to the Load)

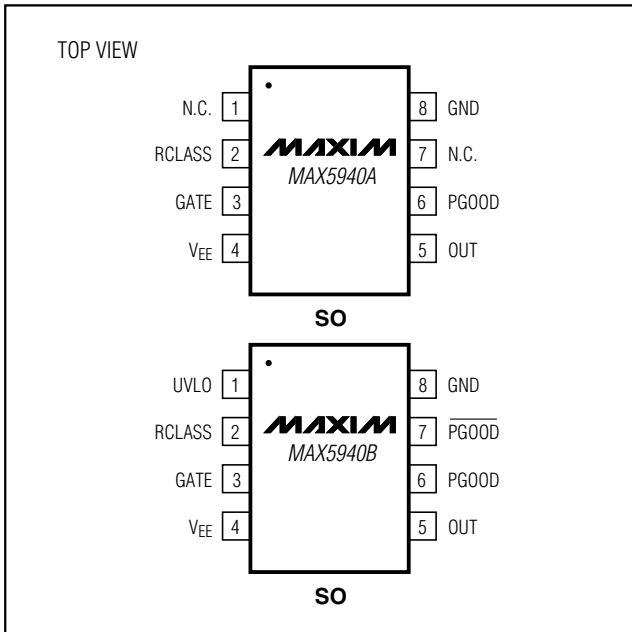
MAX5940A/MAX5940B

IEEE 802.3af PD Interface Controller For Power-Over-Ethernet

Typical Operating Circuits (continued)



Pin Configurations



Chip Information

TRANSISTOR COUNT: 3,643
PROCESS: BiCMOS

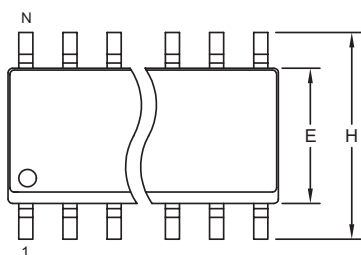
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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX5940A/MAX5940B

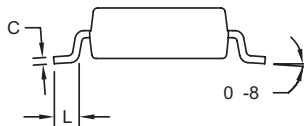
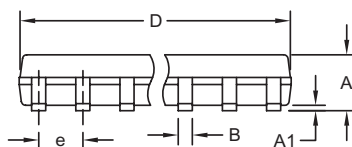
SOICN .EPS



| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

| DIM | INCHES | | MILLIMETERS | | N | MS012 |
|-----|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |



NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

| | |
|--|--|
| | |
| <small>PROPRIETARY INFORMATION</small> | |
| <small>TITLE:</small> PACKAGE OUTLINE, .150" SOIC | |
| <small>APPROVAL</small> | <small>DOCUMENT CONTROL NO.</small> 21-0041 |
| <small>REV.</small> B | <small>1/1</small> |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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