



STP80NF10 STB80NF10

N-CHANNEL 100V - 0.012Ω - 80A - TO-220/D²PAK
LOW GATE CHARGE STripFET™II MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB80NF10	100 V	< 0.015 Ω	80 A
STP80NF10	100 V	< 0.015 Ω	80 A

- TYPICAL R_{DS(on)} = 0.012Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-AC CONVERTERS
- UPS AND MOTOR CONTROL

Figure 1: Package

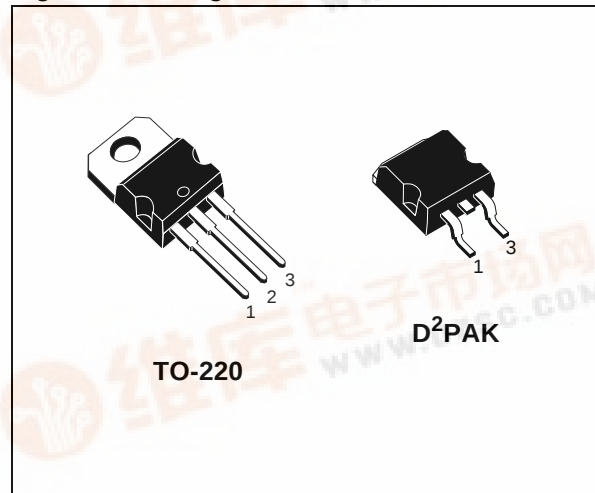


Figure 2: Internal Schematic Diagram

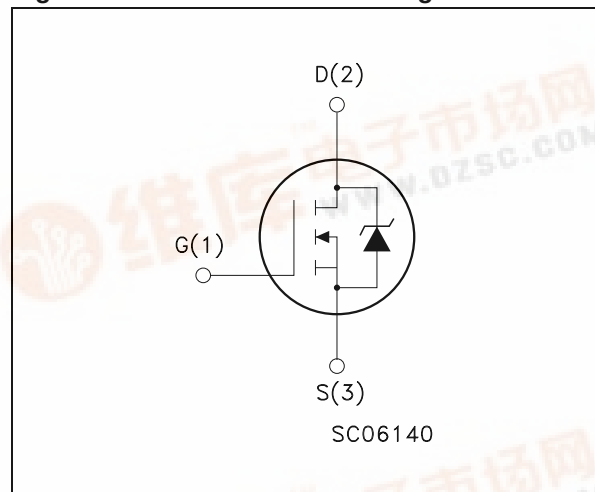


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB80NF10T4	B80NF10@	D ² PAK	TAPE & REEL
STP80NF10	P80NF10@	TO-220	TUBE

STP80NF10 - STB80NF10

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	100	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	100	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	80 (*)	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	320	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating Factor	2	W/ $^\circ\text{C}$
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	200	mJ
T_{stg}	Storage Temperature	-55 to 175	$^\circ\text{C}$
T_j	Operating Junction Temperature	175	$^\circ\text{C}$

(●) Pulse width limited by safe operating area

(*) Limited by Package

(1) $I_{SD} \leq 80\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(2) Starting $T_j = 25^\circ\text{C}$, $I_D = 80\text{A}$, $V_{DD} = 50\text{V}$

Table 4: Thermal Data

$R_{thj-case}$	Thermal Resistance Junction-case Max	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

Table 5: Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA

Table 6: On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 40\text{ A}$		0.012	0.015	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15V$, $I_D = 40A$		50		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1\text{ MHz}$, $V_{GS} = 0$		5500 700 175		pF pF pF

Table 8: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50V$, $I_D = 40A$ $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 14)		26 80		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80V$, $I_D = 80A$, $V_{GS} = 10V$		135 23 51.3	182	nC nC nC

Table 9: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off-Delay Time Fall Time	$V_{DD} = 50V$, $I_D = 40A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 14)		116 60		ns ns

Table 10: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
I_{SDM} (2)	Source-drain Current (pulsed)				320	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 80A$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 80A$, $di/dt = 100A/\mu s$, $V_{DD} = 50V$, $T_j = 150^\circ C$ (see test circuit, Figure 5)		106 0.45 8.5		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

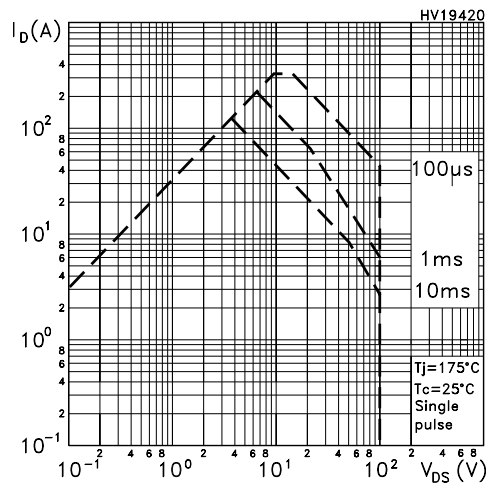


Figure 4: Output Characteristics

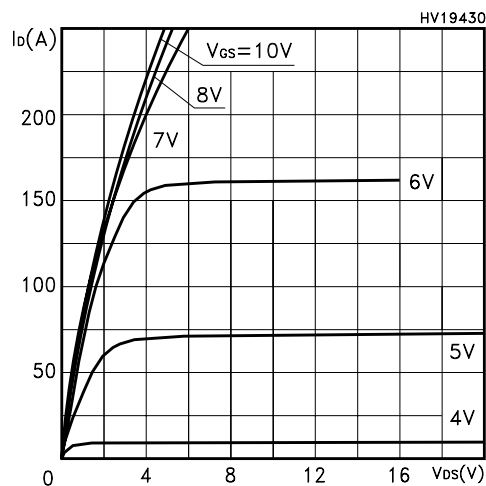


Figure 5: Transconductance

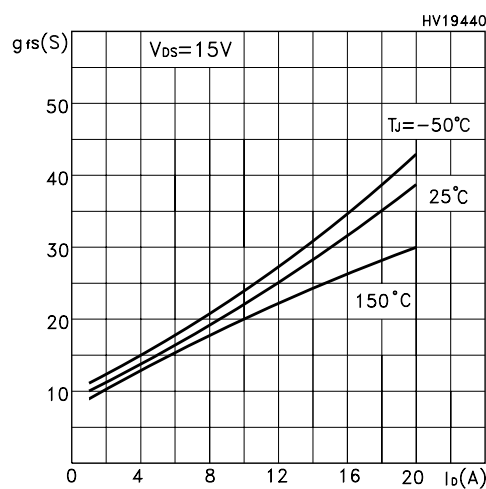


Figure 6: Thermal Impedance

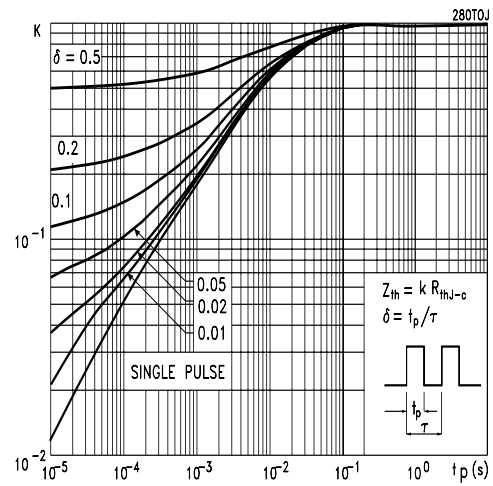


Figure 7: Transfer Characteristics

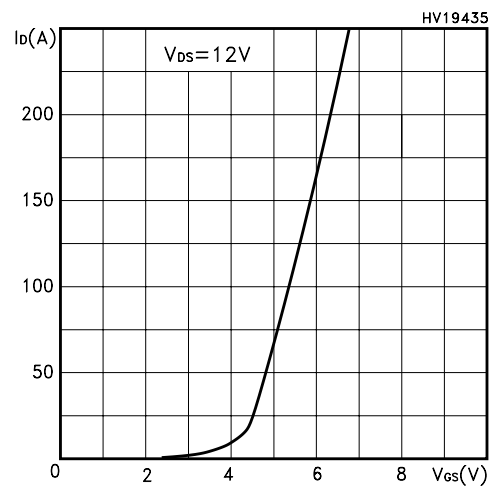


Figure 8: Static Drain-source On Resistance

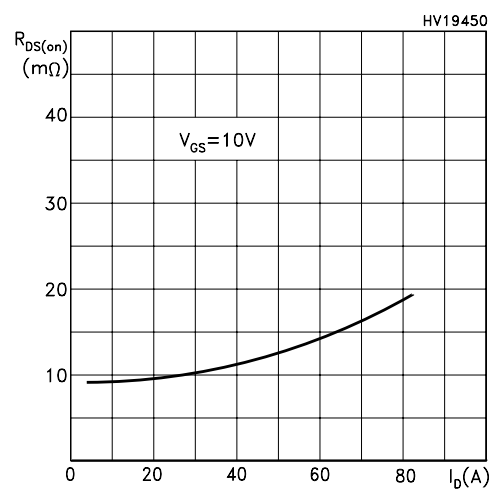


Figure 9: Gate Charge vs Gate-source Voltage

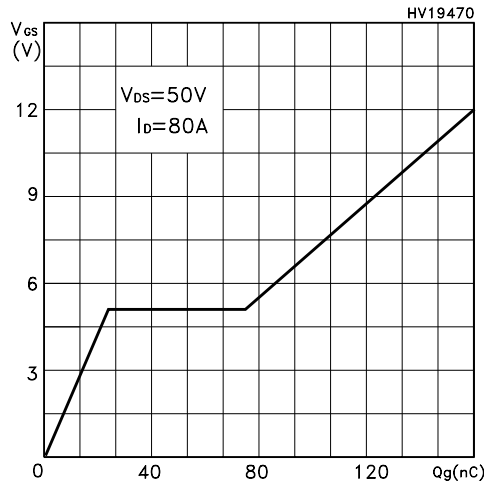


Figure 10: Normalized Gate Threshold Voltage vs Temperature

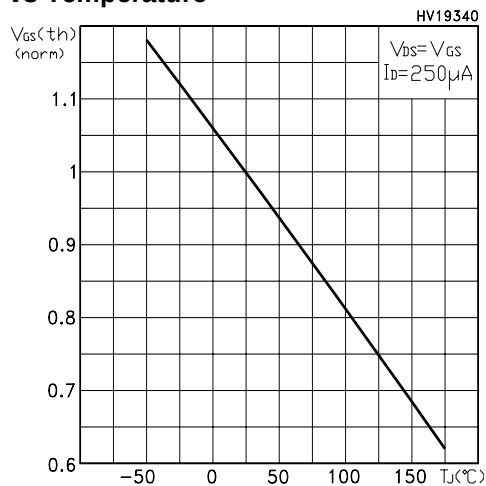


Figure 11: Source-Drain Diode Forward Characteristics

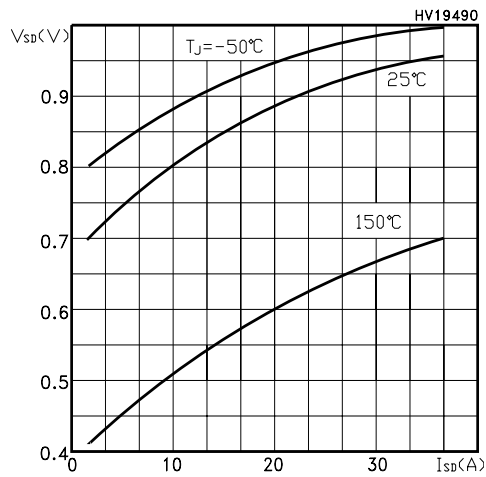


Figure 12: Capacitance Variations

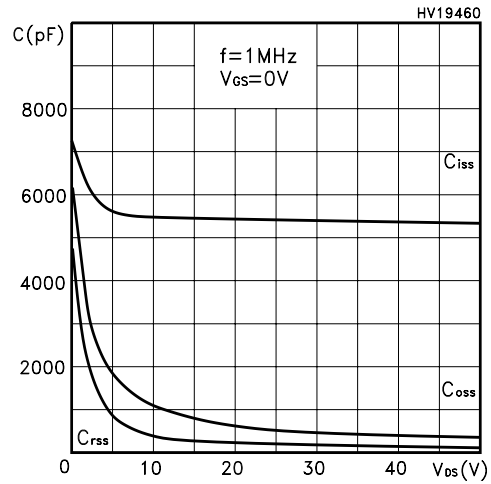


Figure 13: Normalized On Resistance vs Temperature

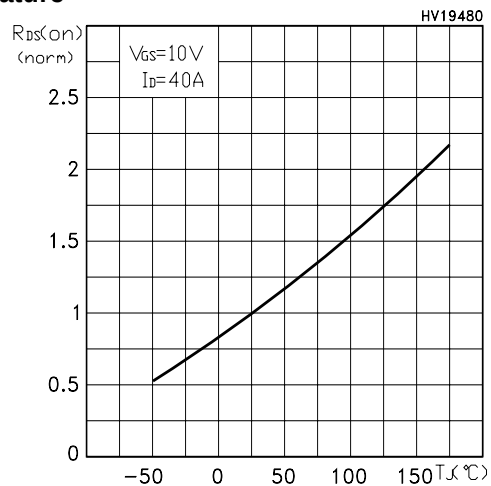


Figure 14: Switching Times Test Circuit For Resistive Load

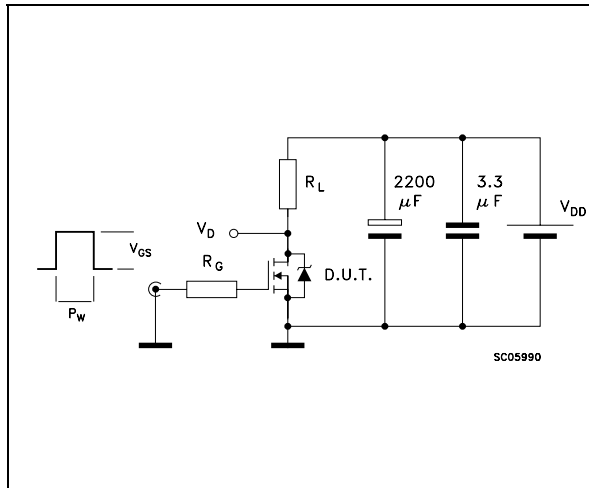


Figure 15: Test Circuit For Inductive Load Switching and Diode Recovery Times

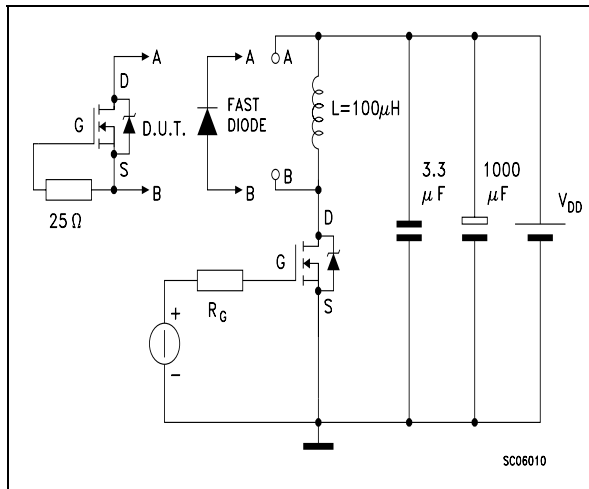
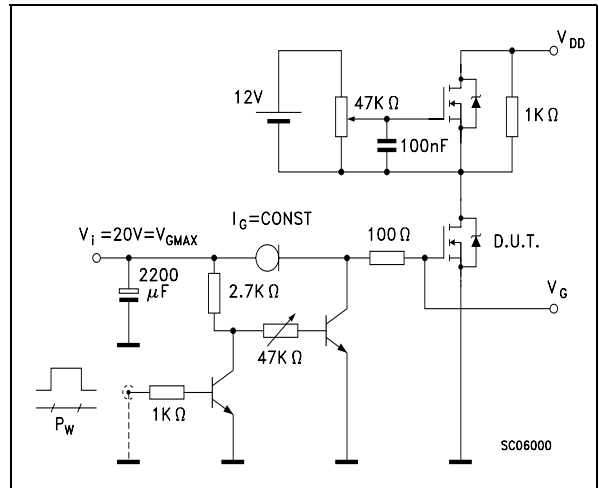
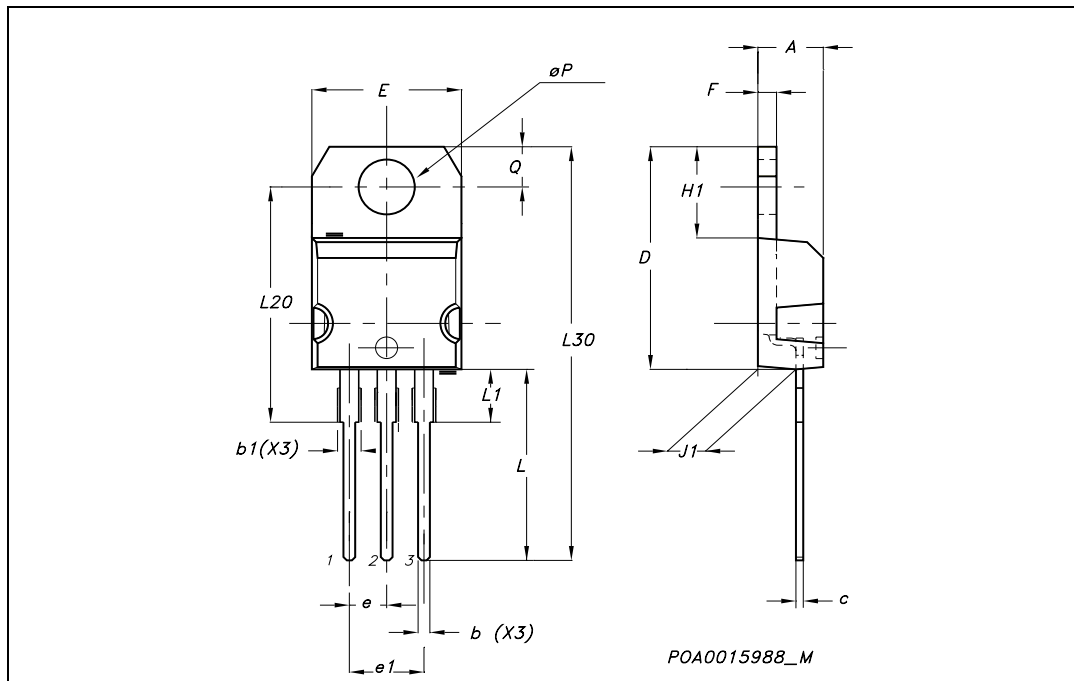


Figure 16: Gate Charge Test Circuit



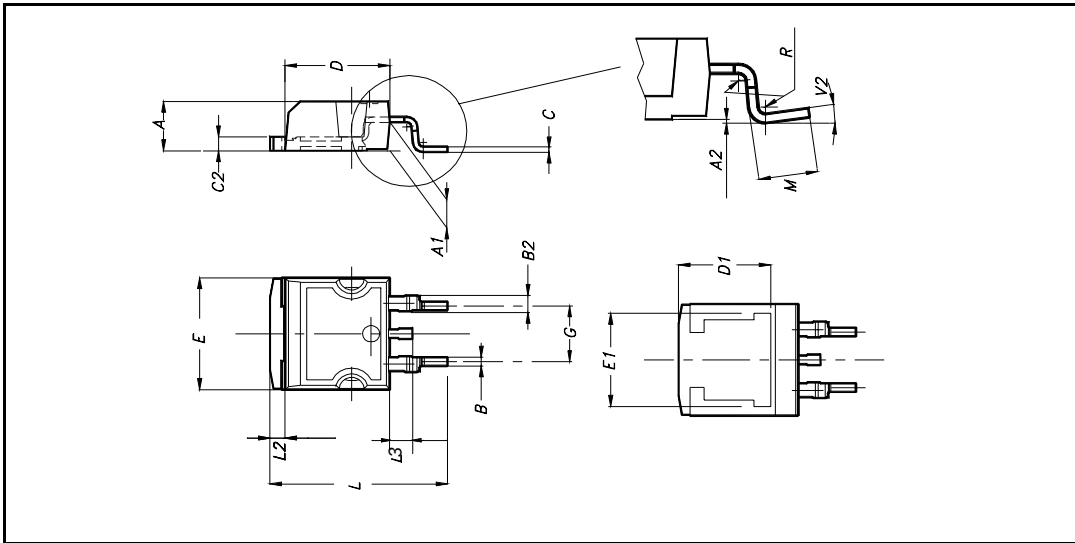
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

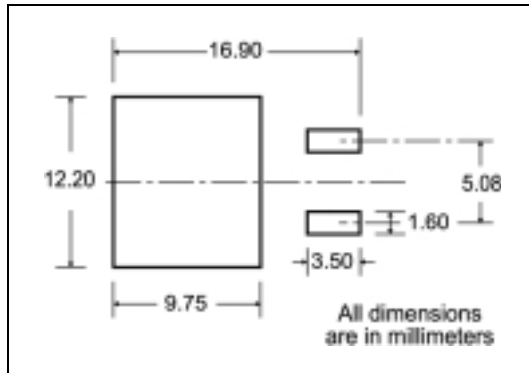


D²PAK MECHANICAL DATA

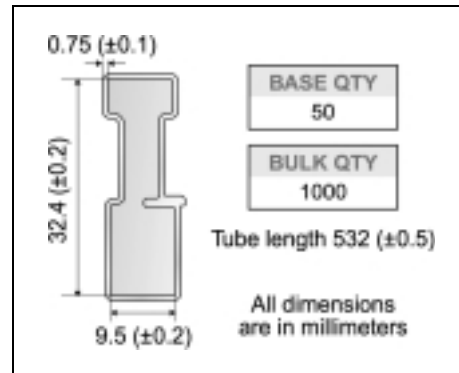
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



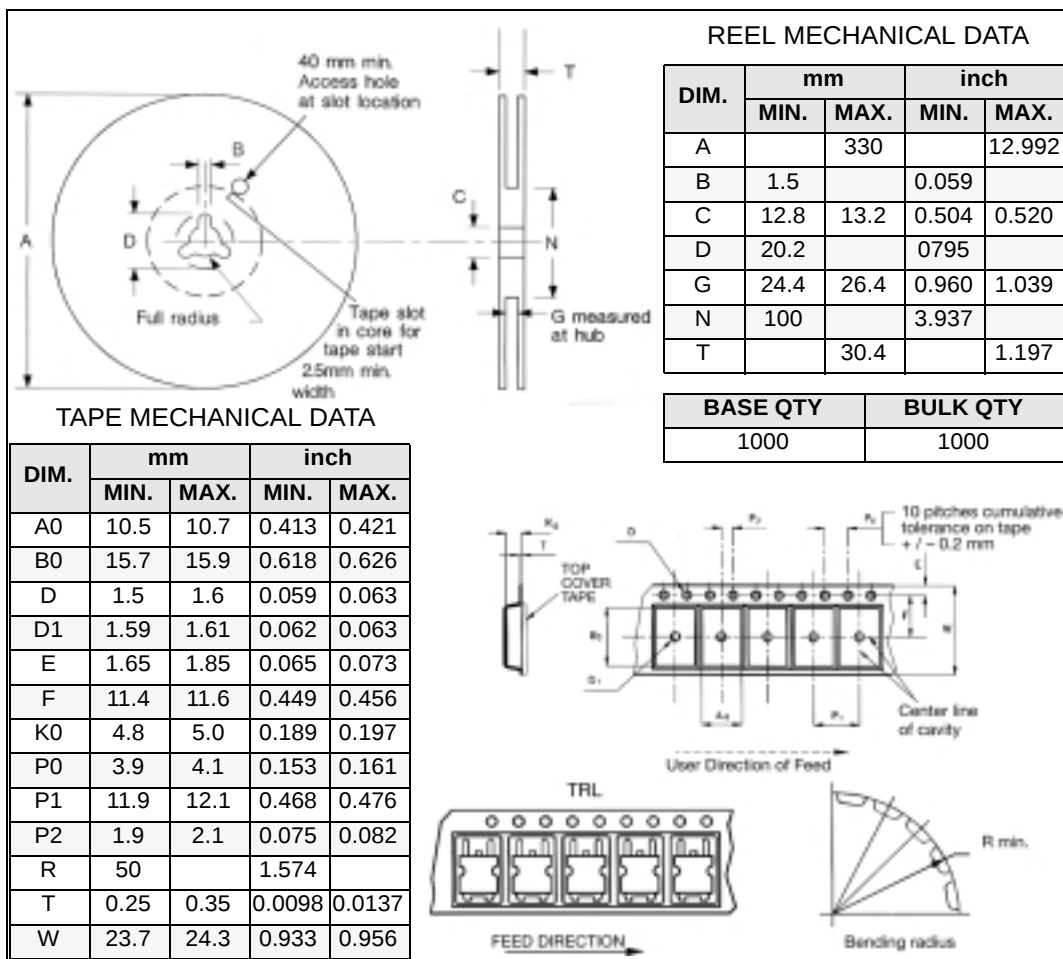
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



* on sales type

STP80NF10 - STB80NF10

Table 11: Revision History

Date	Revision	Description of Changes
04-Nov-2003	1	NEW DATASHEET ACCORDING TO PCN DSG-TRA/03/382
22-Nov-2004	2	NEW STYLESHEET, NO CONTENT CHANGE
21-Jan-2005	3	Value Change on Table 3

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