SYNERGY SEMICONDUCTOR

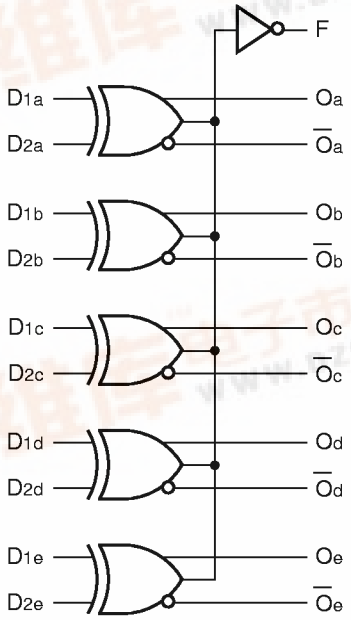
QUINT EXCLUSIVE OR/NOR GATE

SY100S307

FEATURES

- Max. propagation delay of 1000ps
- IEE min. of –58mA
- Extended supply voltage option: VEE = –4.2V to –5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than National 300K at lower power
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPACK and 28-pin PLCC packages

BLOCK DIAGRAM



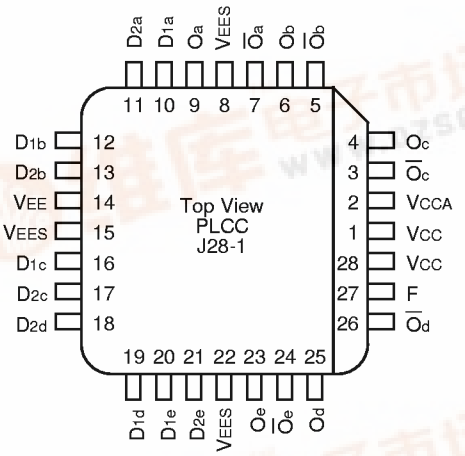
PIN NAMES

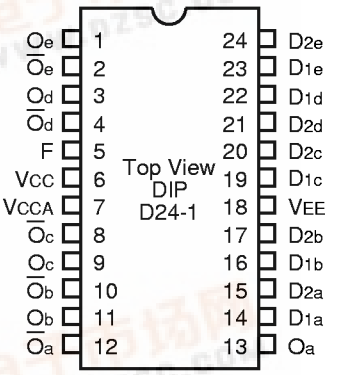
Pin	Function
Dna – Dne	Data Inputs (n-1...5)
E	Enable Input
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

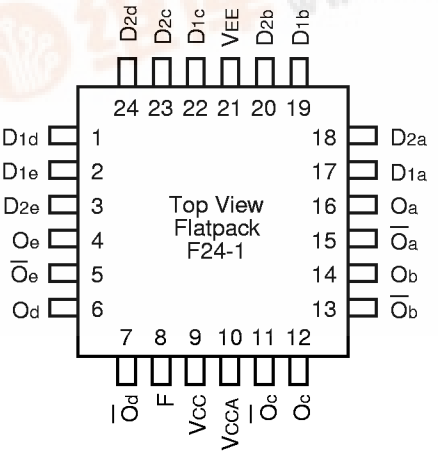
DESCRIPTION

The SY100S307 is an ultra-fast quint exclusive-OR/NOR gate designed for use in high-performance ECL systems. A function output that is the wire-OR result of the exclusive-OR outputs is also available. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS







LOGIC EQUATION

F = $(D1a \oplus D2a) + (D1b \oplus D2b) + (D1c \oplus D2c) + (D1d \oplus D2d) + (D1e \oplus D2e)$.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current $D2a$ — $D2e$ $D2a$ — $D2e$	 — —	 — —	 200 250	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–58	–40	–27	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PH2}	Propagation Delay $D2a$ — $D2e$ to O, $\overline{O}$	200	1200	200	1150	300	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay $D1a$ — $D1e$ to O, $\overline{O}$	200	1100	200	1050	200	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1625	300	1625	300	1625	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PH2}	Propagation Delay $D2a$ — $D2e$ to O, $\overline{O}$	200	1100	200	1150	200	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay $D1a$ — $D1e$ to O, $\overline{O}$	200	1000	200	950	200	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1525	300	1525	300	1525	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

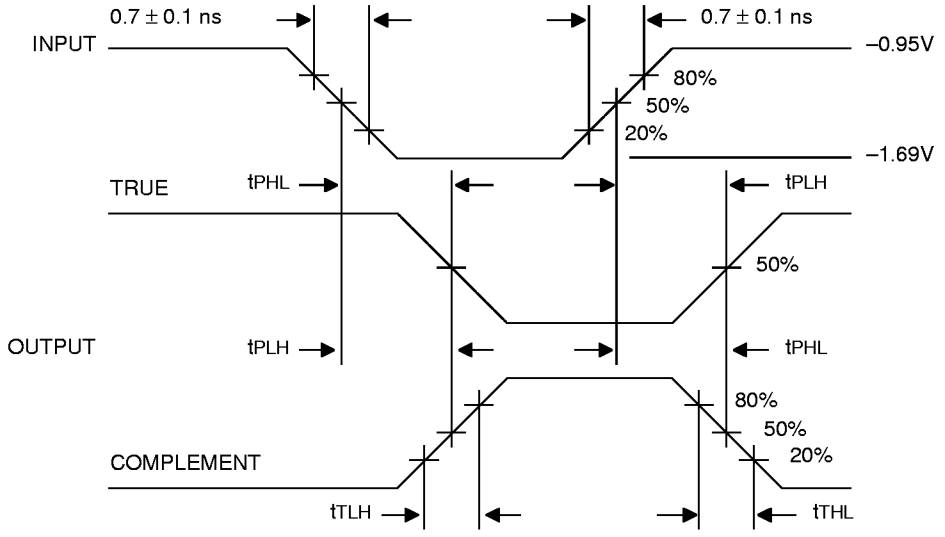
AC ELECTRICAL CHARACTERISTICS (Continued)

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PH2}	Propagation Delay D_{2a} — D_{2e} to O, $\overline{O}$	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay D_{1a} — D_{1e} to O, $\overline{O}$	300	900	300	900	300	930	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1425	300	1425	300	1425	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



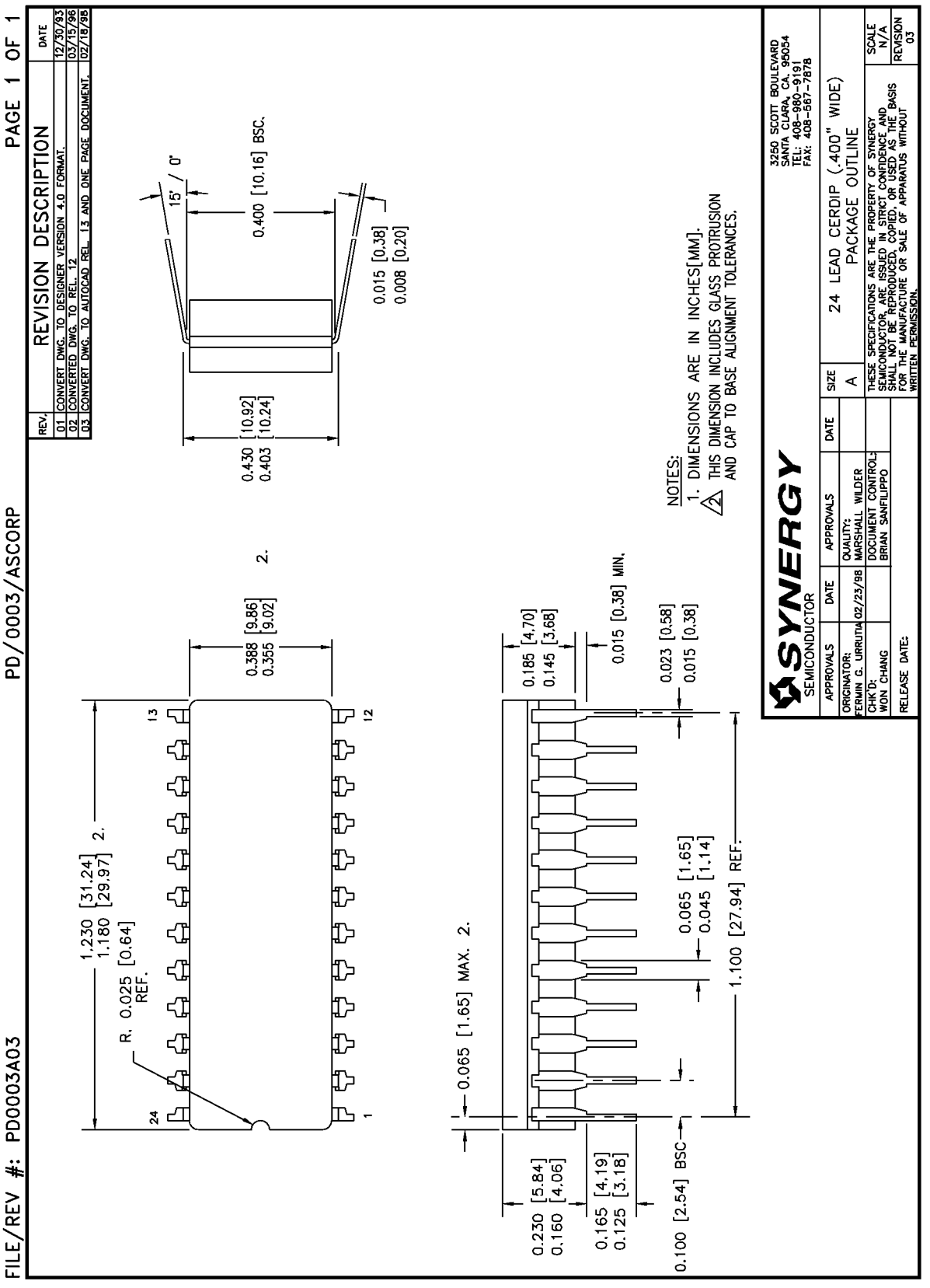
Propagation Delay and Transition Times

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

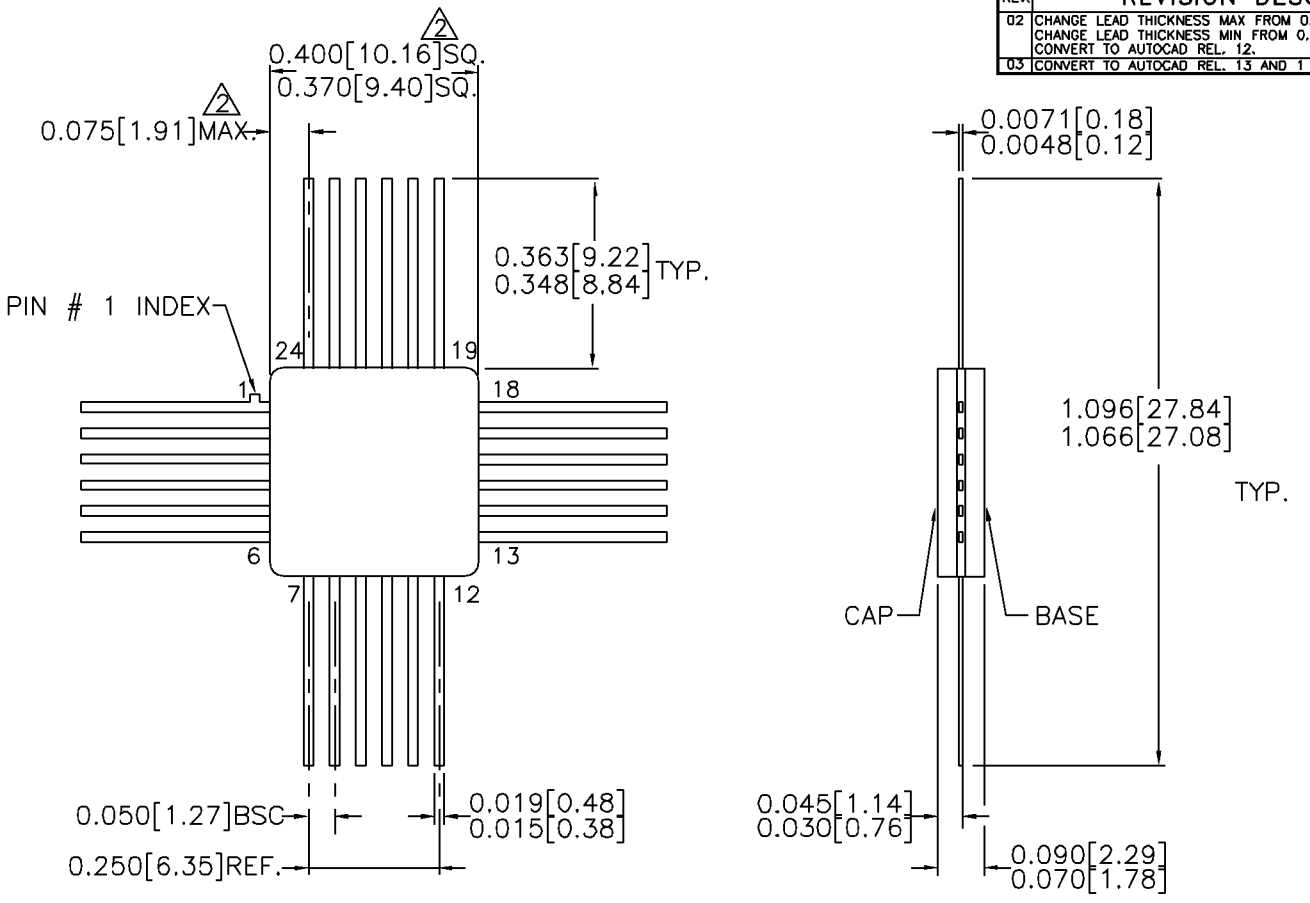
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S307DC	D24-1	Commercial
SY100S307FC	F24-1	Commercial
SY100S307JC	J28-1	Commercial
SY100S307JCTR	J28-1	Commercial

24 LEAD CERDIP (D24-1)



REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006[0.15] TO 0.0071[0.18] CHANGE LEAD THICKNESS MIN FROM 0.004[0.10] TO 0.0048[0.12] CONVERT TO AUTOCAD REL. 12.	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

SYNERGY SEMICONDUCTOR
3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO	
RELEASE DATE:			

SIZE: A

24 LEAD CERPACK
PACKAGE OUTLINE

SCALE: N/A
REVISION: 03

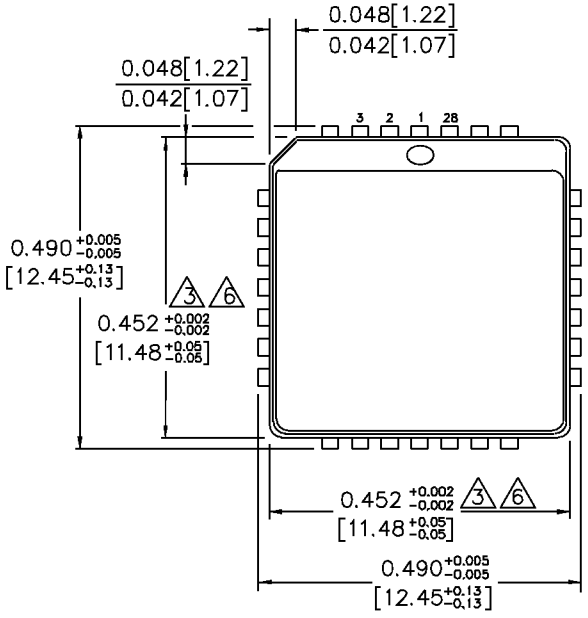
24 LEAD CERPACK (F24-1)

SYNERGY SEMICONDUCTOR

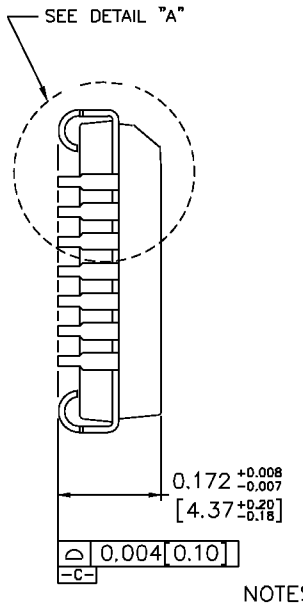
SY100S307

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

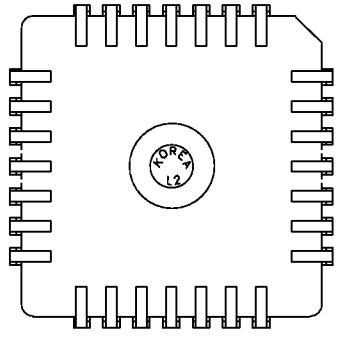
TOP VIEW



SIDE VIEW

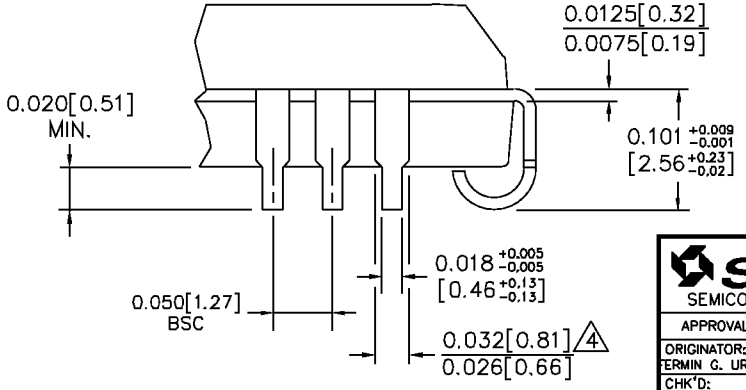


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

SYNERGY SEMICONDUCTOR

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SANTA CLARA, CA, 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE
ORIGINATOR: TERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO	
RELEASE DATE:			

SIZE	
A	28 LEAD PLCC PACKAGE OUTLINE

SCALE N/A

REVISION 03

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

SYNERGY SEMICONDUCTOR

SY100S307