IDT

HIGH-SPEED 3.3V 32K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

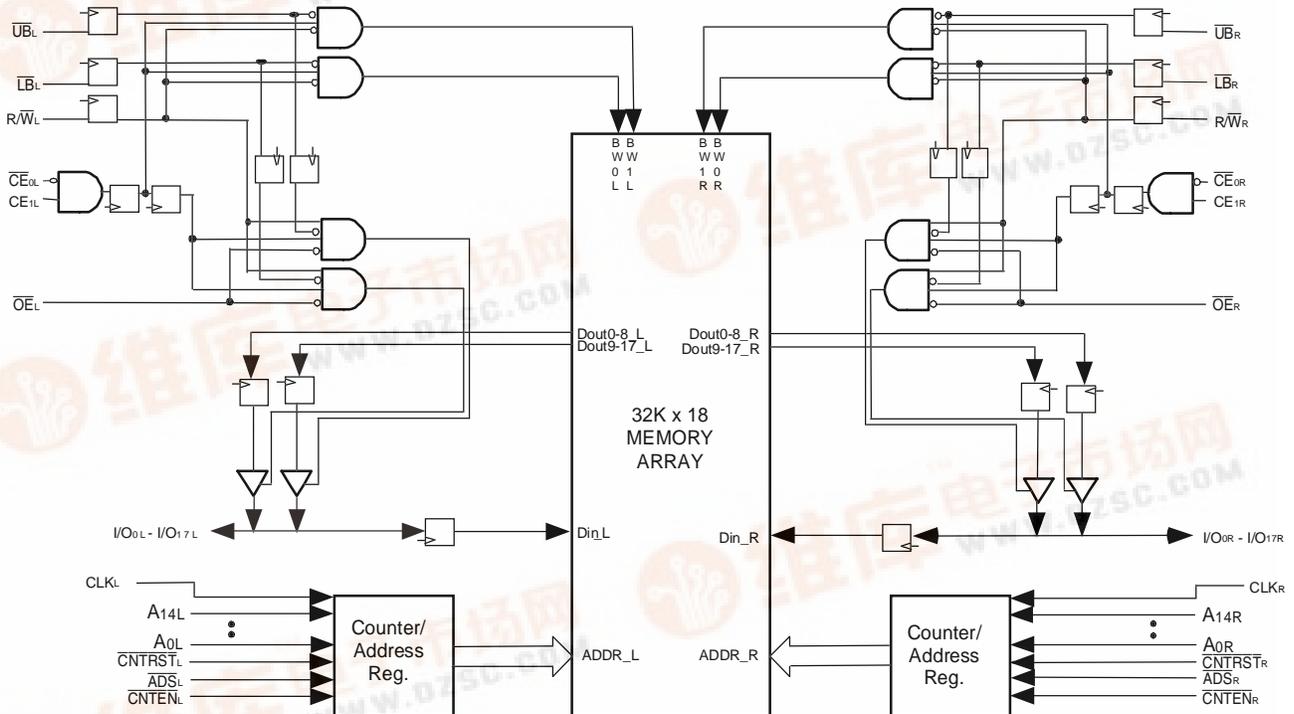## IDT70V3379S

Features:

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - Commercial: 4.2/5/6ns (max.)
  - Industrial: 5/6ns (max)
- Pipelined output mode
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
  - Fast 4.2ns clock to data out
  - 1.8ns setup to clock and 0.7ns hold on all control, data, and
    - address inputs @ 133MHz
  - Data input, address, byte enable and control registers
  - Self-timed write allows fast cycle time
- Separate byte controls for multiplexed bus and bus matching compatibility
- LVTTL- compatible, single 3.3V (±150mV) power supply for core
- LVTTL- compatible, selectable 3.3V (±150mV)/2.5V (±125mV) power supply for I/Os and control signals on each port
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Available in a 128-pin Thin Quad Plastic Flatpack (TQFP) and 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array

Functional Block Diagram

4833 tbl 01

Description:

The IDT70V3379 is a high-speed 32K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3379 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3379 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Pin Configuration[1,2,3,4]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
	I/O_{9L}	NC	V_{SS}	NC	NC	NC	A_{12L}	A_{8L}	NC	V_{DD}	CLK_L	$\overline{CNTEN_L}$	A_{4L}	A_{0L}	OPT_L	NC	V_{SS}	A
	NC	V_{SS}	NC	V_{SS}	NC	A_{13L}	A_{9L}	NC	$\overline{CE_{0L}}$	V_{SS}	$\overline{ADS_L}$	A_{5L}	A_{1L}	V_{SS}	V_{DDQR}	I/O_{8L}	NC	B
	V_{DDQL}	I/O_{9R}	V_{DDQR}	V_{DD}	NC	A_{14L}	A_{10L}	$\overline{UB_L}$	CE_{1L}	V_{SS}	$R/\overline{W}_L$	A_{6L}	A_{2L}	V_{DD}	I/O_{8R}	NC	V_{SS}	C
	NC	V_{SS}	I/O_{10L}	NC	NC	A_{11L}	A_{7L}	$\overline{LB_L}$	V_{DD}	$\overline{OE_L}$	$\overline{CNTRST_L}$	A_{3L}	V_{DD}	NC	V_{DDQL}	I/O_{7L}	I/O_{7R}	D
	I/O_{11L}	NC	V_{DDQR}	I/O_{10R}										I/O_{6L}	NC	V_{SS}	NC	E
	V_{DDQL}	I/O_{11R}	NC	V_{SS}										V_{SS}	I/O_{6R}	NC	V_{DDQR}	F
	NC	V_{SS}	I/O_{12L}	NC										NC	V_{DDQL}	I/O_{5L}	NC	G
	V_{DD}	NC	V_{DDQR}	I/O_{12R}										V_{DD}	NC	V_{SS}	I/O_{5R}	H
	V_{DDQL}	V_{DD}	V_{SS}	V_{SS}										V_{SS}	V_{DD}	V_{SS}	V_{DDQR}	J
	I/O_{14R}	V_{SS}	I/O_{13R}	V_{SS}										I/O_{3R}	V_{DDQL}	I/O_{4R}	V_{SS}	K
	NC	I/O_{14L}	V_{DDQR}	I/O_{13L}										NC	I/O_{3L}	V_{SS}	I/O_{4L}	L
	V_{DDQL}	NC	I/O_{15R}	V_{SS}										V_{SS}	NC	I/O_{2R}	V_{DDQR}	M
	NC	V_{SS}	NC	I/O_{15L}										I/O_{1R}	V_{DDQL}	NC	I/O_{2L}	N
	I/O_{16R}	I/O_{16L}	V_{DDQR}	NC	NC	NC	A_{12R}	A_{8R}	NC	V_{DD}	CLK_R	$\overline{CNTEN_R}$	A_{4R}	NC	I/O_{1L}	V_{SS}	NC	P
	V_{SS}	NC	I/O_{17R}	NC	NC	A_{13R}	A_{9R}	NC	$\overline{CE_{0R}}$	V_{SS}	$\overline{ADS_R}$	A_{5R}	A_{1R}	V_{SS}	V_{DDQL}	I/O_{0R}	V_{DDQR}	R
	NC	I/O_{17L}	V_{DDQL}	V_{SS}	NC	A_{14R}	A_{10R}	$\overline{UB_R}$	CE_{1R}	V_{SS}	$R/\overline{W}_R$	A_{6R}	A_{2R}	V_{SS}	NC	V_{SS}	NC	T
	V_{SS}	NC	V_{DD}	NC	NC	A_{11R}	A_{7R}	$\overline{LB_R}$	V_{DD}	$\overline{OE_R}$	$\overline{CNTRST_R}$	A_{3R}	A_{0R}	V_{DD}	OPT_R	NC	I/O_{0L}	U

Center: 70V3379BF BF-208[5] 208-Pin fpBGA Top View[6]

4833 tbl 02

NOTES:
1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4] (con't.)

70V3379BC
BC-256[5]

256-Pin BGA
Top View[6]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	A_{14L}	A_{11L}	A_{8L}	NC	$CE1_L$	$\overline{OE}_L$	$CNTEN_L$	A_{5L}	A_{2L}	A_{0L}	NC	NC
B	NC	NC	NC	NC	NC	A_{12L}	A_{9L}	$\overline{UB}_L$	$\overline{CE0}_L$	$R/\overline{W}_L$	$\overline{CNTRST}_L$	A_{4L}	A_{1L}	V_{DD}	NC	NC
C	NC	I/O_{9L}	V_{SS}	NC	A_{13L}	A_{10L}	A_{7L}	NC	$\overline{LB}_L$	CLK_L	$\overline{ADS}_L$	A_{6L}	A_{3L}	OPT_L	NC	I/O_{8L}
D	NC	I/O_{9R}	NC	V_{DD}	V_{DDQL}	V_{DDQL}	V_{DDQR}	V_{DDQR}	V_{DDQL}	V_{DDQL}	V_{DDQR}	V_{DDQR}	V_{DD}	NC	NC	I/O_{8R}
E	I/O_{10R}	I/O_{10L}	NC	V_{DDQL}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{DDQR}	NC	I/O_{7L}	I/O_{7R}
F	I/O_{11L}	NC	I/O_{11R}	V_{DDQL}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQR}	I/O_{6R}	NC	I/O_{6L}
G	NC	NC	I/O_{12L}	V_{DDQR}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQL}	I/O_{5L}	NC	NC
H	NC	I/O_{12R}	NC	V_{DDQR}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQL}	NC	NC	I/O_{5R}
J	I/O_{13L}	I/O_{14R}	I/O_{13R}	V_{DDQL}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQR}	I/O_{4R}	I/O_{3R}	I/O_{4L}
K	NC	NC	I/O_{14L}	V_{DDQL}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQR}	NC	NC	I/O_{3L}
L	I/O_{15L}	NC	I/O_{15R}	V_{DDQR}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQL}	I/O_{2L}	NC	I/O_{2R}
M	I/O_{16R}	I/O_{16L}	NC	V_{DDQR}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{DDQL}	I/O_{1R}	I/O_{1L}	NC
N	NC	I/O_{17R}	NC	V_{DD}	V_{DDQR}	V_{DDQR}	V_{DDQL}	V_{DDQL}	V_{DDQR}	V_{DDQR}	V_{DDQL}	V_{DDQL}	V_{DD}	NC	I/O_{0R}	NC
P	NC	I/O_{17L}	NC	NC	A_{13R}	A_{10R}	A_{7R}	NC	$\overline{LB}_R$	CLK_R	$\overline{ADS}_R$	A_{6R}	A_{3R}	NC	NC	I/O_{0L}
R	NC	NC	NC	NC	NC	A_{12R}	A_{9R}	$\overline{UB}_R$	$\overline{CE0}_R$	$R/\overline{W}_R$	$\overline{CNTRST}_R$	A_{4R}	A_{1R}	OPT_R	NC	NC
T	NC	NC	NC	NC	A_{14R}	A_{11R}	A_{8R}	NC	$CE1_R$	$\overline{OE}_R$	$CNTEN_R$	A_{5R}	A_{2R}	A_{0R}	NC	NC

4833 drw 02c

NOTES:
1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3,4] (con't.)

70V3379PRF
PK-128[5]

128-Pin TQFP
Top View[6]

4833 drw 02a
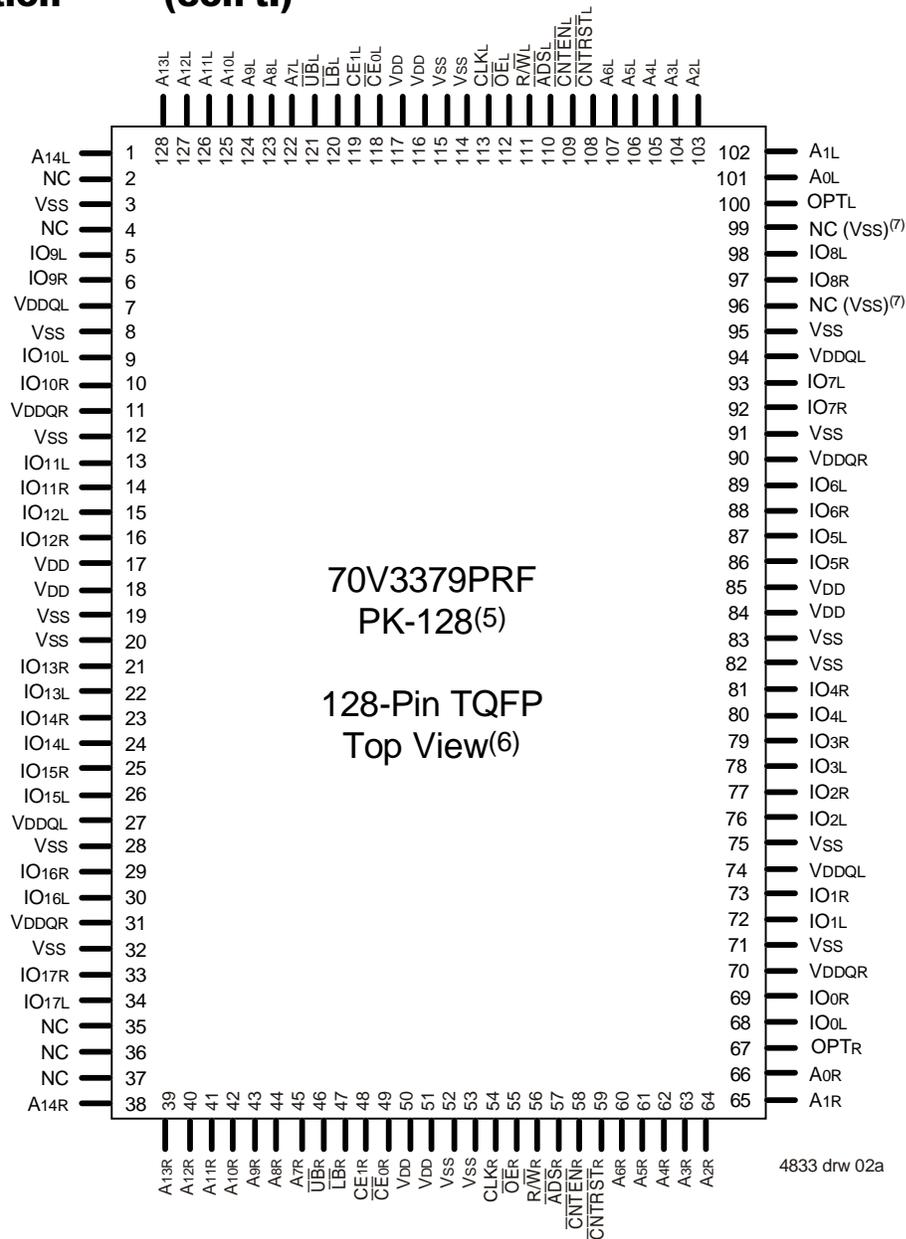
NOTES:
1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
7. In the 70V3379 (32K x 18) and 70V3389 (64K x 18), pins 96 and 99 are NC. The upgrade devices 70V3399 (128K x 18) and 70V3319 (256K x 18) assign these pins as V_{SS}. Customers who plan to take advantage of the upgrade path should treat these pins as VSS on the 70V3379 and 70V3389. If no upgrade is needed, the pins can be treated as NC.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{14L}	A_{0R} - A_{14R}	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
UB_L - LB_L	UB_R - LB_R	Byte Enables (9-bit bytes)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)[1]
OPT_L	OPT_R	Option for selecting V_{DDQX}[1,2]
V_{DD}		Power (3.3V)[1]
V_{SS}		Ground (0V)

4833 tbl 01

NOTES:
1. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to V_{IH} (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to V_{IL} (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O$_{9-18}$	Lower Byte I/O$_{0-8}$	MODE
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D$_{IN}$	Write to Lower Byte Only
X	↑	L	H	L	H	L	D$_{IN}$	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D$_{IN}$	D$_{IN}$	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D$_{OUT}$	Read Lower Byte Only
L	↑	L	H	L	H	H	D$_{OUT}$	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D$_{OUT}$	D$_{OUT}$	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

4833 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = V_{IH}.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control[1,2]

Address	Previous Address	Addr Used	CLK[6]	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O[3]	MODE
X	X	0	↑	X	X	L[4]	D$_{I/O}$(0)	Counter Reset to Address 0
An	X	An	↑	L[4]	X	H	D$_{I/O}$(n)	External Address Used
An	Ap	Ap	↑	H	H	H	D$_{I/O}$(p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L[5]	H	D$_{I/O}$(p+1)	Counter Enabled—Internal Address generation

4833 tbl 03

NOTES:
1. "H" = V$_{IH}$, "L" = V$_{IL}$, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE$_1$, $\overline{BE}$n and $\overline{OE}$.
3. Outputs are in Pipelined mode: the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{CNTRST}$ are independent of all other memory control signals including $\overline{CE}_0$, CE$_1$ and $\overline{BE}$n
5. The address counter advances if $\overline{CNTEN}$ = V$_{IL}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE$_1$, $\overline{BE}$n.

Recommended Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	V$_{DD}$
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4833 tbl 04

NOTES:
1. Industrial temperature: for specific speeds, packages and powers contact your sales office.
2. This is the parameter T$_A$. This is the "instant on" case tempereature.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T$_{BIAS}$	Temperature Under Bias	-55 to +125	°C
T$_{STG}$	Storage Temperature	-65 to +150	°C
I$_{OUT}$	DC Output Current	50	mA

4833 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V$_{TERM}$ must not exceed V$_{DD}$ + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to $\leq$ 20mA for the period of V$_{TERM}$ $\geq$ V$_{DD}$ + 150mV.

Recommended DC Operating Conditions with V$_{DDQ}$ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{DD}$	Core Supply Voltage	3.15	3.3	3.45	V
V$_{DDQ}$	I/O Supply Voltage[3]	2.375	2.5	2.625	V
V$_{SS}$	Ground	0	0	0	V
V$_{IH}$	Input High Voltage[3] (Address & Control Inputs)	1.7	—	V$_{DDQ}$ + 125mV[2]	V
V$_{IH}$	Input High Voltage - I/O[3]	1.7	—	V$_{DDQ}$ + 125mV[2]	V
V$_{IL}$	Input Low Voltage	-0.3[1]	—	0.7	V

4833 tbl 05a

NOTES:
1. V$_{IL}$ $\geq$ -1.5V for pulse width less than 10 ns.
2. V$_{TERM}$ must not exceed V$_{DDQ}$ + 125mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V$_{IL}$ (0V), and V$_{DDQX}$ for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V$_{DDQ}$ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{DD}$	Core Supply Voltage	3.15	3.3	3.45	V
V$_{DDQ}$	I/O Supply Voltage[3]	3.15	3.3	3.45	V
V$_{SS}$	Ground	0	0	0	V
V$_{IH}$	Input High Voltage (Address & Control Inputs)[3]	2.0	—	V$_{DDQ}$ + 150mV[2]	V
V$_{IH}$	Input High Voltage - I/O[3]	2.0	—	V$_{DDQ}$ + 150mV[2]	V
V$_{IL}$	Input Low Voltage	-0.3[1]	—	0.8	V

4833 tbl 05b

NOTES:
1. V$_{IL}$ $\geq$ -1.5V for pulse width less than 10 ns.
2. V$_{TERM}$ must not exceed V$_{DDQ}$ + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V$_{IH}$ (3.3V), and V$_{DDQX}$ for that port must be supplied as indicated above.

Capacitance[1]

(T_A = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10.5	pF

4833 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3379S Min.	70V3379S Max.	Unit
$|I_{LI}|$	Input Leakage Current[1]	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$|I_{LO}|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage[2]	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage[2]	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage[2]	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage[2]	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

4833 tbl 08

NOTE:
1. At $V_{DD} \leq$ - 2.0V input leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3] (V_{DD} = 3.3V ± 150mV)

| Symbol	Parameter	Test Condition	Version		70V3379S4 Com'l Only		70V3379S5 Com'l & Ind		70V3379S6 Com'l & Ind		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	375	460	285	360	245	310	mA
			IND	S	—	—	285	415	245	360	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	S	145	190	105	145	95	125	mA
			IND	S	—	—	105	175	95	150	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	S	265	325	190	260	175	225	mA
			IND	S	—	—	190	300	175	260	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L	S	6	15	6	15	6	15	mA
			IND	S	—	—	6	30	6	30	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{DD} - 0.2V[5] V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	265	325	180	260	170	225	mA
			IND	S	—	—	180	300	170	260	

4833 tbl 09

NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. I_{DD} $_{DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}$x = V_{IL} means $\overline{CE}$0x = V_{IL} and CE1x = V_{IH}
   $\overline{CE}$x = V_{IH} means $\overline{CE}$0x = V_{IH} or CE1x = V_{IL}
   $\overline{CE}$x ≤ 0.2V means $\overline{CE}$0x ≤ 0.2V and CE1x ≥ V_{CC} - 0.2V
   $\overline{CE}$x ≥ V_{CC} - 0.2V means $\overline{CE}$0x ≥ V_{CC} - 0.2V or CE1x - 0.2V
   "X" represents "L" for left port or "R" for right port.
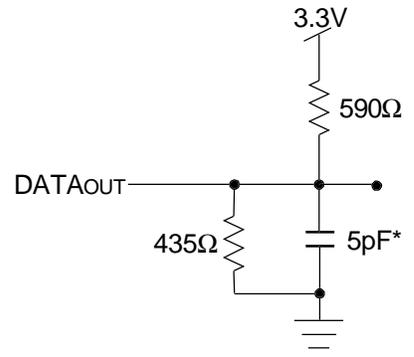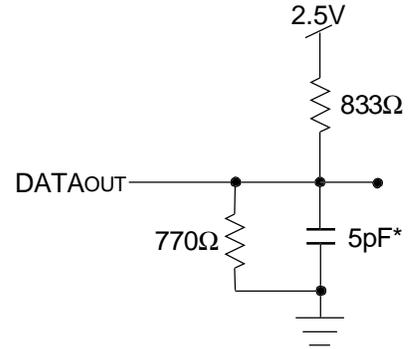
AC Test Conditions

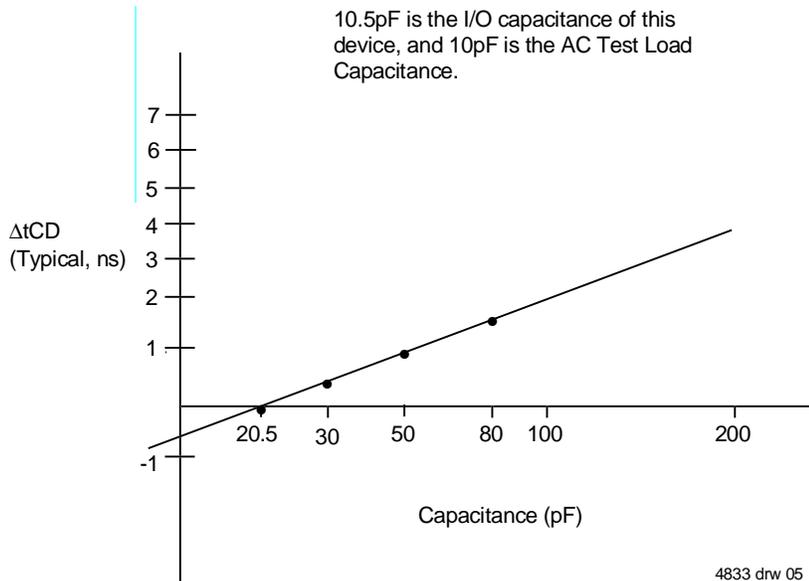|	
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4833 tbl 10
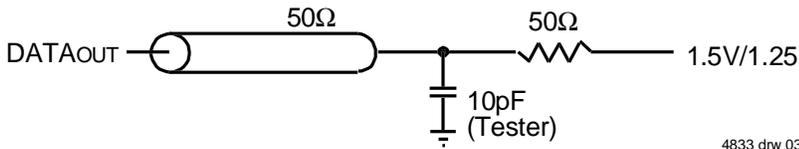
Figure 1. AC Output Test load.

Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

10.5pF is the I/O capacitance of this device, and 10pF is the AC Test Load Capacitance.

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[1,2]
### (V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

Symbol	Parameter	70V3379S4 Com'l Only		70V3379S5 Com'l & Ind		70V3379S6 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC2}	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t_{CL2}	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HA}	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SC}	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HC}	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SB}	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HB}	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SD}	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HD}	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t_{OE} [1]	Output Enable to Data Valid	—	4	—	5	—	6	ns
t_{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t_{CD2}	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t_{CKHZ}	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t_{CKLZ}	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
t_{CO}	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4833 tbl 11

NOTES:
1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$).
2. These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation[2]

4833 drw 06
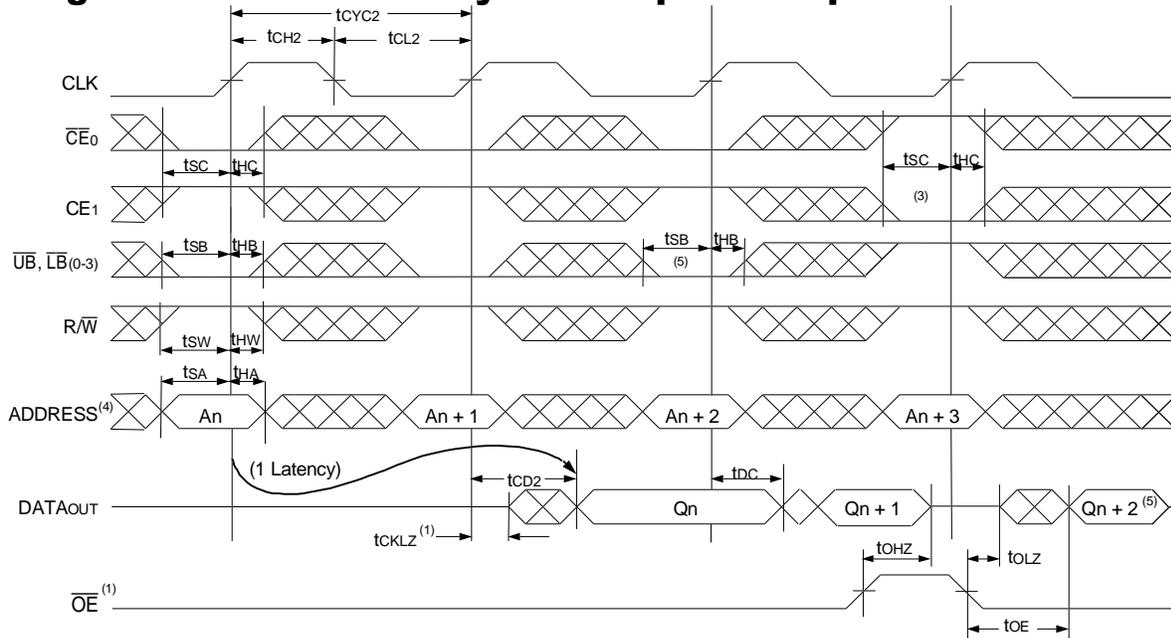
NOTES:
1. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{UB}$, $\overline{LB}$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the appropriate Byte of DATA$_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).

Timing Waveform of a Multi-Device Pipelined Read[1,2]
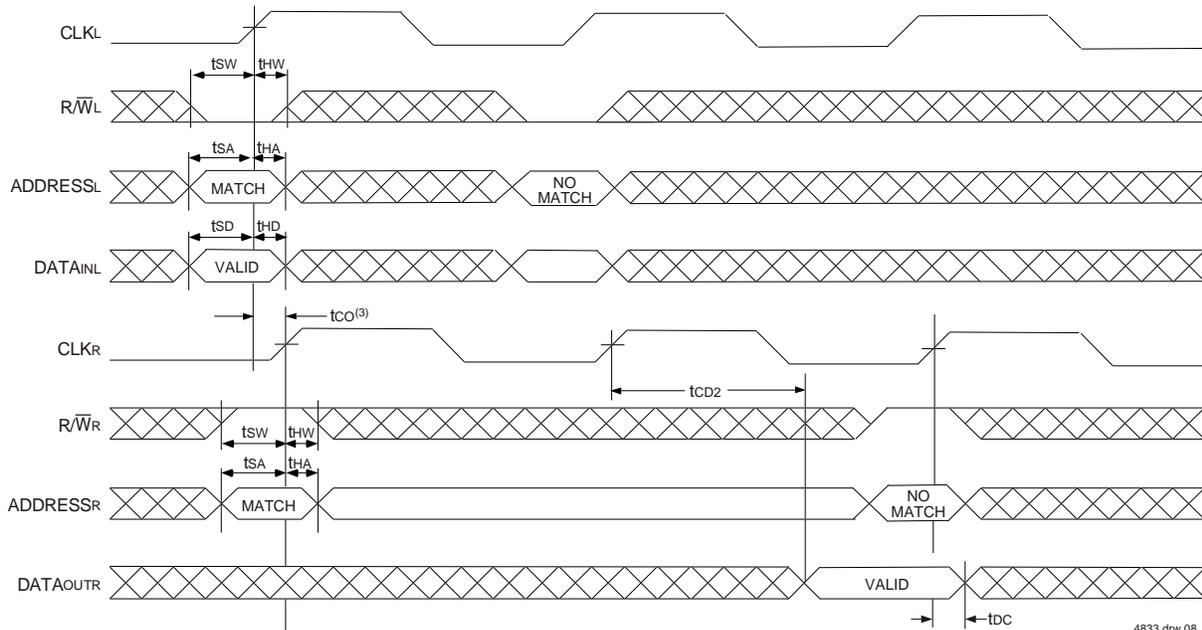

4833 drw 07
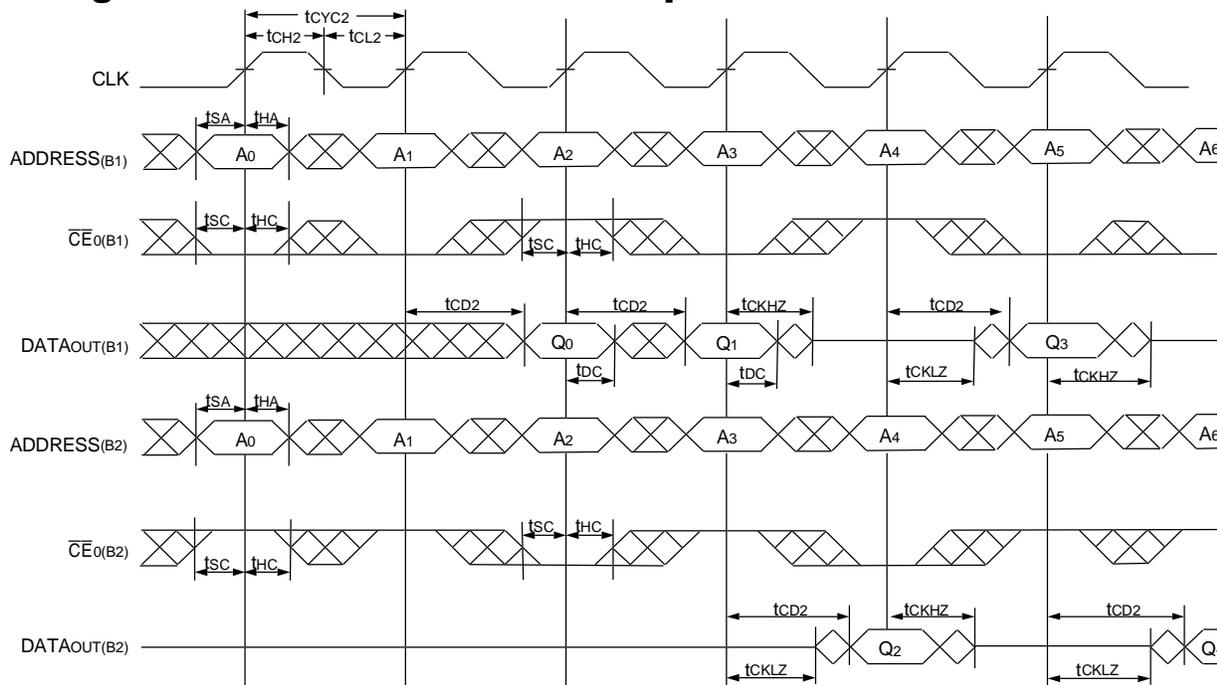
NOTES:
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3379 for this waveform, and are setup for depth expansion in this example. ADDRESS$_{(B1)}$ = ADDRESS$_{(B2)}$ in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
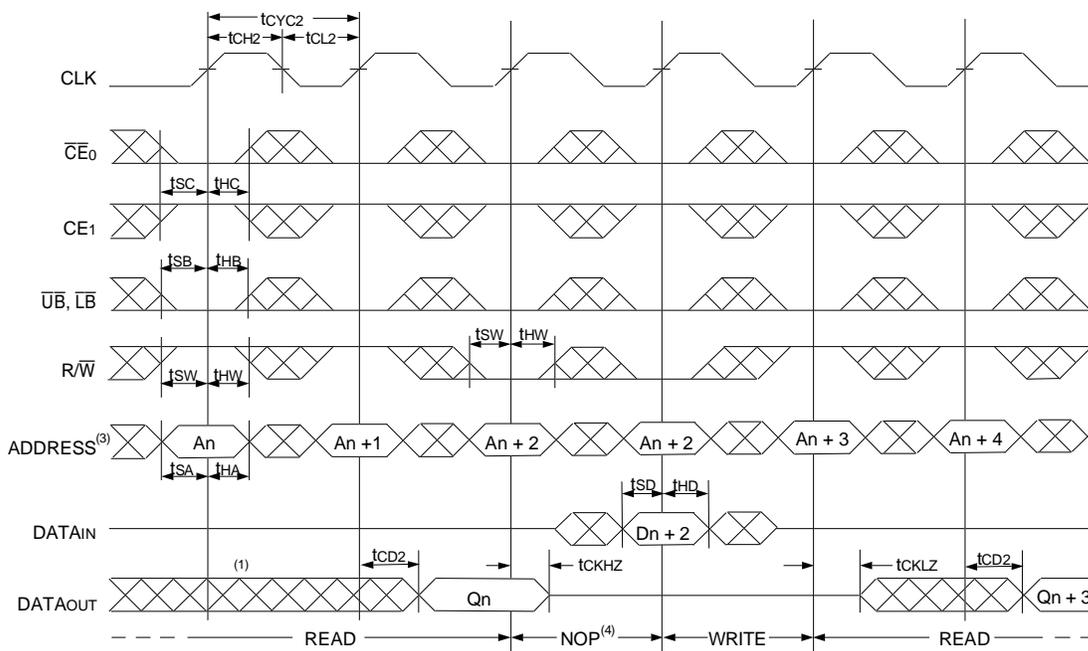
Timing Waveform of Left Port Write to Pipelined Right Port Read[1,2]

CLKL

tSW tHW

R/$\overline{W}$L

tSA tHA

ADDRESSL   MATCH   NO MATCH

tSD tHD

DATAINL   VALID

tCO[3]

CLKR

tCD2

R/$\overline{W}$R

tSW tHW

tSA tHA

ADDRESSR   MATCH   NO MATCH

DATAOUTR   VALID

tDC

4833 drw 08

NOTES:
1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V$_{IL}$; CE$_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V$_{IH}$.
2. $\overline{OE}$ = V$_{IL}$ for the Right Port, which is being read from. $\overline{OE}$ = V$_{IH}$ for the Left Port, which is being written to.
3. If t$_{CO}$ ≤ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be t$_{CO}$ + 2 t$_{CYC2}$ + t$_{CD2}$). If t$_{CO}$ > minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be t$_{CO}$ + t$_{CYC}$ + t$_{CD2}$).

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V$_{IL}$)[2]

tCYC2

tCH2 tCL2

CLK

$\overline{CE}_0$

tSC tHC

CE$_1$

tSB tHB

$\overline{UB}$, $\overline{LB}$

tSW tHW

R/$\overline{W}$

tSW tHW

ADDRESS[3]   An   An +1   An + 2   An + 2   An + 3   An + 4

tSA tHA

tSD tHD

DATAIN   Dn + 2

tCD2   tCKHZ   tCKLZ tCD2

DATAOUT   (1)   Qn   Qn + 3

READ   NOP[4]   WRITE   READ

4833 drw 09

NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V$_{IL}$; CE$_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V$_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V$_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[2]
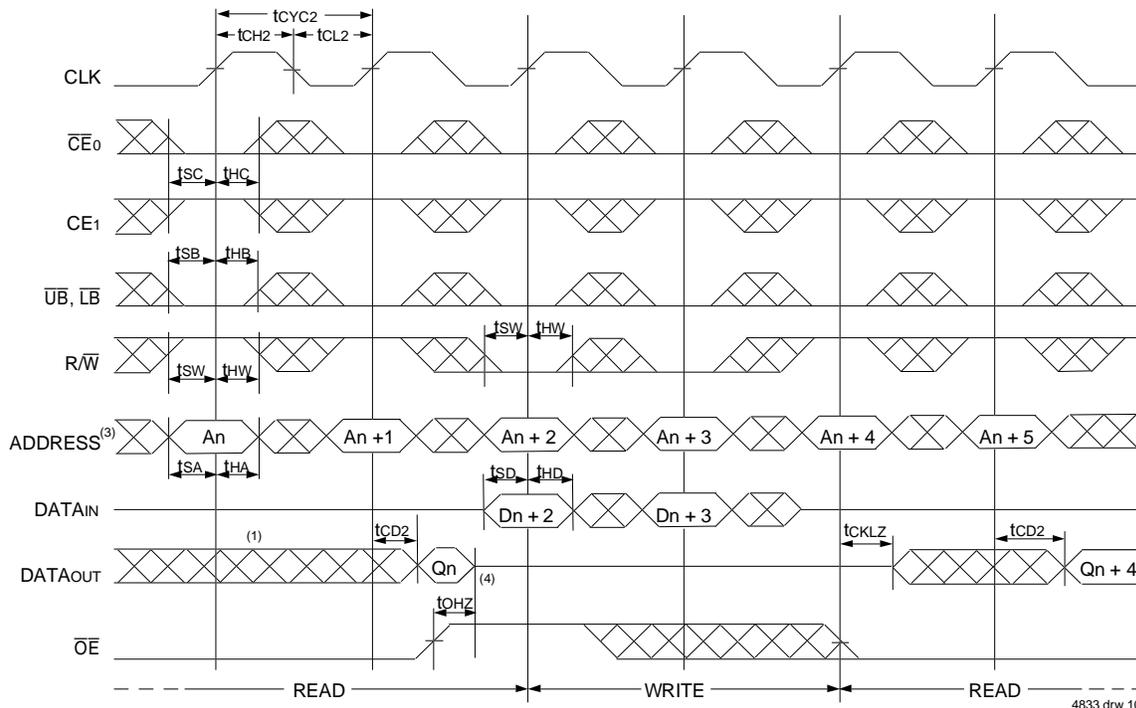
4833 drw 10

NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V$_{IL}$; CE$_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V$_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V$_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.
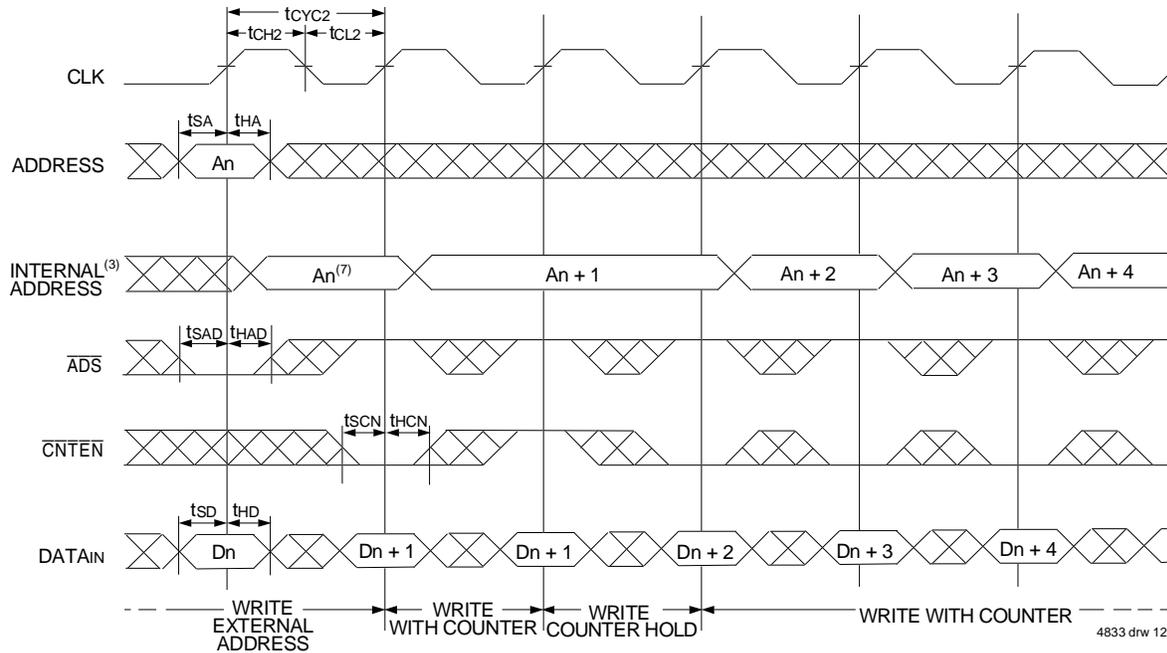
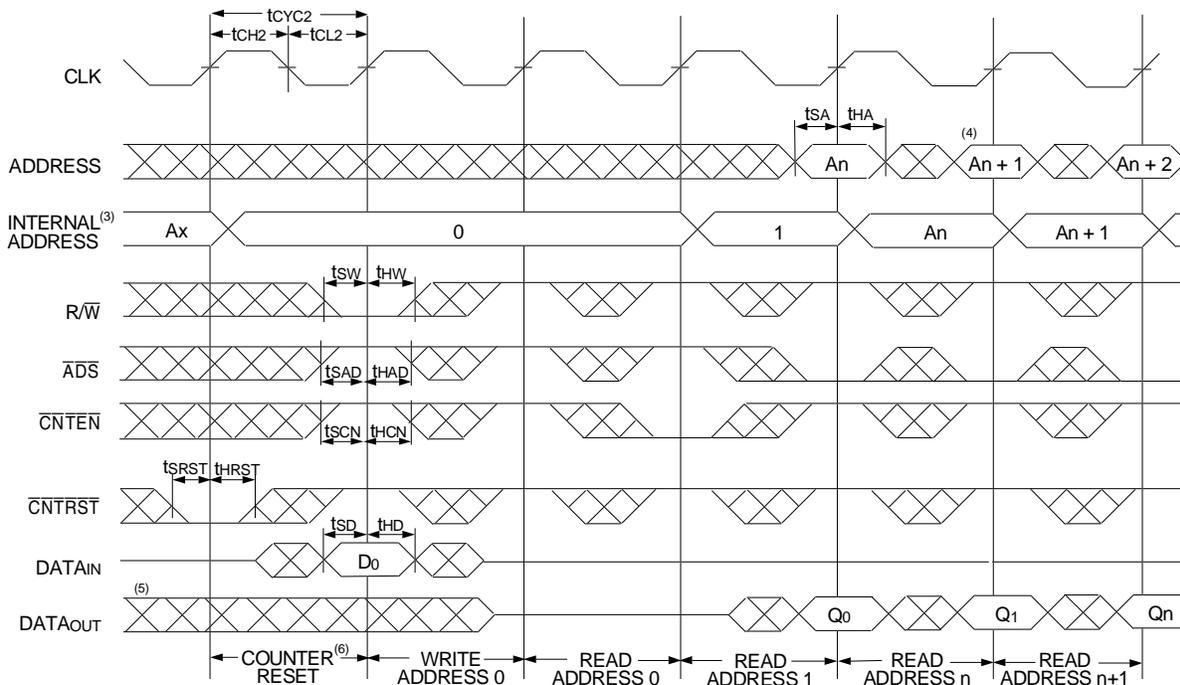# Timing Waveform of Pipelined Read with Address Counter Advance[1]

4833 drw 11
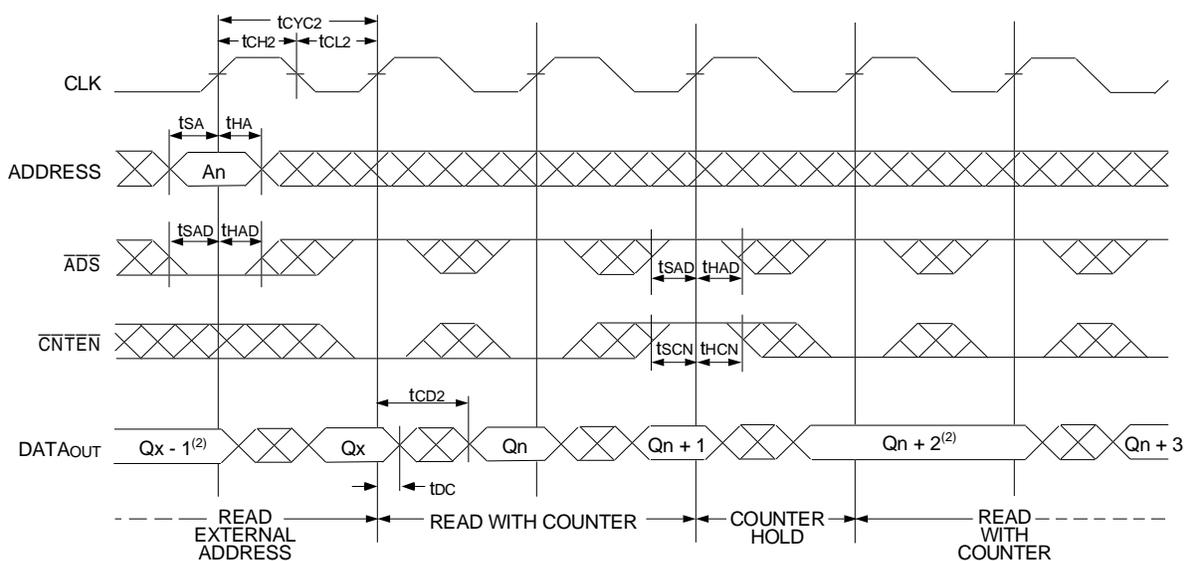
NOTES:
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ = V$_{IL}$; CE$_1$, R/$\overline{W}$, and $\overline{CNTRST}$ = V$_{IH}$.
2. If there is no address change via $\overline{ADS}$ = V$_{IL}$ (loading a new address) or $\overline{CNTEN}$ = V$_{IL}$ (advancing the address), i.e. $\overline{ADS}$ = V$_{IH}$ and $\overline{CNTEN}$ = V$_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance[1]

CLK

t_{CYC2}
t_{CH2} t_{CL2}

ADDRESS

t_{SA} t_{HA}
An

INTERNAL[3] ADDRESS

An[7]   An + 1   An + 2   An + 3   An + 4

$\overline{ADS}$

t_{SAD} t_{HAD}

$\overline{CNTEN}$

t_{SCN} t_{HCN}

DATA_IN

t_{SD} t_{HD}
Dn   Dn + 1   Dn + 1   Dn + 2   Dn + 3   Dn + 4

WRITE EXTERNAL ADDRESS   WRITE WITH COUNTER   WRITE COUNTER HOLD   WRITE WITH COUNTER

4833 drw 12

Timing Waveform of Counter Reset[2]

CLK

t_{CYC2}
t_{CH2} t_{CL2}

ADDRESS

t_{SA} t_{HA}
(4)
An   An + 1   An + 2

INTERNAL[3] ADDRESS

Ax   0   1   An   An + 1

R/$\overline{W}$

t_{SW} t_{HW}

$\overline{ADS}$

t_{SAD} t_{HAD}

$\overline{CNTEN}$

t_{SCN} t_{HCN}

$\overline{CNTRST}$

t_{SRST} t_{HRST}

DATA_IN

t_{SD} t_{HD}
D0

DATA_OUT

(5)
Q0   Q1   Qn

COUNTER RESET[6]   WRITE ADDRESS 0   READ ADDRESS 0   READ ADDRESS 1   READ ADDRESS n   READ ADDRESS n+1

4833 drw 13

NOTES:
1. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_IL; CE_1 and $\overline{CNTRST}$ = V_IH.
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ = V_IL; CE_1 = V_IH.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_IL and equals the counter output when $\overline{ADS}$ = V_IH.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_IL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: A_DDR 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_IL advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

Functional Description

The IDT70V3379 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3379s for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3379 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3379 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.
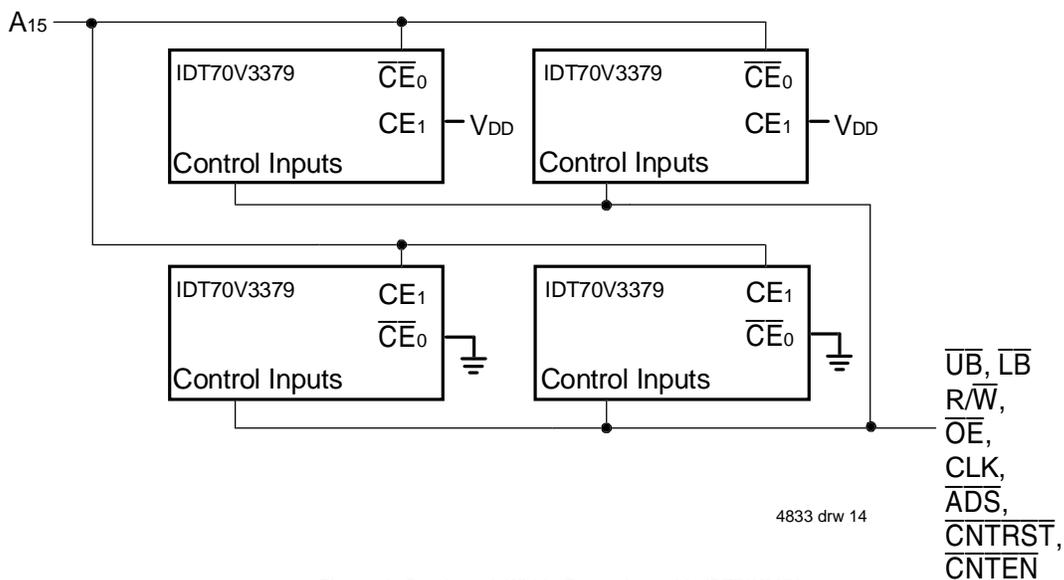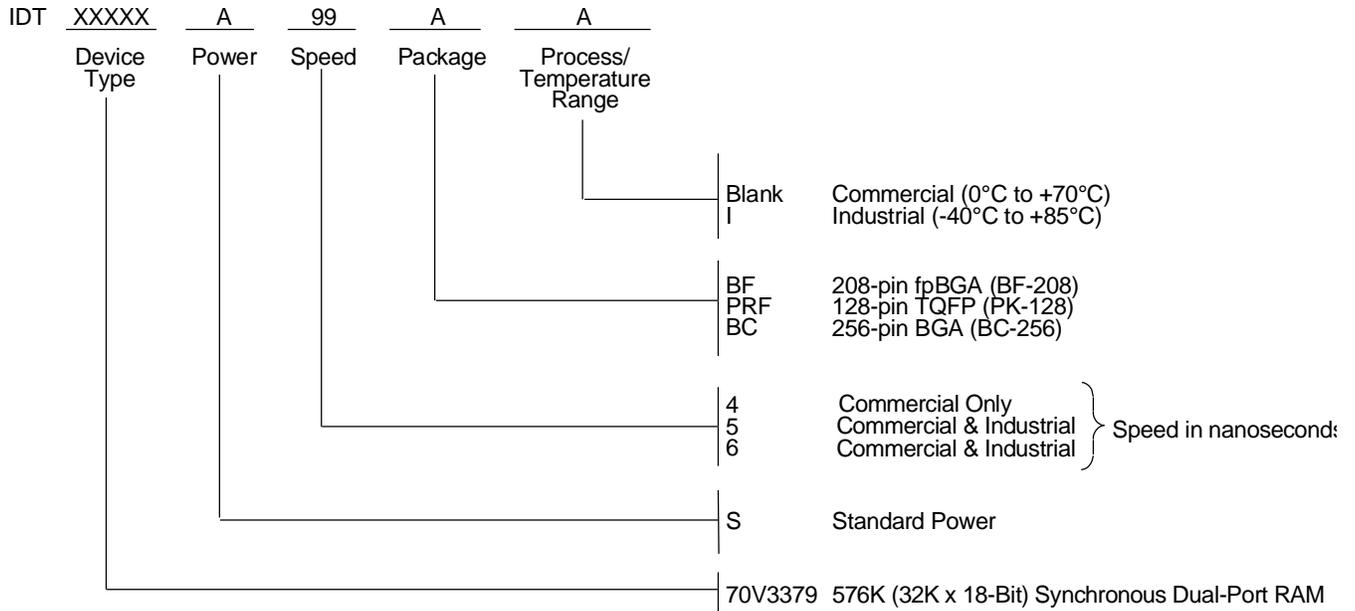

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Figure 4. Depth and Width Expansion with IDT70V3379

Ordering Information

```
IDT   XXXXX     A     99     A       A
      Device  Power  Speed  Package  Process/
      Type                           Temperature
                                     Range
```

Blank	Commercial (0°C to +70°C)	
I	Industrial (-40°C to +85°C)	

BF	208-pin fpBGA (BF-208)	
PRF	128-pin TQFP (PK-128)	
BC	256-pin BGA (BC-256)	

4	Commercial Only	
5	Commercial & Industrial	Speed in nanoseconds
6	Commercial & Industrial	

S	Standard Power

70V3379	576K (32K x 18-Bit) Synchronous Dual-Port RAM

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Datasheet Document History

1/18/98:	Initial Public Release	
3/15/99:	Page 10	Additional Notes
4/28/99:	Added fpBGA package	
6/8/99:	Page 2	Changed package body height from 1.5mm to 1.4mm
6/11/99:	Page 5	Deleted note 6 for Table II
7/14/99:	Page 2	Corrected pin to T3 to V_{DDQL}
8/4/99:	Page 6 Improved power numbers	
10/4/99:	Upgraded speed to 133MHz, added 2.5V I/O capability	
11/12/99:	Replaced IDT logo	
2/28/00:	Added new BGA package, added full 2.5V interface capability	
5/1/00:	Page 2	Added ball pitch
	Page 3	Renamed pins
	Page 6	Made corrections to Truth Table
	Page 9	Changed Ω numbers in figure 2
6/7/00:	Page 4	Added information to pin and pin notes
	Page 6	Increated storage temperature parameter
		Clarified T_A Parameter
	Page 8	DC Electrical parameters–changed wording from "open" to "disabled"
		Removed note 7 on DC Electrical Characteristics table
1/10/01:	Page 1	Changed 64K to 32K in block drawing
	Removed Preliminary status	
4/10/01:	Added Industrial Temperature Ranges and removed related notes	