

100156



Not Intended For New Designs

T-46-07-01

100156 Mask-Merge/Latch

General Description

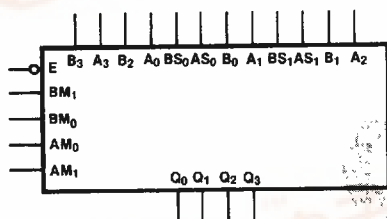
The 100156 merges two 4-bit words to form a 4-bit output word. The AM_n enable allows the merge of A into B by one, two or three places (per the AS_n value) from the left. The BM_n enable similarly allows the merge of B into A from the left (per the BS_n value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is

equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable ($\bar{E}$) input. All inputs have a 50 k Ω (typical) pull-down resistor tied to V_{EE} .

Ordering Code: See Section 6

Logic Symbol



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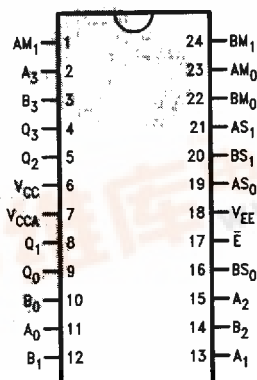
Pin Names	Description
$\bar{E}$	Latch Enable Input (Active LOW)
A_0-A_3	A Data Inputs
B_0-B_3	B Data Inputs
AM_0, AM_1	A Merge Enable Inputs
BM_0, BM_1	B Merge Enable Inputs
AS_0, AS_1	A Address Inputs
BS_0, BS_1	B Address Inputs
Q_0-Q_3	Data Outputs

Note:

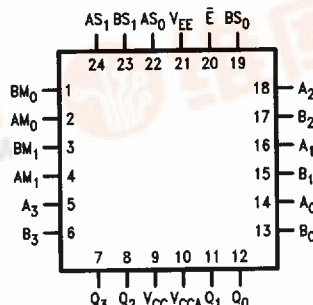
When $\bar{E}$ is HIGH, Q_n outputs do not change.
When $\bar{E}$ is LOW, $Q_n = A$ or B depending on which is selected.

Connection Diagrams

24-Pin DIP

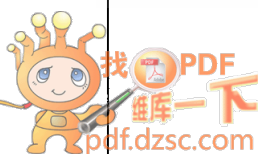


24-Pin Quad Cerpak

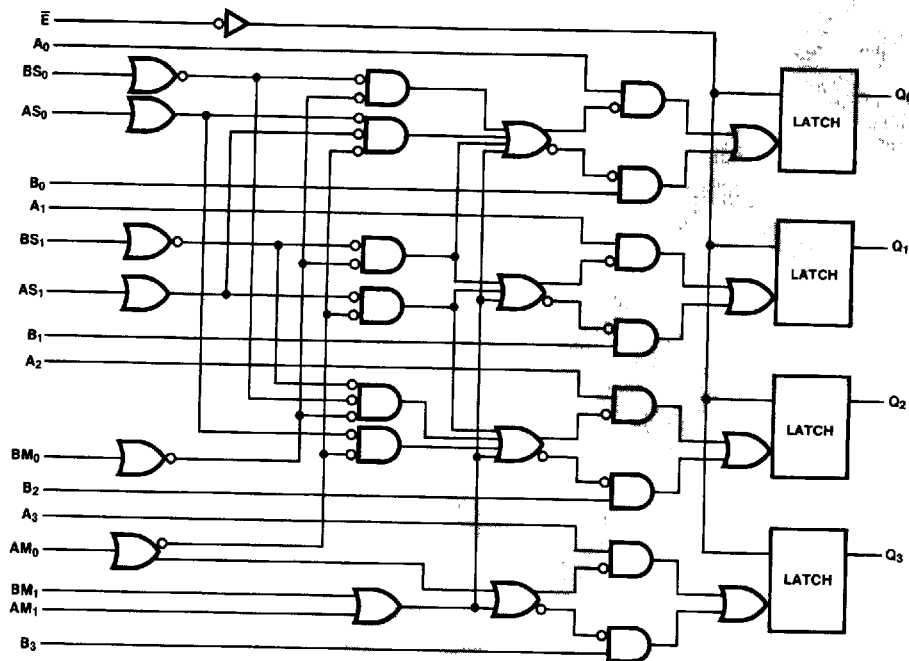


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Logic Diagram



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Truth Table

Inputs									Outputs				Remarks
Merge Enables				Addresses				E					
BM ₁	BM ₀	AM ₁	AM ₀	BS ₁	BS ₀	AS ₁	AS ₀		Q ₀	Q ₁	Q ₂	Q ₃	
X	X	H	X	X	X	X	X	L	B ₀	B ₁	B ₂	B ₃	Select B
H	X	X	X	X	X	X	X	L	B ₀	B ₁	B ₂	B ₃	
L	L	L	L	X	X	X	X	L	A ₀	A ₁	A ₂	A ₃	Select A
L	L	L	H	X	X	L	L	L	B ₀	B ₁	B ₂	B ₃	Merge A → B
L	L	L	H	X	X	L	H	L	A ₀	B ₁	B ₂	B ₃	
L	L	L	H	X	X	H	L	L	A ₀	A ₁	B ₂	B ₃	
L	L	L	H	X	X	H	H	L	A ₀	A ₁	A ₂	B ₃	
L	H	L	L	L	L	X	X	L	A ₀	A ₁	A ₂	A ₃	Merge B → A
L	H	L	L	L	H	X	X	L	B ₀	A ₁	A ₂	A ₃	
L	H	L	L	L	L	X	X	L	B ₀	B ₁	A ₂	A ₃	
L	H	L	L	H	H	X	X	L	B ₀	B ₁	B ₂	A ₃	
L	H	L	H	L	L	L	H	L	A ₀	B ₁	B ₂	B ₃	Merge A → B
L	H	L	H	L	L	H	L	L	A ₀	A ₁	B ₂	B ₃	
L	H	L	H	L	L	H	H	L	A ₀	A ₁	A ₂	B ₃	
L	H	L	H	L	H	H	H	L	B ₀	A ₁	B ₂	B ₃	Merge A → B then Merge B → A
L	H	L	H	L	H	H	H	L	B ₀	A ₁	A ₂	B ₃	
L	H	L	H	H	L	H	H	L	B ₀	B ₁	A ₂	B ₃	
L	H	L	H	H	H	H	H	L	B ₀	B ₁	B ₂	B ₃	B Address ≥ A Address
L	H	L	H	H	H	H	L	L	B ₀	B ₁	B ₂	B ₃	
L	H	L	H	H	H	L	H	L	B ₀	B ₁	B ₂	B ₃	
L	H	L	H	H	H	L	L	L	B ₀	B ₁	B ₂	B ₃	
L	H	L	H	H	H	L	L	L	B ₀	B ₁	B ₂	B ₃	
L	H	L	H	H	L	L	H	L	B ₀	B ₁	B ₂	B ₃	
L	H	L	H	H	L	L	L	L	B ₀	B ₁	B ₂	B ₃	
L	H	L	H	L	L	L	L	L	B ₀	B ₁	B ₂	B ₃	
X	X	X	X	X	X	X	X	H	Q ₀	Q ₁	Q ₂	Q ₃	Latch
Before Start	At Start	After End	At End										

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C)

0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin

-7.0V to $+0.5\text{V}$

Input Voltage (DC)

V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH)

-50mA

Operating Range (Note 2)

-5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810	−1705	−1620			
V _{OHC}	Output HIGH Voltage	−1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1020		−870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810		−1605			
V _{OHC}	Output HIGH Voltage	−1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1595			
V _{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1035		−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1830		−1620			
V _{OHC}	Output HIGH Voltage	−1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

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DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current $A_n, B_n, BM_n, AM_n, BS_n, AS_n, \bar{E}$			265	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-235	-161	-107	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.90	0.50	1.80	0.50	2.00	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}$ to Outputs	1.00	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.80	0.45	1.90	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.80 2.90		0.80 2.90		0.80 2.90		ns	Figure 3
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.10 0.80		2.10 0.80		2.10 0.80		ns	
$t_{pw(L)}$	Pulse Width LOW $\bar{E}$	2.00		2.00		2.00		ns	

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.70	0.50	1.60	0.50	1.80	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}$ to Outputs	1.00	2.30	1.00	2.20	1.00	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.50	1.20	3.50	1.20	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.70 2.80		0.70 2.80		0.70 2.80		ns	Figure 3
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.00 0.70		2.00 0.70		2.00 0.70		ns	
$t_{pw(L)}$	Pulse Width LOW $\bar{E}$	2.00		2.00		2.00		ns	



Notes:
 $V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
Decoupling $0.1\ \mu F$ from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3\ pF$
Pin numbers shown are for flatpak; for DIP see logic symbol



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FIGURE 3. Data Setup and Hold Times