EMIF03-SIM01F2

3 LINES EMI FILTER INCLUDING ESD PROTECTION

IPAD™

MAIN PRODUCT APPLICATIONS:

EMI filtering and ESD protection for:

- SIM Interface (Subscriber Identify Module)
- UIM Interface (Universal Identify Module)

DESCRIPTION

The EMIF03-SIM01F2 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF03 flip chip packaging means the package size is equal to the die size.
This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

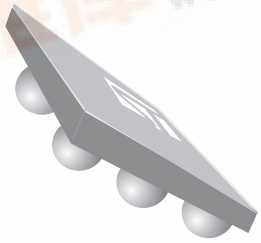
BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming: 1.42mm x 1.42mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2
Level 4 15kV (air discharge)
8kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3



Flip-Chip (8 Bumps)

Table 1: Order Code

Part Number	Marking
EMIF03-SIM01F2	FC

Figure 1: Pin Configuration (Ball side)

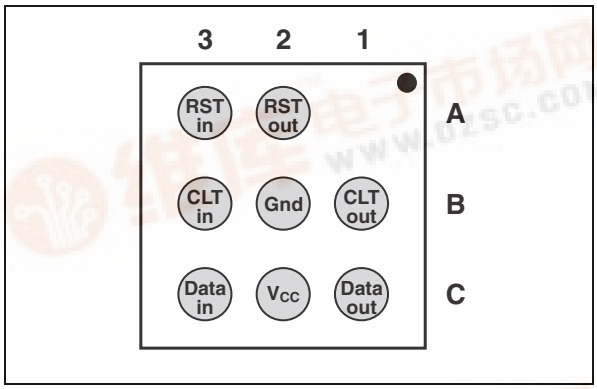
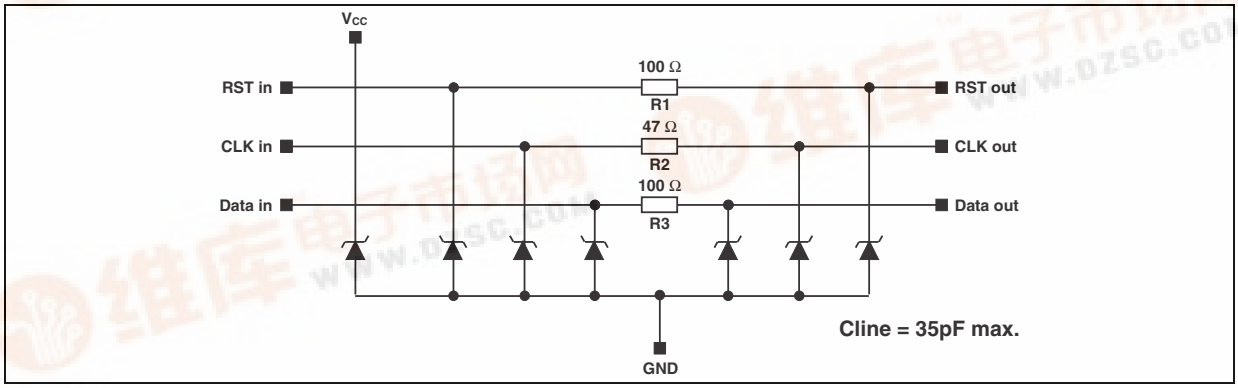


Figure 2: Configuration



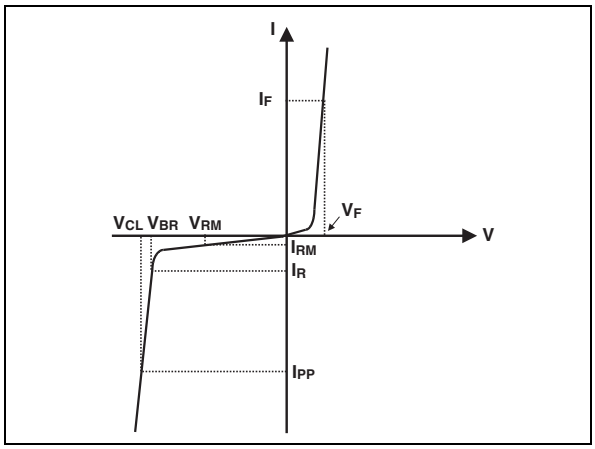
TM: IPAD is a trademark of STMicroelectronics.

Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3V per line			1	µA
R_d			1.5		Ω
R_1		95	100	105	Ω
R_2		44.65	47	49.35	Ω
R_3		95	100	105	Ω
C_{line}	@ 0V			35	pF

Figure 3: S21 (dB) attenuation measurement

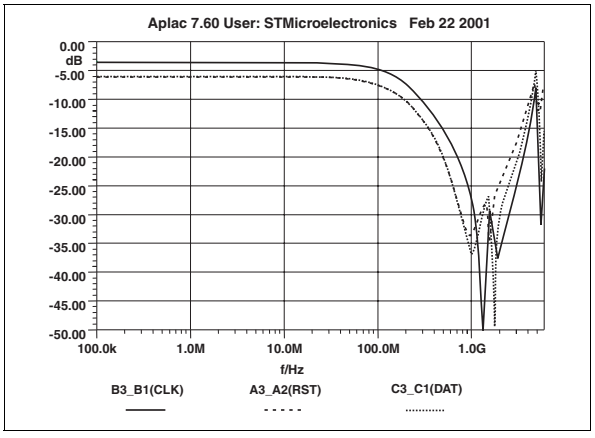


Figure 4: Analog crosstalk measurements

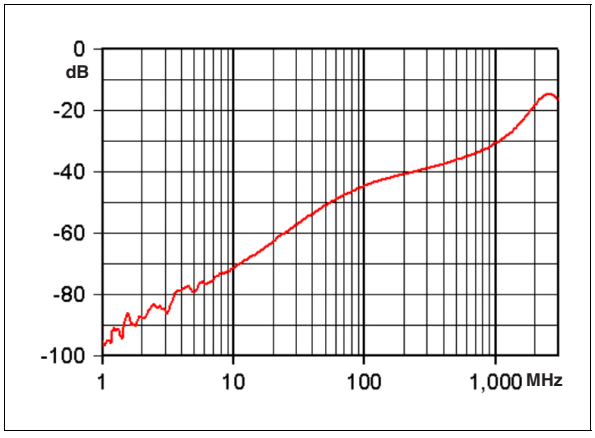


Figure 5: Digital crosstalk measurement

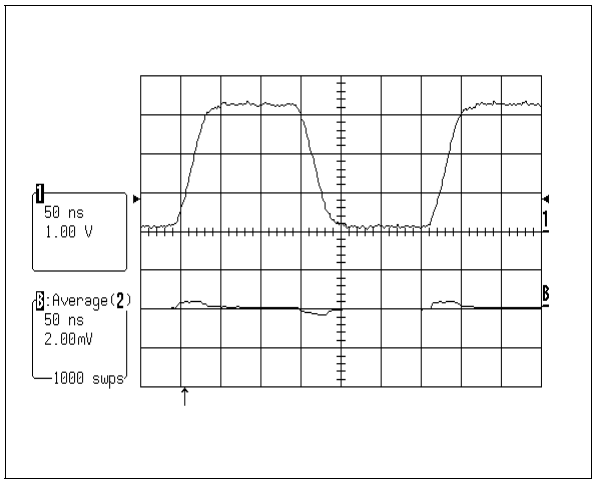


Figure 6: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

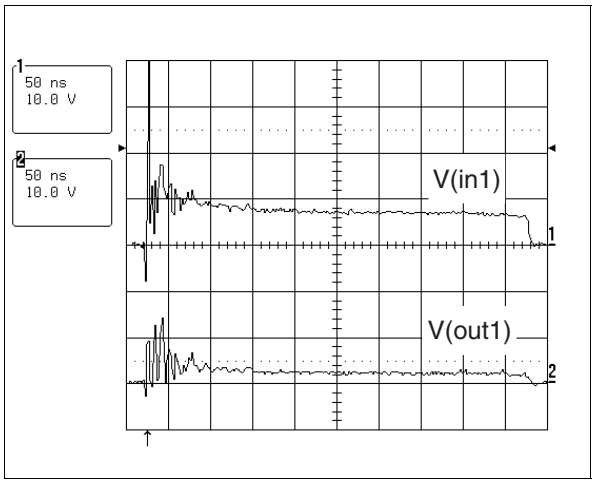


Figure 7: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

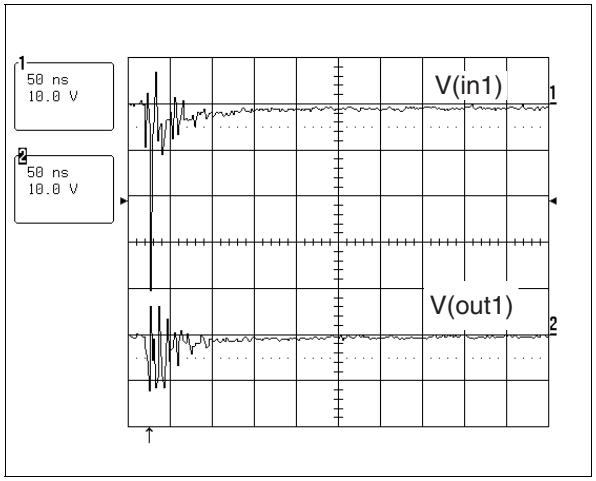


Figure 8: Line capacitance versus applied voltage (typical)

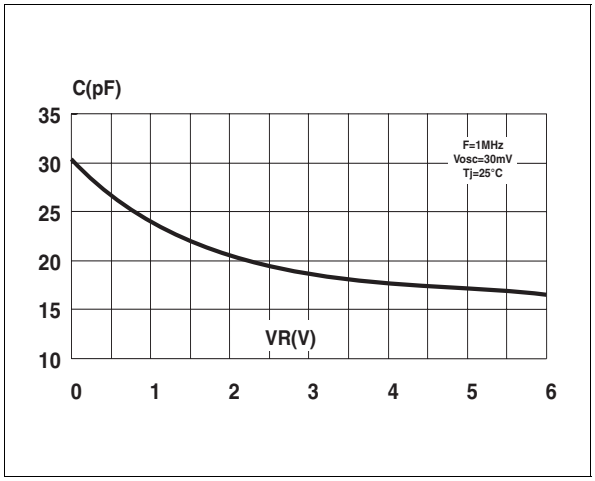


Figure 9: Aplac model

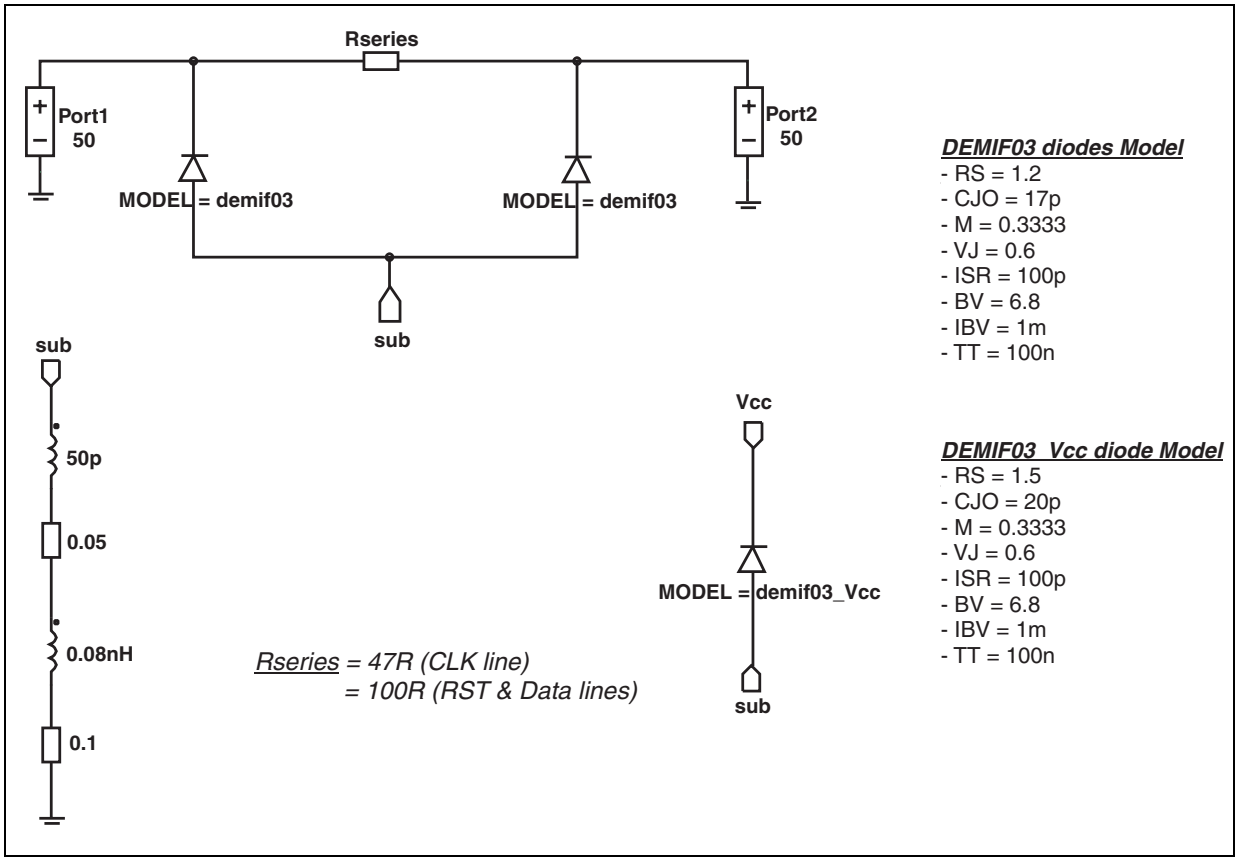


Figure 10: Ordering Information Scheme

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm
= 3: Leadfree Pitch = 400µm, Bump = 250µm

Figure 11: FLIP-CHIP Package Mechanical Data

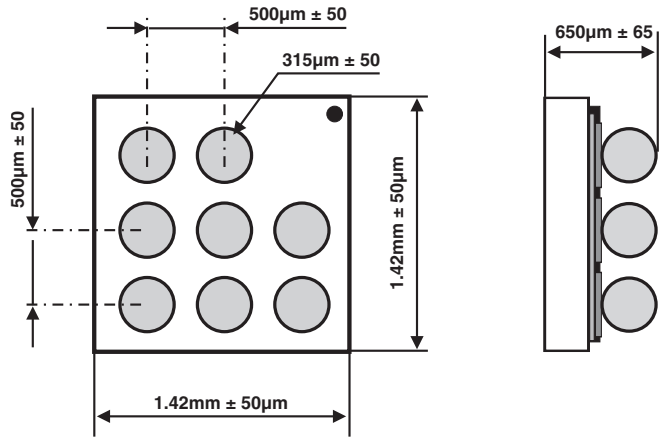


Figure 12: Foot print recommendations

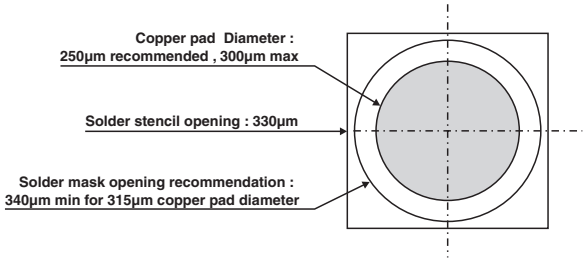


Figure 13: Marking

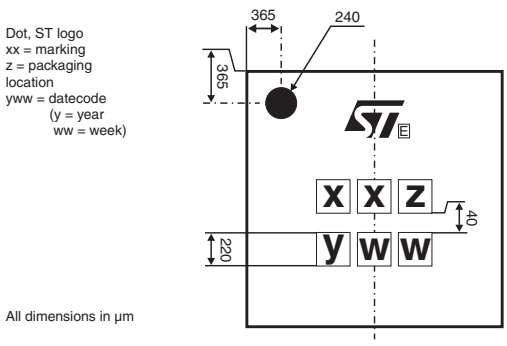


Figure 14: FLIP-CHIP Tape and Reel Specification

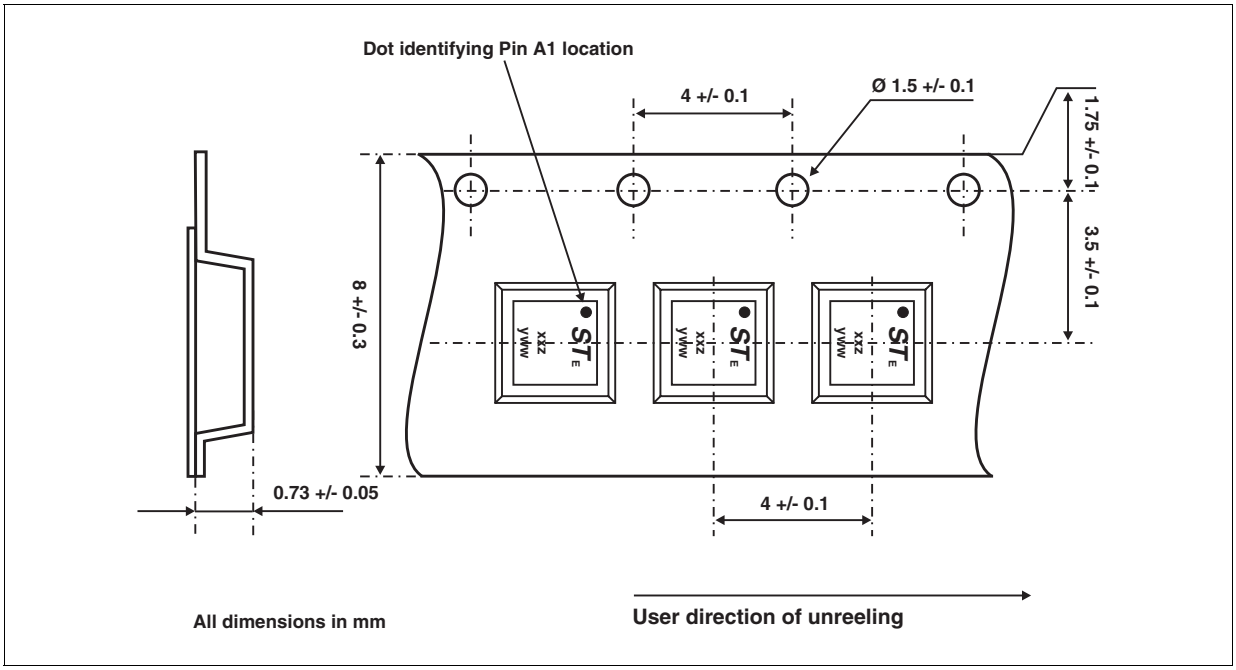


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM01F2	FC	Flip-Chip	2.9 mg	5000	Tape & reel 7”

Note: More informations are available in the application notes:
AN1235: “Flip-Chip: Package description and recommendations for use”
AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
08-Oct-2004	1	First issue
13-Dec-2204	2	Table 4 on page 6: Flip-Chip weight corrected from 3.3 mg to 2.9 mg.