AON2408
20V N-Channel MOSFET

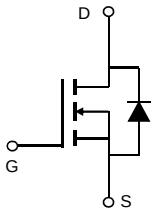
General Description

The AON2408 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

Features

V_{DS}	20V
I_D (at V_{GS}=4.5V)	8A
$R_{DS(ON)}$ (at V_{GS} =4.5V)	< 14.5mΩ
$R_{DS(ON)}$ (at V_{GS} =2.5V)	< 19mΩ

Green Product



Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [G]	T_A=25℃	I_D	8	A
	T_A=100℃		6	
Pulsed Drain Current [C]		I_{DM}	32	
Power Dissipation [A]	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	37	45	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		66	80	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	0.5	0.83	1.2	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	32			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=8A		11.6	14.5	mΩ
		T_J=125℃		16.3	20.5	
		V_{GS}=2.5V, I_D=4A		15	19	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.65	1	V
I_S	Maximum Body-Diode Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		782		pF
C_{oss}	Output Capacitance			158		pF
C_{rss}	Reverse Transfer Capacitance			98		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.4		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=8A		7		nC
Q_{gs}	Gate Source Charge			1		nC
Q_{gd}	Gate Drain Charge			2.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=4.5V, V_{DS}=10V, R_L=1.25Ω, R_{GEN}=3Ω		3		ns
t_r	Turn-On Rise Time			4.5		ns
$t_{D(off)}$	Turn-Off DelayTime			28		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8A, dI/dt=100A/µs		11		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8A, dI/dt=100A/µs		2.7		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

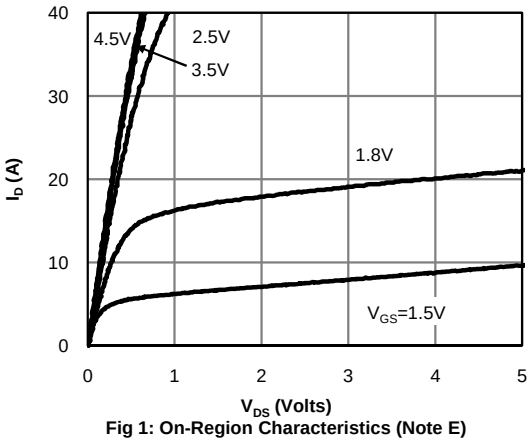


Fig 1: On-Region Characteristics (Note E)

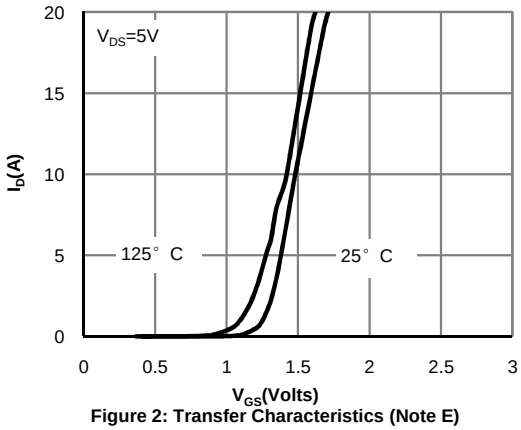


Figure 2: Transfer Characteristics (Note E)

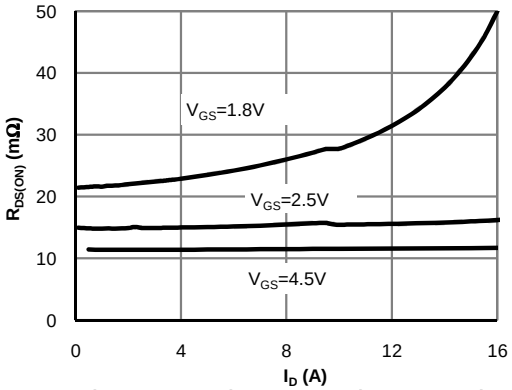


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

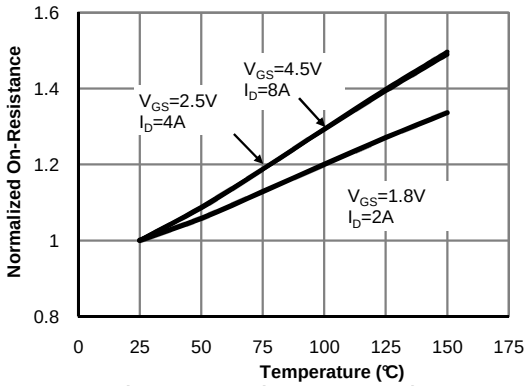


Figure 4: On-Resistance vs. Junction Temperature (Note E)

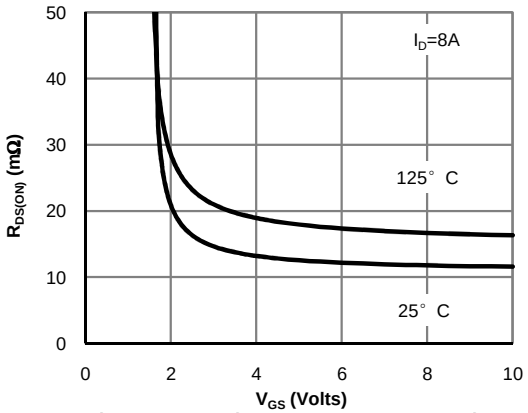


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

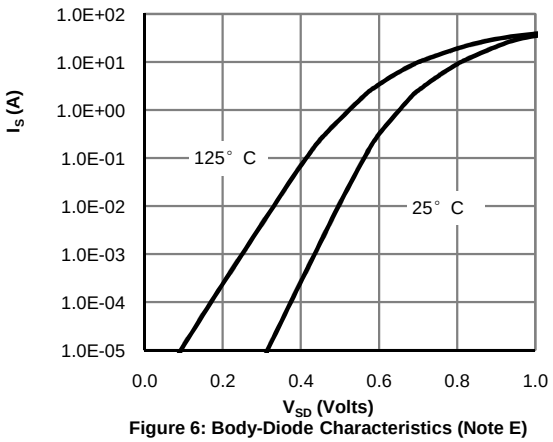


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

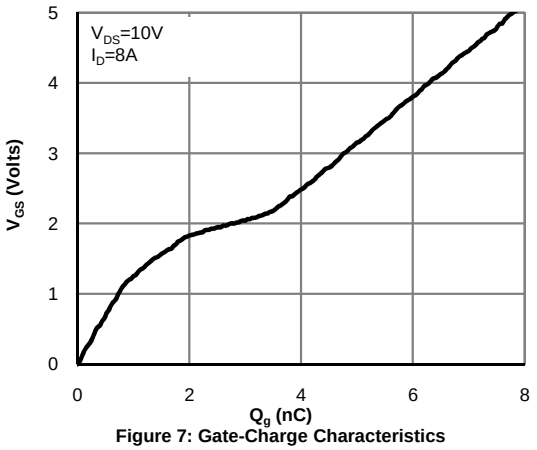


Figure 7: Gate-Charge Characteristics

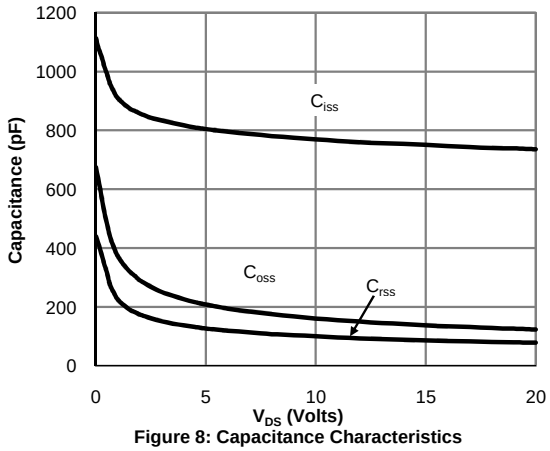


Figure 8: Capacitance Characteristics

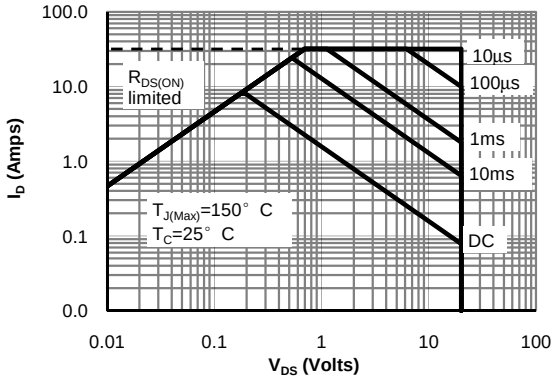


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

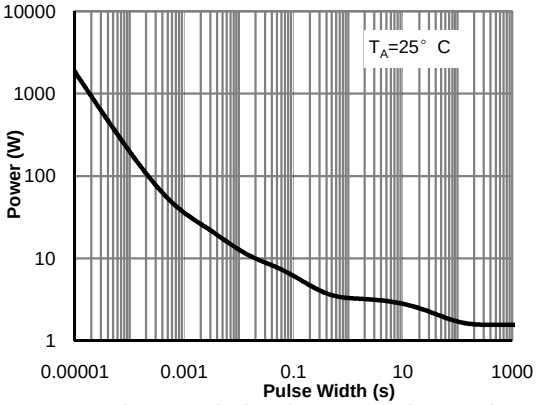


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note H)

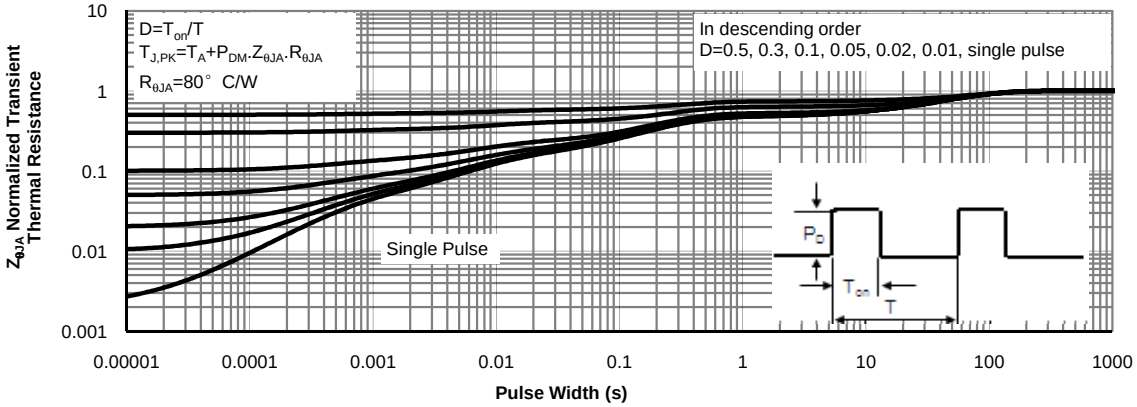
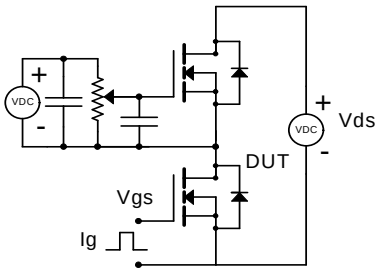
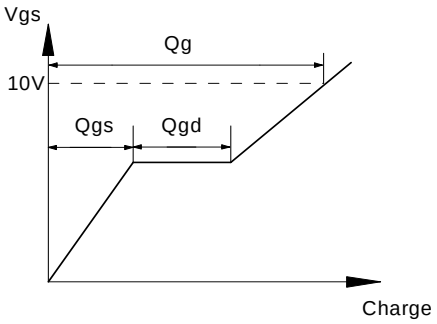


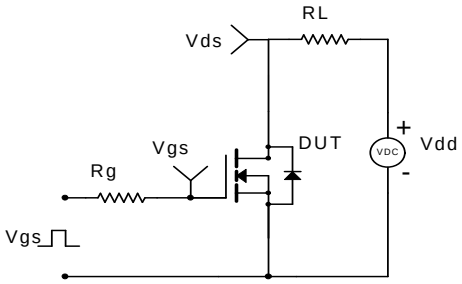
Figure 12: Normalized Maximum Transient Thermal Impedance (Note H)

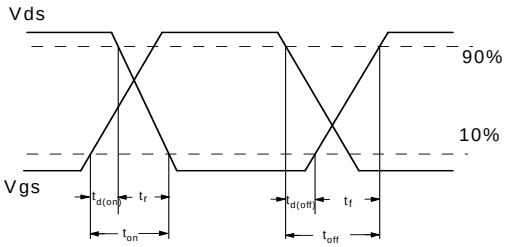
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms