

DATA SHEET

74ABT16841A

74ABTH16841A

20-bit bus interface latch (3-State)

Product specification
Supersedes data of 1995 Sep 28
IC23 Data Handbook

1998 Feb 27



20-bit bus interface latch (3-State)

74ABT16841A 74ABTH16841A

FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- 74ABTH16841A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16841A Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16841A consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{\text{nOE}}$) is Low. When $\overline{\text{nOE}}$ is High the output is in the High-impedance state.

Two options are available, 74ABT16841A which does not have the bus-hold feature and 74ABTH16841A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$	3.1 2.2	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	500	μA
I_{CCL}		Outputs LOW; $V_{\text{CC}} = 5.5\text{V}$	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16841A DL	BT16841A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16841A DGG	BT16841A DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16841A DL	BH16841A DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16841A DGG	BH16841A DGG	SOT364-1

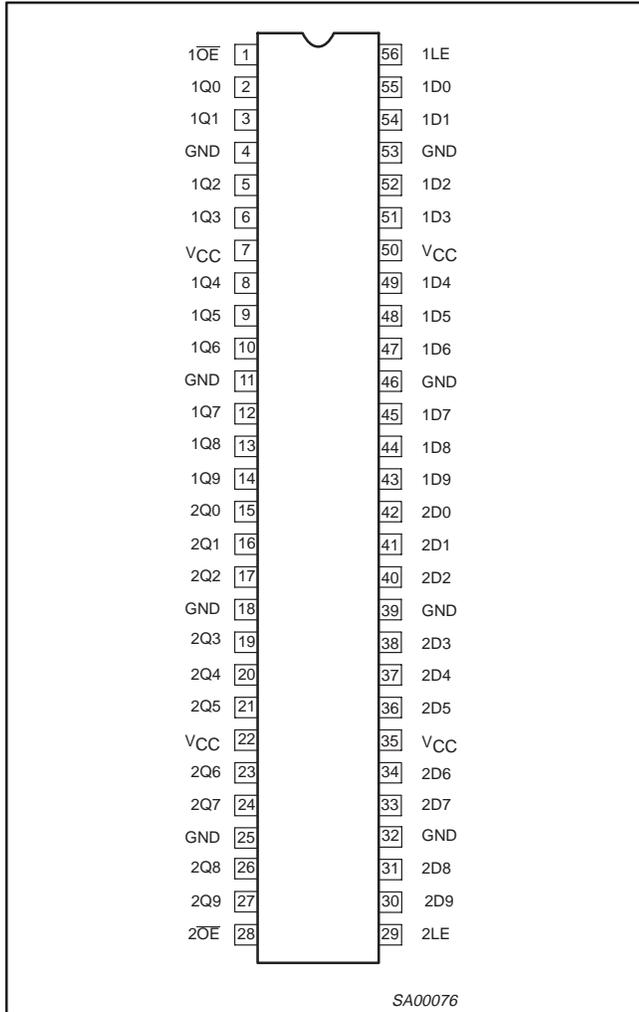
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 – 1D9 2D0 – 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
1, 28	$\overline{1\text{OE}}, \overline{2\text{OE}}$	Output enable inputs (active-Low)
56, 29	1LE, 2LE	Latch enable inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

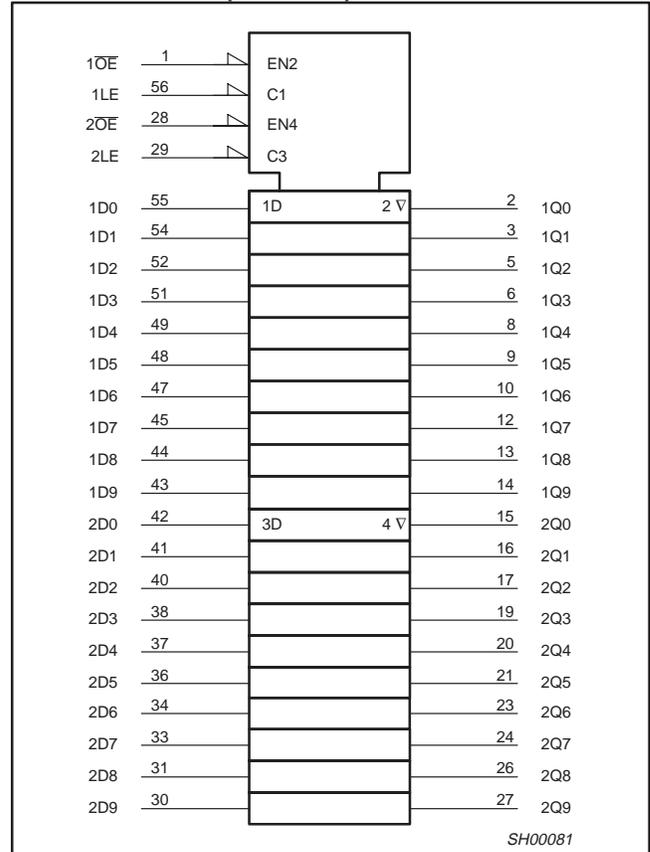
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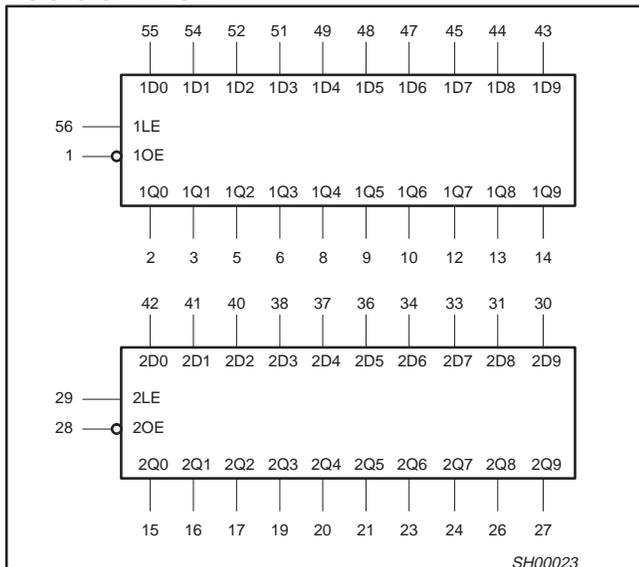
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
nOE	nLE	nDx	nQ0 – nQ9	
L	H	L	L	Transparent
L	H	H	H	
L	↓	l	L	Latched
L	↓	h	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low LE transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low LE transition
- ↓ = High-to-Low LE transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state

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74ABT16841A
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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current 74ABT16841A	V _{CC} = 5.5V; V _I = V _{CC} or GND		±0.01	±1		±1.0	µA
I _I	Input leakage current 74ABTH16841A	V _{CC} = 5.5V; V _I = V _{CC} or GND		±0.01	±1		±1	µA
		V _{CC} = 5.5V; V _I = V _{CC}		0.01	1		1	µA
		V _{CC} = 5.5V; V _I = 0		-2	-3		-5	µA
I _{HOLD}	Bus Hold current inputs ⁶ 74ABTH16841A	V _{CC} = 4.5V; V _I = 0.8V	35			35		µA
		V _{CC} = 4.5V; V _I = 2.0V	-75			-75		µA
		V _{CC} = 5.5V; V _I = 0 to 5.5V	±800					µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	µA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	µA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	10		10	µA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-10		-10	µA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-70	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	1		1	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		10	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	1		1	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.2	1		1	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay nDx to nQx	2	1.1	3.1	4.1	1.1	4.9	ns
			1.5	2.2	3.1	1.5	3.6	
t _{PLH} t _{PHL}	Propagation delay nLE to nQx	1	1.5	2.5	3.3	1.5	3.7	ns
			1.0	2.1	2.8	1.0	3.1	
t _{PZH} t _{PZL}	Output enable time to High and Low level	4	1.2	2.4	3.2	1.2	4.0	ns
			5	2.2	2.9	1.2	3.6	
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4	1.8	3.0	4.0	1.8	4.9	ns
			5	2.5	3.2	1.5	3.7	

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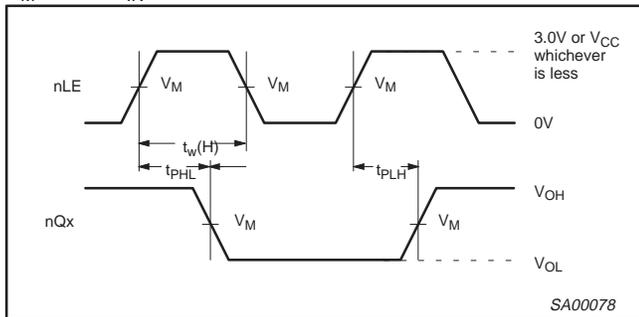
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

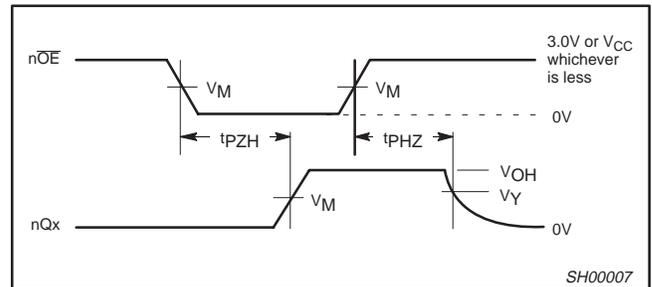
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nLE	3	2.0 1.0	1.0 0.4	2.0 1.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nLE	3	2.0 2.0	-0.3 -0.7	2.0 2.0		ns
$t_w(\text{H})$	nLE pulse width High	1	2.9	1.9	2.9		ns

AC WAVEFORMS

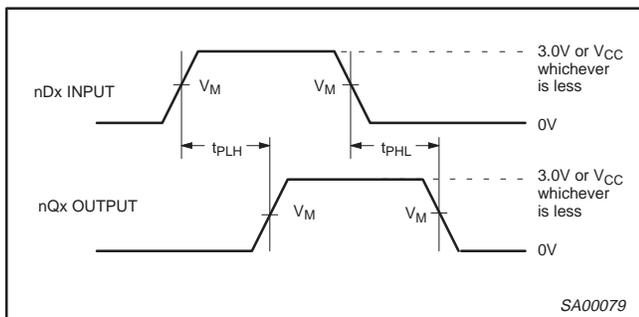
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



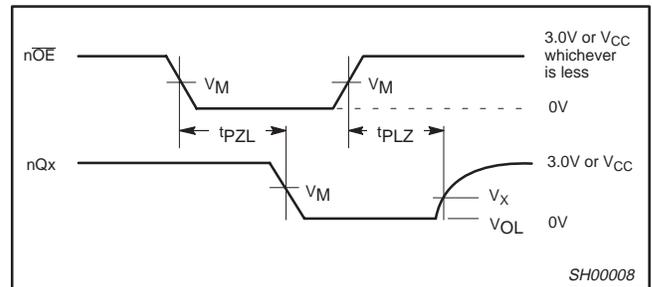
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



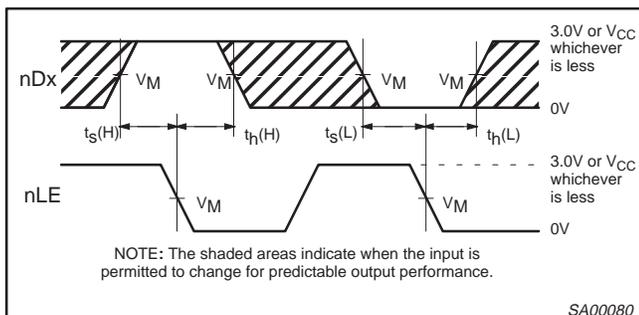
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Propagation Delay for Data to Outputs



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

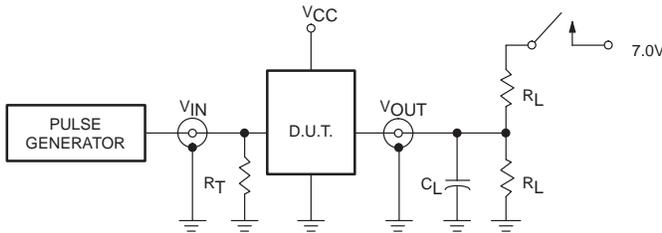


Waveform 3. Data Setup and Hold Times

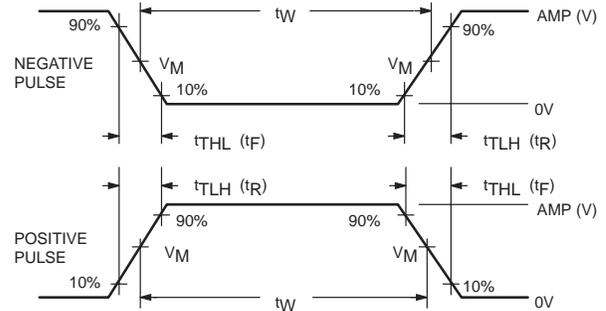
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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

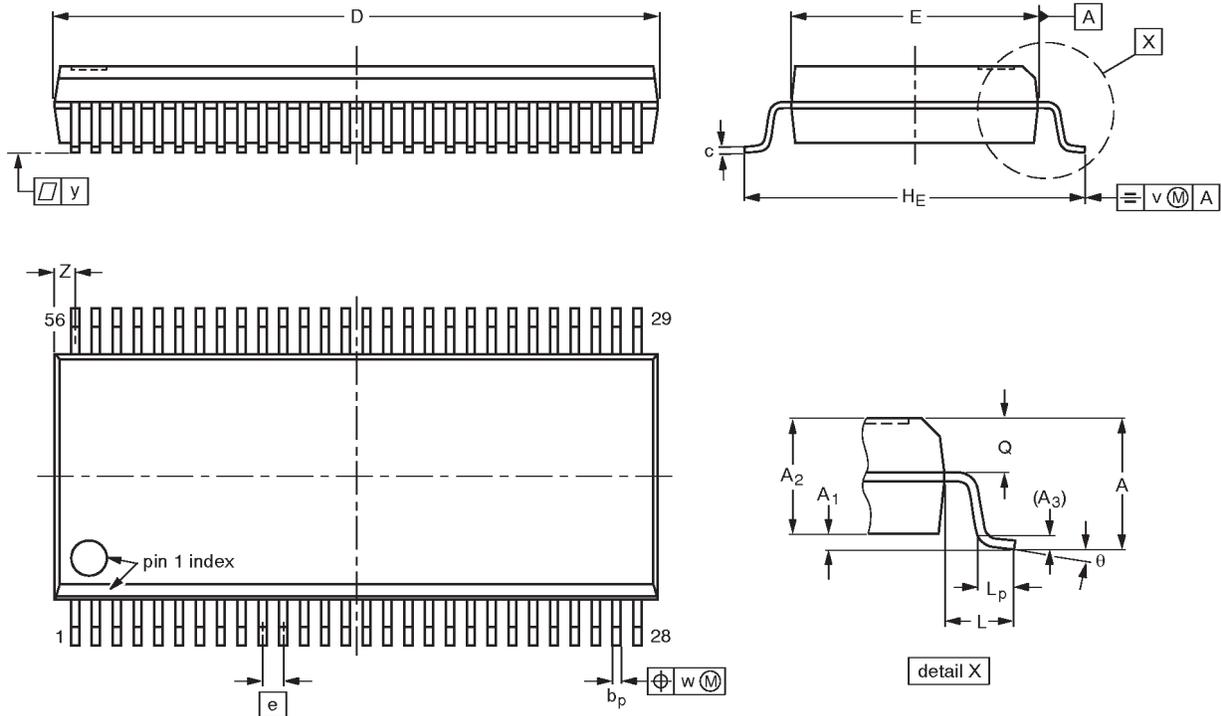
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

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74ABTH16841A

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

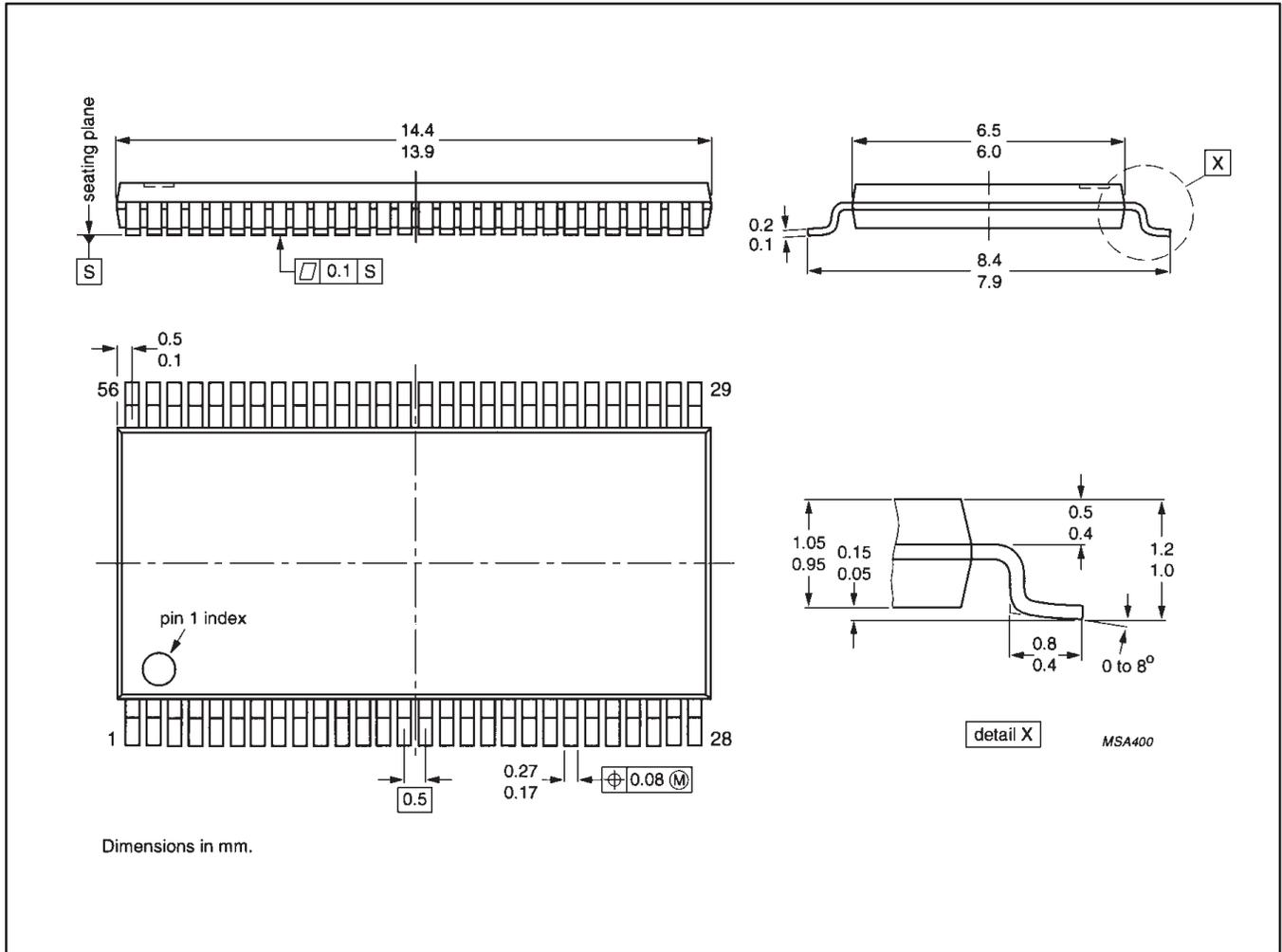
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

20-bit bus interface latch (3-State)

74ABT16841A 74ABTH16841A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



20-bit bus interface latch (3-State)

74ABT16841A
74ABTH16841A

Data sheet status

Data sheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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