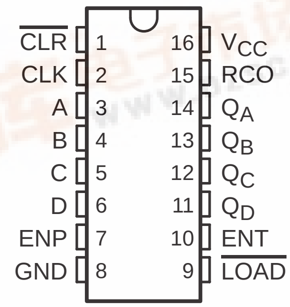
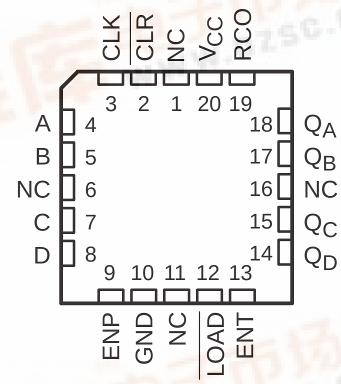
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 9.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV161A . . . J OR W PACKAGE
SN74LV161A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV161A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The 'LV161A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube of 40	SN74LV161AD	LV161A
		Reel of 2500	SN74LV161ADR	
	SOP − NS	Reel of 2000	SN74LV161ANSR	74LV161A
	SSOP − DB	Reel of 2000	SN74LV161ADBR	LV161A
	TSSOP − PW	Tube of 90	SN74LV161APW	LV161A
		Reel of 2000	SN74LV161APWR	
		Reel of 250	SN74LV161APWT	
	TVSOP − DGV	Reel of 2000	SN74LV161ADGVR	LV161A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV161AJ	SNJ54LV161AJ
	CFP − W	Tube of 150	SNJ54LV161AW	SNJ54LV161AW
	LCCC − FK	Tube of 55	SNJ54LV161AFK	SNJ54LV161AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information (continued)

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the ’LV161A devices is asynchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{LOAD}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

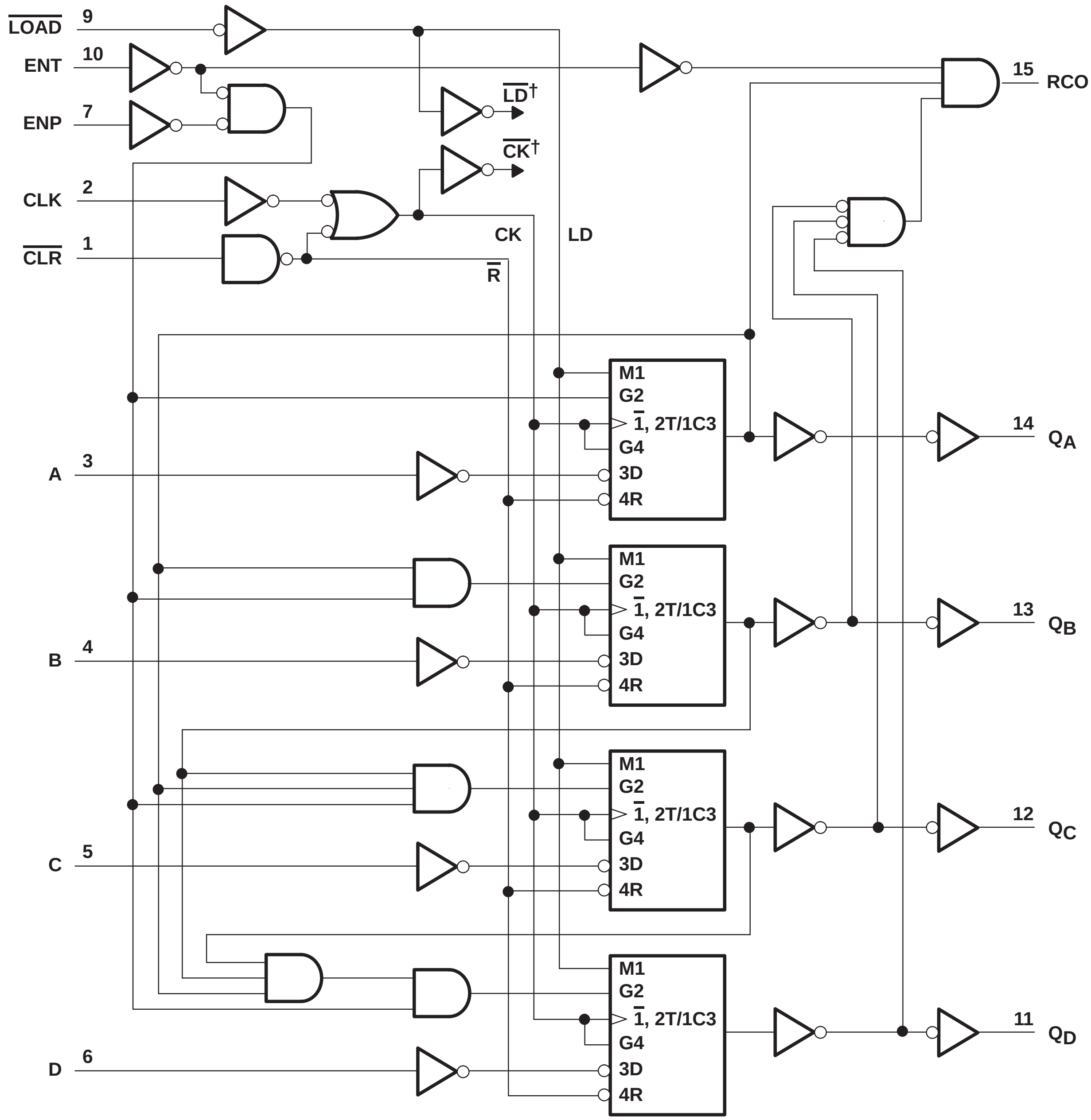
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CLK	QA	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to “0”
H	L	X	X		A	B	C	D	Preset Data
H	H	X	L		No Change				No Count
H	H	L	X		No Change				No Count
H	H	H	H		Count up				Count
H	X	X	X		No Change				No Count

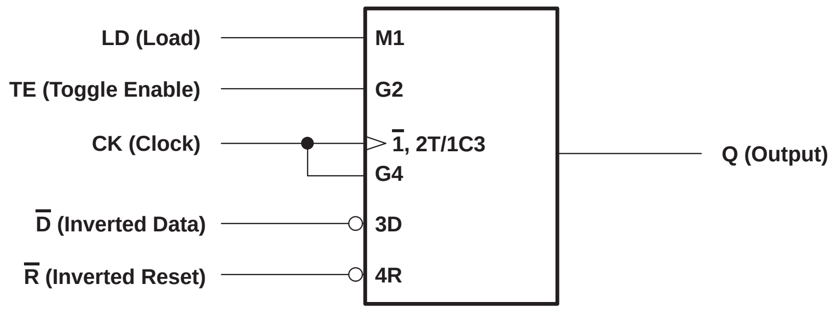
logic diagram (positive logic)



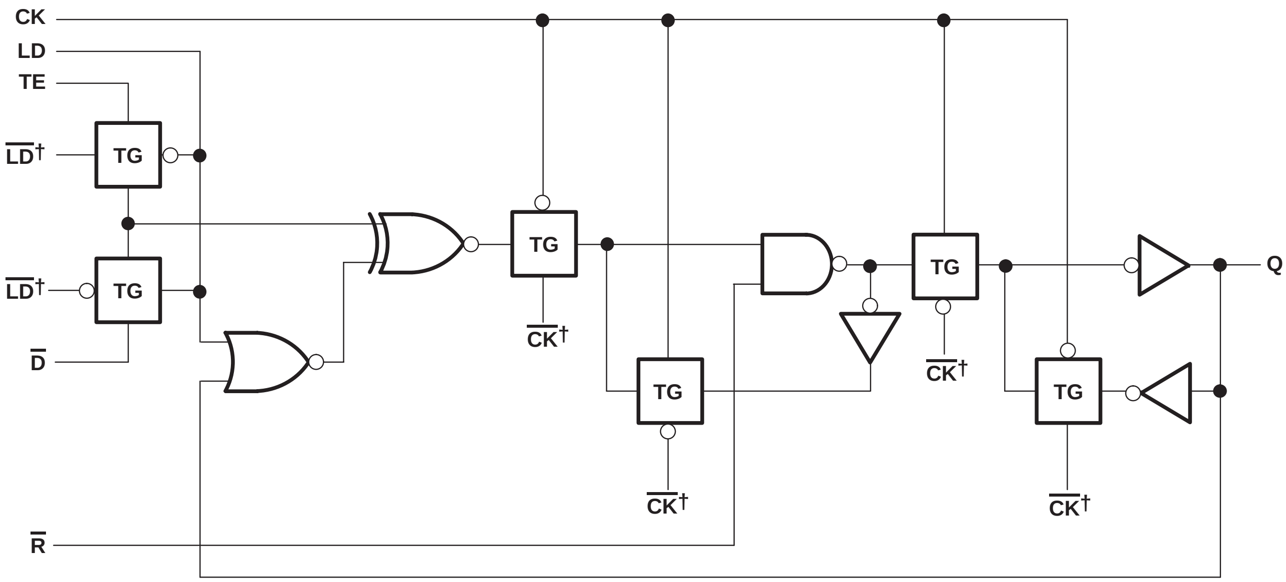
† For simplicity, routing of complementary signals LD and CK is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

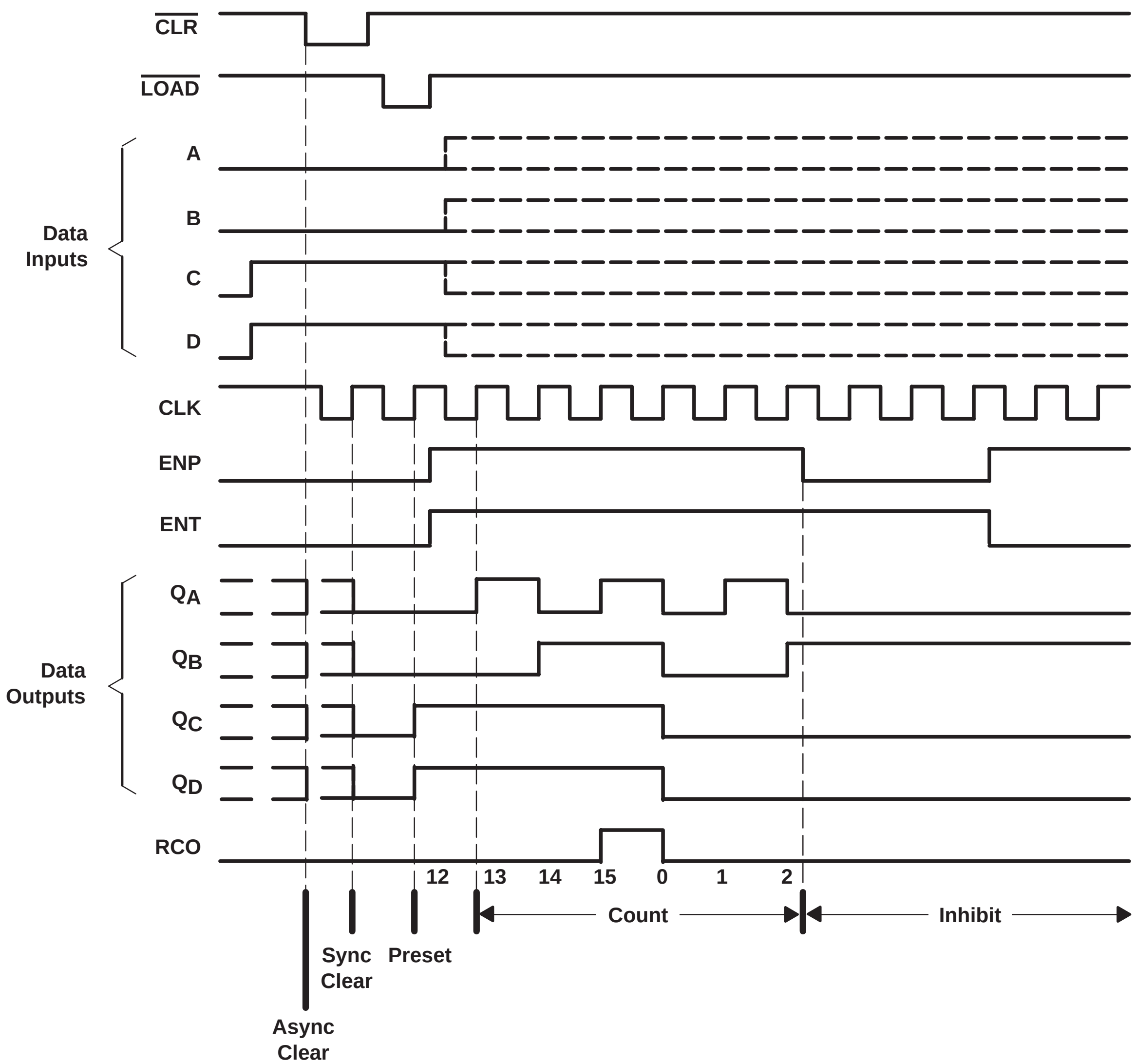


† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the overall logic diagram of the device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Output voltage range applied in high or low state, V_O (see Notes 1 and 2)		−0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the power-off state, V_O (see Note 1)		−0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0)		−20 mA
Output clamp current, I_{OK} (V_O < 0)		−50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	73°C/W
	DB package	82°C/W
	DGV package	120°C/W
	NS package	64°C/W
	PW package	108°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−6		−6	
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV161A			SN74LV161A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −6 mA	3 V	2.48			2.48			
	I_{OH} = −12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		1.8			1.8		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7		7		7		ns
		$\overline{\text{CLR}}$ low	7		7		7		
t_{su}	Setup time before CLK↑	$\overline{\text{CLR}}$	4.5		4.5		4.5		ns
		Data (A, B, C, and D)	7.5		8.5		8.5		
		ENP, ENT	9.5		11		11		
		$\overline{\text{LOAD}}$ low	10		11.5		11.5		
t_h	Hold time, all synchronous inputs after CLK↑		1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		$\overline{\text{CLR}}$ low	5		5		5		
t_{su}	Setup time before CLK↑	$\overline{\text{CLR}}$	2.5		2.5		2.5		ns
		Data (A, B, C, and D)	5.5		6.5		6.5		
		ENP, ENT	7.5		9		9		
		$\overline{\text{LOAD}}$ low	8		9.5		9.5		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV161A		SN74LV161A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		$\overline{\text{CLR}}$ low	5		5		5		
t_{su}	Setup time before CLK↑	$\overline{\text{CLR}}$	1.5		1.5		1.5		ns
		Data (A, B, C, and D)	4.5		4.5		4.5		
		ENP, ENT	5		6		6		
		$\overline{\text{LOAD}}$ low	5		6		6		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50*	125*		40*		40		MHz
			C_L = 50 pF	30	95		25		25		
t_{pd}	CLK	Q	C_L = 15 pF		7.9*	16.2*	1*	19.5*	1	19.5	ns
		RCO (count mode)			8.9*	17*	1*	20.5*	1	20.5	
		RCO (preset mode)			11.9*	20.6*	1*	24.5*	1	24.5	
	ENT	RCO			8.3*	15.7*	1*	19*	1	19	
t_{PHL}	$\overline{CLR}$	Q			8.8*	17*	1*	20.5*	1	20.5	
		RCO			9.8*	16.6*	1*	20*	1	20	
t_{pd}	CLK	Q	C_L = 50 pF		10.5	19.2	1	22.5	1	22.5	ns
		RCO (count mode)			11.7	20	1	23.5	1	23.5	
		RCO (preset mode)			14.5	23.6	1	27.5	1	27.5	
	ENT	RCO			11	18.7	1	22	1	22	
t_{PHL}	$\overline{CLR}$	Q			11.4	20	1	23.5	1	23.5	
		RCO			12.6	19.6	1	23	1	23	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	80*	165*		70*		70		MHz
			C_L = 50 pF	55	125		50		50		
t_{pd}*	CLK	Q	C_L = 15 pF		6	12.8	1*	15*	1	15	ns
		RCO (count mode)			6.7	13.6	1*	16*	1	16	
		RCO (preset mode)			8.6	17.2	1*	20*	1	20	
	ENT	RCO			6.2	12.3	1*	14.5*	1	14.5	
t_{PHL}*	$\overline{CLR}$	Q			6.5	13.6	1*	16*	1	16	
		RCO			7.2	13.2	1*	15.5*	1	15.5	
t_{pd}	CLK	Q	C_L = 50 pF		7.8	16.3	1	18.5	1	18.5	ns
		RCO (count mode)			8.7	17.1	1	19.5	1	19.5	
		RCO (preset mode)			10.6	20.7	1	23.5	1	23.5	
	ENT	RCO			8.3	15.8	1	18	1	18	
t_{PHL}	$\overline{CLR}$	Q			8.4	17.1	1	19.5	1	19.5	
		RCO			9.2	16.7	1	19	1	19	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	135*	220		115*		115		MHz
			C_L = 50 pF	95	165		85		85		
t_{pd}	CLK	Q	C_L = 15 pF		4.5*	8.1*	1*	9.5*	1	9.5	ns
		RCO (count mode)			5.1*	8.1*	1*	9.5*	1	9.5	
		RCO (preset mode)			6.3*	10.3*	1*	12*	1	12	
	ENT	RCO			4.8*	8.1*	1*	9.5*	1	9.5	
t_{PHL}	$\overline{CLR}$	Q			4.9*	9*	1*	10.5*	1	10.5	
		RCO			5.5*	8.6*	1*	10*	1	10	
t_{pd}	CLK	Q	C_L = 50 pF		5.9	10.1	1	11.5	1	11.5	ns
		RCO (count mode)			6.6	10.1	1	11.5	1	11.5	
		RCO (preset mode)			7.8	12.3	1	14	1	14	
	ENT	RCO			6.1	10.1	1	11.5	1	11.5	
t_{PHL}	$\overline{CLR}$	Q			6.3	11	1	12.5	1	12.5	
		RCO			6.9	10.6	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

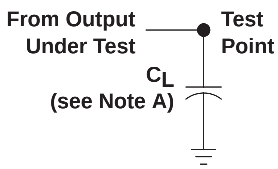
PARAMETER		SN74LV161A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.2	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

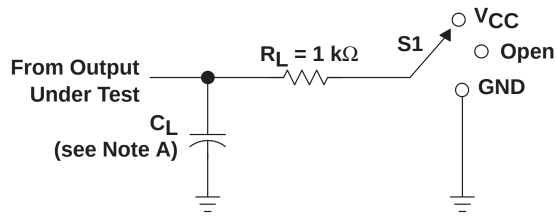
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	23.6	pF
			5 V	25.8	

PARAMETER MEASUREMENT INFORMATION

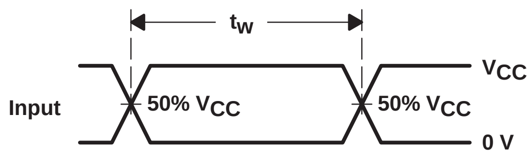


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

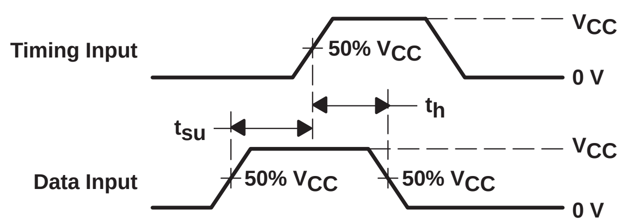


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

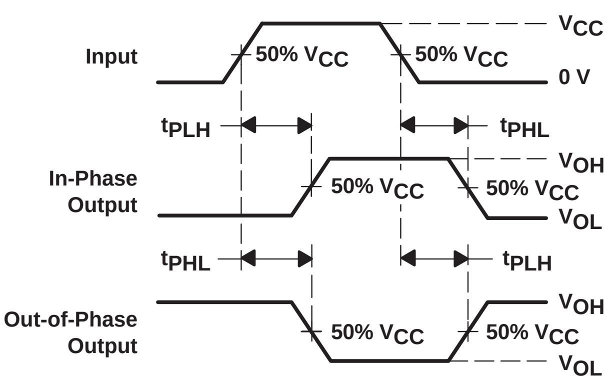
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



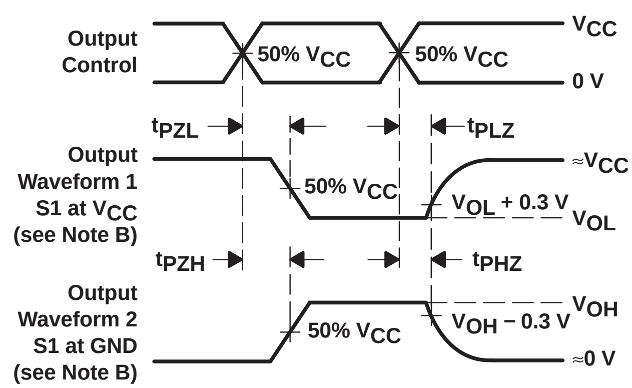
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LV161AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PACKAGE OPTION ADDENDUM

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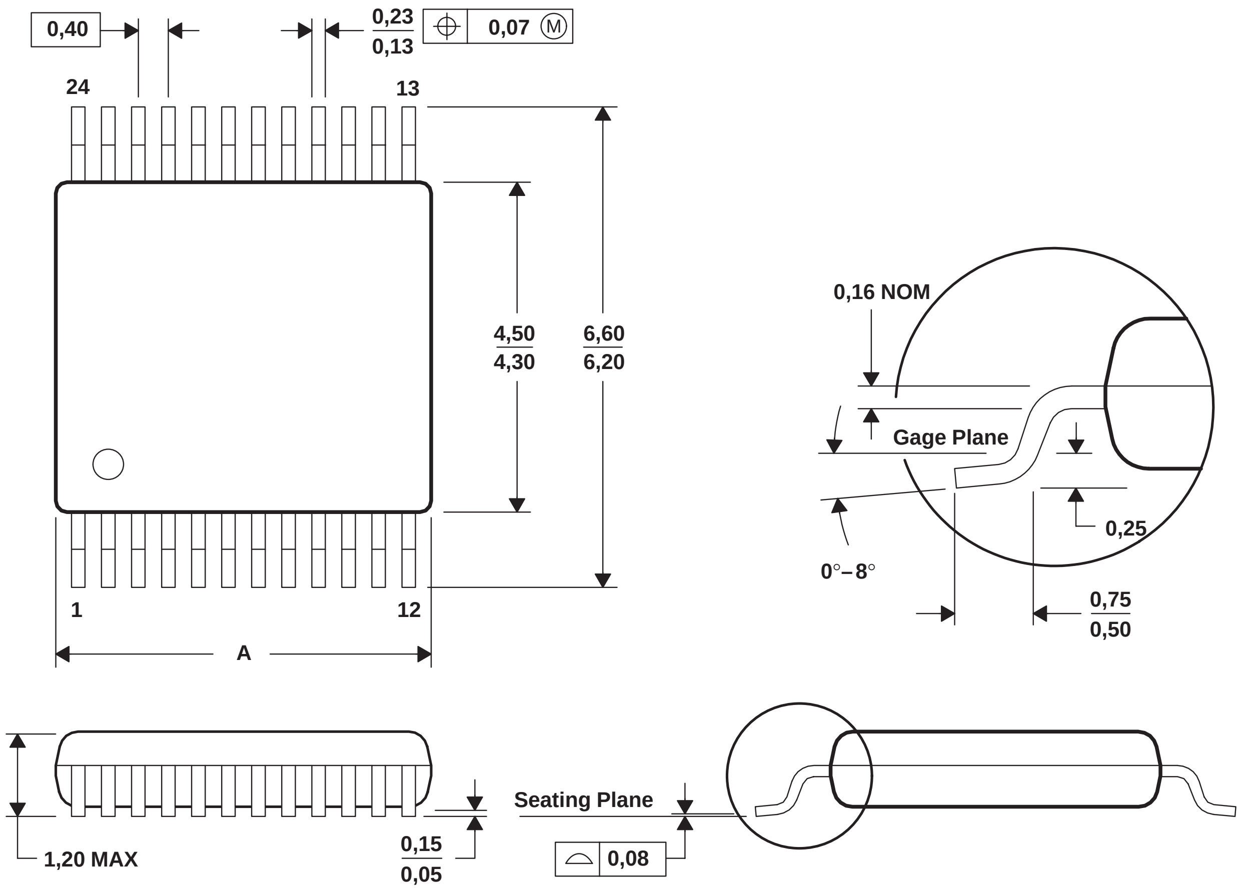
DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

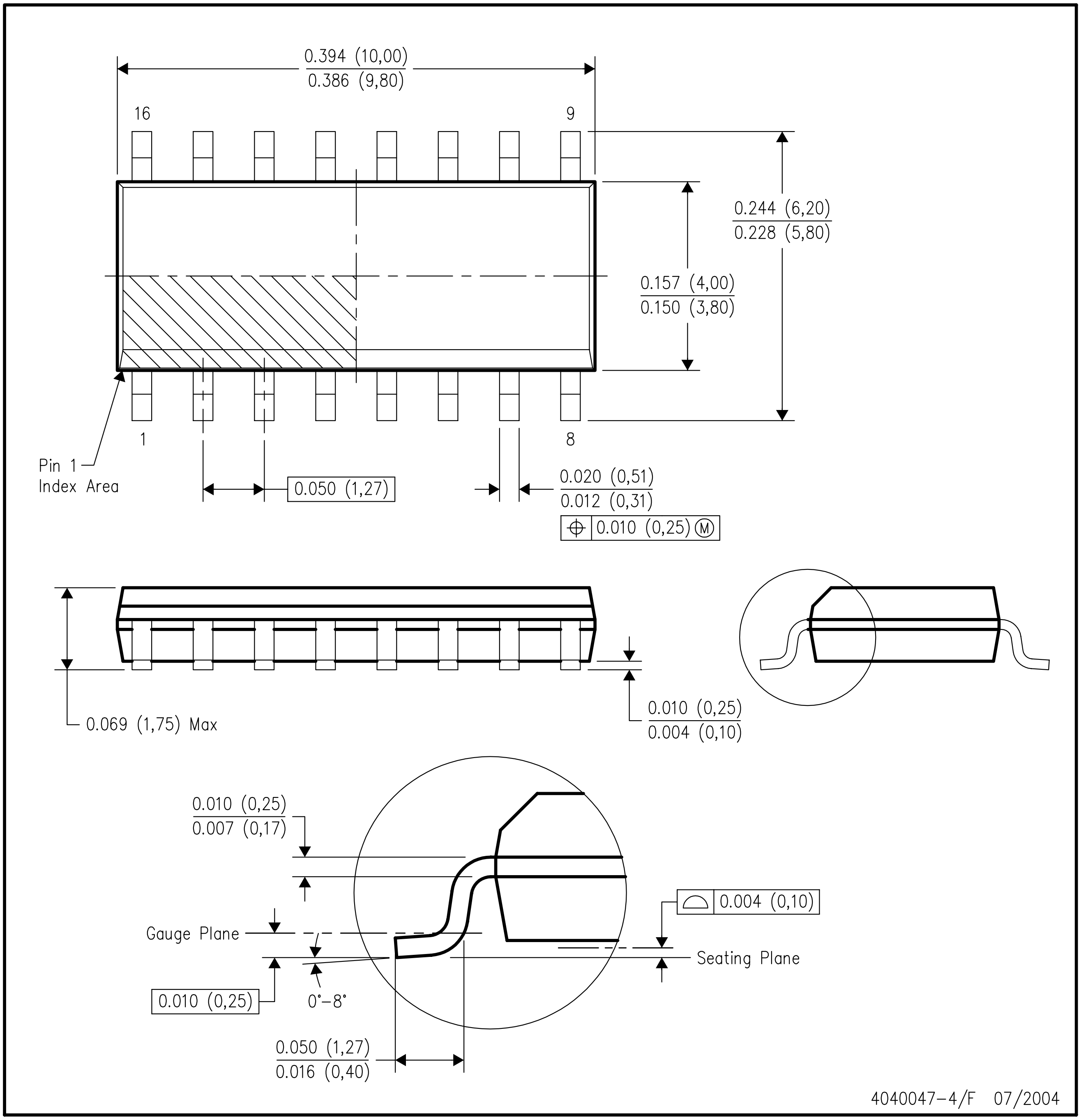


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

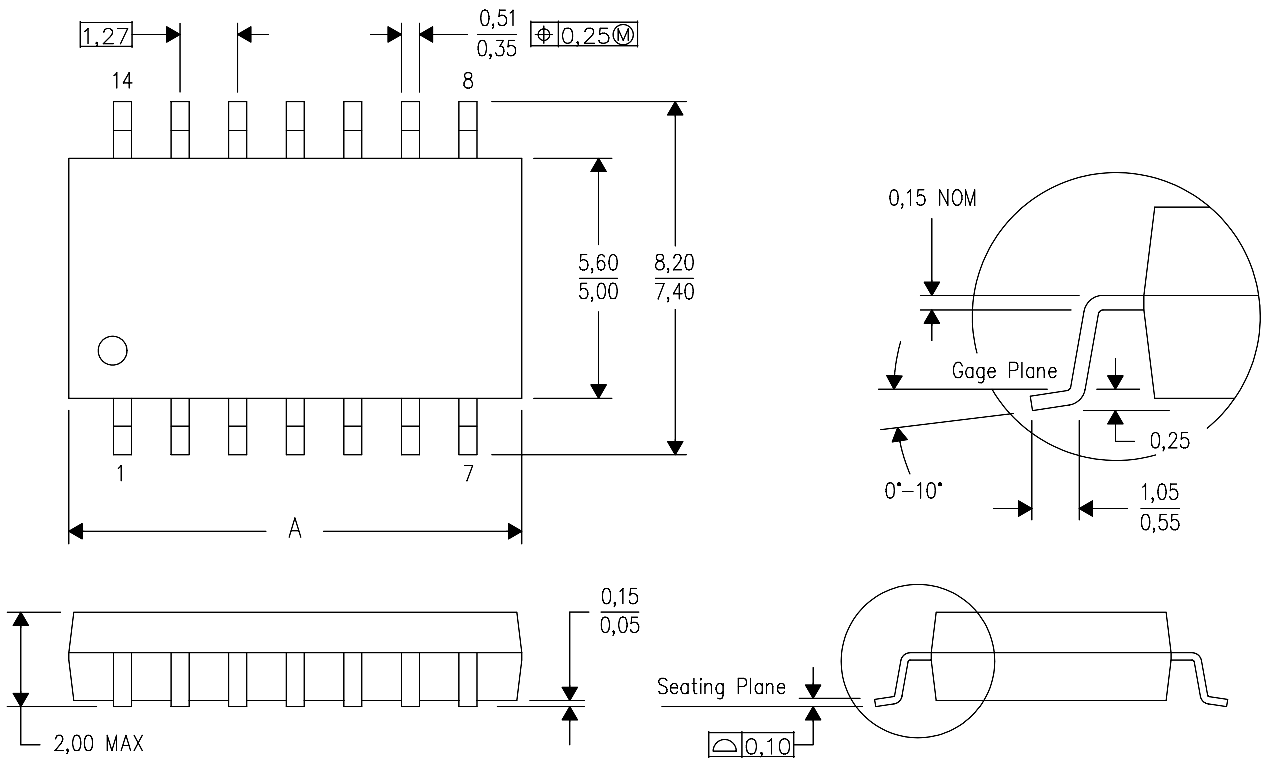
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AC.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



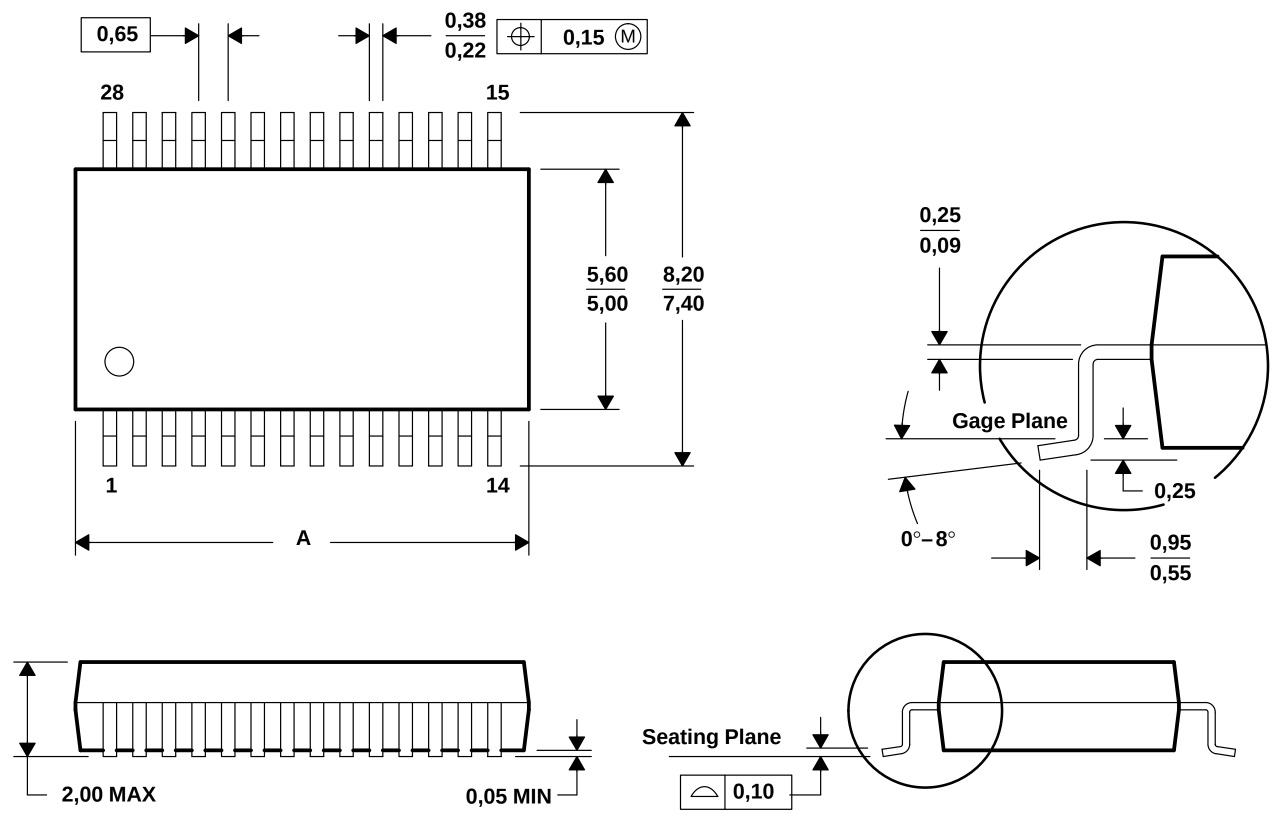
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



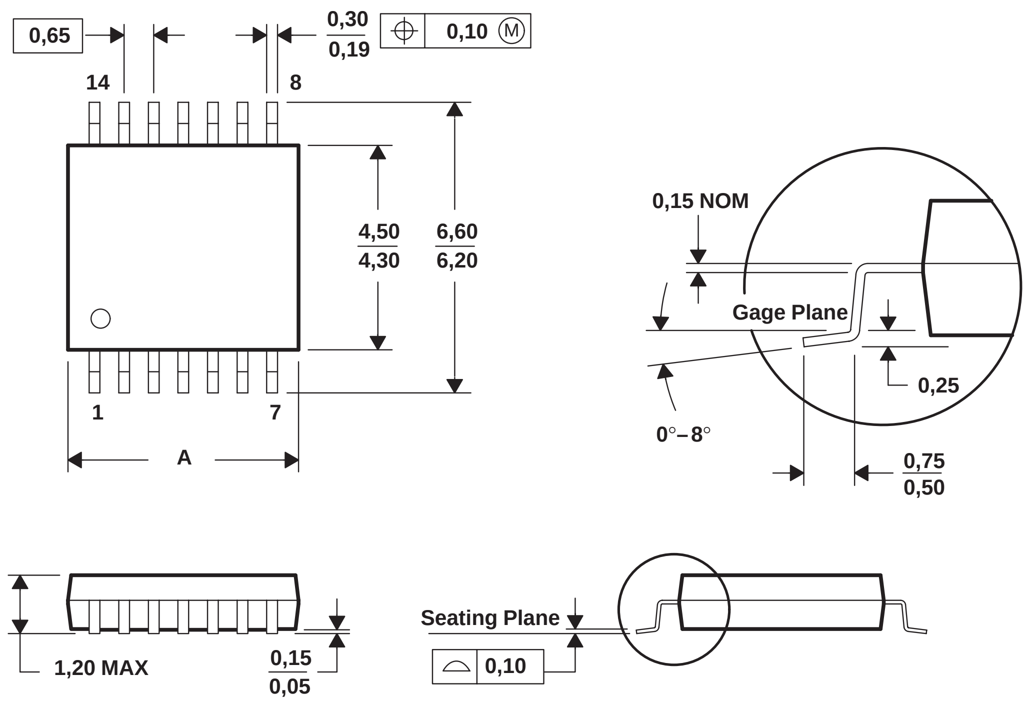
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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