FAMILY OF 600-μA/Ch 2.8-MHz RAIL-TO-RAIL INPUT/OUTPUT HIGH-DRIVE OPERATIONAL AMPLIFIERS

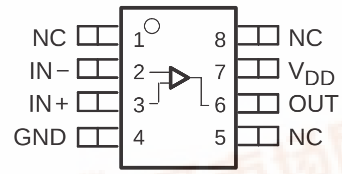
SGLS180A − AUGUST 2003 − REVISED OCTOBER 2004

- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **CMOS Rail-To-Rail Input/Output**
- **Input Bias Current . . . 2.5 pA**
- **Low Supply Current . . . 600 μA/Channel**
- **Gain-Bandwidth Product . . . 2.8 MHz**

† Contact Texas Instruments for details. Q100 qualification data available on request.

- **High Output Drive Capability**
  - **±10 mA at 180 mV**
  - **±35 mA at 500 mV**
- **Input Offset Voltage . . . 250 μV (typ)**
- **Supply Voltage Range . . . 2.7 V to 6 V**

TLV2471
D PACKAGE
(TOP VIEW)



description

The TLV247x is a family of CMOS rail-to-rail input/output operational amplifiers that establishes a new performance point for supply current versus ac performance. These devices consume just 600 μA/channel while offering 2.8 MHz of gain-bandwidth product. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower operational amplifiers. The TLV247x can swing to within 180 mV of each supply rail while driving a 10-mA load. For non-RRO applications, the TLV247x can supply ±35 mA at 500 mV off the rail. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV247x family ideal for sensor interface, portable medical equipment, and other data acquisition circuits.

The family is fully specified at 3 V and 5 V across the automotive temperature range (−40°C to 125°C).

FAMILY TABLE

DEVICE	NUMBER OF CHANNELS	UNIVERSAL EVM BOARD
TLV2471	1	See the EVM selection guide (SLOU060)
TLV2472	2	
TLV2474	4	

A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS‡

DEVICE	V_{DD} (V)	V_{IO} (μV)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (per channel) (μA)	OUTPUT DRIVE	RAIL-TO-RAIL
TLV247X	2.7 − 6	250	2.8	1.5	600	±35 mA	I/O
TLV245X	2.7 − 6	20	0.22	0.11	23	±10 mA	I/O
TLV246X	2.7 − 6	150	6.4	1.6	550	±90 mA	I/O
TLV277X	2.5 − 6	360	5.1	10.5	1000	±10 mA	O

‡ All specifications measured at 5 V.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

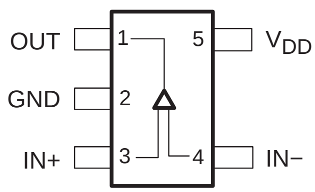
ORDERING INFORMATION†

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOP − D	Tape and reel	TLV2471QDRQ1	2471Q1
	SOP − D	Tape and reel	TLV2471AQDRQ1	2471AQ
	SOT23 − DBV	Tape and reel	TLV2471QDBVRQ1	471Q
−40°C to 125°C	SOP − D	Tape and reel	TLV2472QDRQ1	2472Q1
	SOP − D	Tape and reel	TLV2472AQDRQ1	2472AQ
	MSOP − DGN	Tape and reel	TLV2472QDGNRQ1‡	
−40°C to 125°C	SOP − D	Tape and reel	TLV2474QDRQ1	2474Q1
	SOP − D	Tape and reel	TLV2474AQDRQ1	2474AQ1
	TSSOP − PWP	Tape and reel	TLV2474QPWPRQ1	2474Q1
	TSSOP − PWP	Tape and reel	TLV2474APWPRQ1	2474AQ1

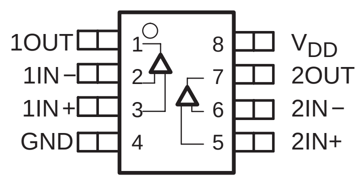
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ Product Preview.

TLV247x PACKAGE PINOUTS

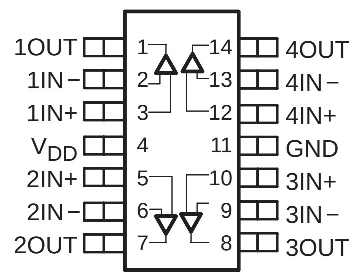
TLV2471
DBV PACKAGE
(TOP VIEW)



TLV2472
D OR DGN PACKAGE
(TOP VIEW)



TLV2474
D OR PWP PACKAGE
(TOP VIEW)



NC − No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 7 V
Differential input voltage, V_{ID} . . . . ±V_{DD}
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, ... −40°C to 125°C
Maximum junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
DBV (3)	55	324.1	385 mW
DGN (8)	4.7	52.7	2370 mW
PWP (14)	2.07	30.7	4070 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		0	V_{DD}	V
Operating free-air temperature, T_A		−40	125	°C

† Relative to GND

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$	TLV247x	25°C		250	2200	μV
				Full range			2400	
			TLV247xA	25°C		250	1600	
				Full range			1800	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$				0.4		μV/°C
I_{IO}	Input offset current	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$		25°C		1.5	50	pA
				Full range			300	
I_{IB}	Input bias current	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$		25°C		2	50	
				Full range			300	
V_{OH}	High-level output voltage	$V_{IC} = V_{DD}/2$	$I_{OH} = -2.5$ mA	25°C	2.85	2.94		V
				Full range	2.8			
			$I_{OH} = -10$ mA	25°C	2.6	2.74		
				Full range	2.5			
V_{OL}	Low-level output voltage	$V_{IC} = V_{DD}/2$	$I_{OL} = 2.5$ mA	25°C		0.07	0.15	V
				Full range			0.2	
			$I_{OL} = 10$ mA	25°C		0.2	0.35	
				Full range			0.5	
I_{OS}	Short-circuit output current	Sourcing		25°C	30			mA
				Full range	20			
		Sinking		25°C	30			
				Full range	20			
I_O	Output current	V_O = 0.5 V from rail		25°C		±22		mA
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = 1$ V,	$R_L = 10\ k\Omega$	25°C	90	116		dB
				Full range	88			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		19.3		pF
z_o	Closed-loop output impedance	f = 10 kHz,	$A_V = 10$	25°C		2		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3 V, $R_S = 50\ \Omega$		25°C	58	78		dB
				Full range	56			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 6 V, No load	$V_{IC} = V_{DD}/2$,	25°C	68	90		dB
				Full range	60			
		V_{DD} = 3 V to 5 V, No load	$V_{IC} = V_{DD}/2$,	25°C	70	92		
				Full range	60			
I_{DD}	Supply current (per channel)	$V_O = 1.5$ V,	No load	25°C		550	750	μA
				Full range			800	

† Full range is −40°C to 125°C. If not specified, full range is −40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	1.1	1.4		V/μs
				Full range	0.6			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		28		nV/√Hz
		f = 1 kHz		25°C		15		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.405		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.1%		
			A_V = 100			0.5%		
	Gain-bandwidth product	f = 10 kHz,	R_L = 600 Ω	25°C		2.8		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.5		μs
			0.01%			3.9		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.6		
			0.01%			4		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		61°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		15		dB

† Full range is −40°C to 125°C. If not specified, full range is −40°C to 125°C.
‡ Depending on package dissipation rating

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω	TLV247x	25°C		250	2200	μV
				Full range			2400	
			TLV247xA	25°C		250	1600	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω				0.4		μV/°C
I_{IO}	Input offset current	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω		25°C		1.7	50	pA
				Full range			300	
I_{IB}	Input bias current	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_S = 50 Ω		25°C		2.5	50	
				Full range			300	
V_{OH}	High-level output voltage	$V_{IC} = V_{DD}/2$	I_{OH} = −2.5 mA	25°C	4.85	4.96		V
				Full range	4.8			
			I_{OH} = −10 mA	25°C	4.72	4.82		
				Full range	4.65			
V_{OL}	Low-level output voltage	$V_{IC} = V_{DD}/2$	I_{OL} = 2.5 mA	25°C		0.07	0.15	V
				Full range			0.2	
			I_{OL} = 10 mA	25°C		0.178	0.28	
				Full range			0.35	
I_{OS}	Short-circuit output current	Sourcing		25°C	110			mA
				Full range	60			
		Sinking		25°C	90			
				Full range	60			
I_O	Output current	V_O = 0.5 V from rail		25°C		±35		mA
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	92	120		dB
				Full range	91			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		18.9		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		1.8		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 5 V, R_S = 50 Ω		25°C	62	84		dB
				Full range	58			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 2.7 V to 6 V, No load	$V_{IC} = V_{DD}/2$,	25°C	68	90		dB
				Full range	60			
		V_{DD} = 3 V to 5 V, No load	$V_{IC} = V_{DD}/2$,	25°C	70	92		
				Full range	60			
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load	25°C		600	900	μA
				Full range			1000	

† Full range is −40°C to 125°C. If not specified, full range is −40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	1.1	1.5		V/μs
				Full range	0.7			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		28		nV/√Hz
		f = 1 kHz		25°C		15		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.39		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.01%		
			A_V = 10			0.05%		
			A_V = 100			0.3%		
	Gain-bandwidth product	f = 10 kHz,	R_L = 600 Ω	25°C		2.8		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.8		μs
			0.01%			3.3		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.7		
			0.01%			3		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		68°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		23		dB

† Full range is −40°C to 125°C for Q suffix. If not specified, full range is −40°C to 125°C.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IB}	Input bias current	vs Free-air temperature	3, 4
I_{IO}	Input offset current		
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
Z_o	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
PSRR	Power supply rejection ratio	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
V_n	Equivalent input noise voltage	vs Frequency	13
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	14, 15
A_{VD}	Differential voltage gain and phase	vs Frequency	16, 17
ϕ_m	Phase margin	vs Load capacitance	18, 19
	Gain margin	vs Load capacitance	20, 21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Supply voltage	23
		vs Free-air temperature	24, 25
	Crosstalk	vs Frequency	26
THD+N	Total harmonic distortion + noise	vs Frequency	27, 28
V_O	Large and small signal follower	vs Time	29 − 32

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

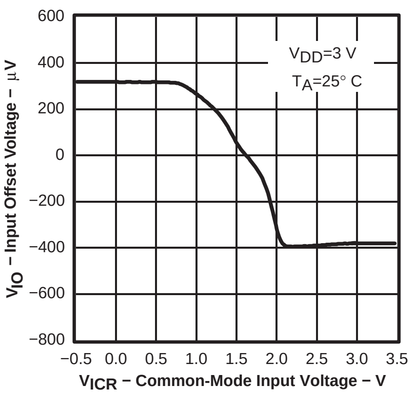


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

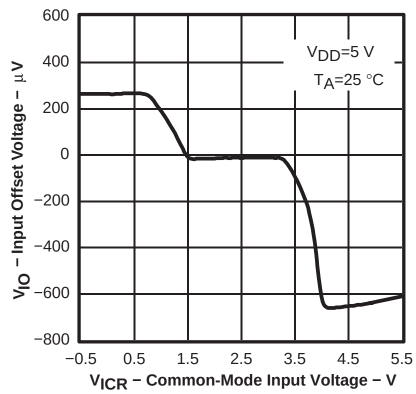


Figure 2

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

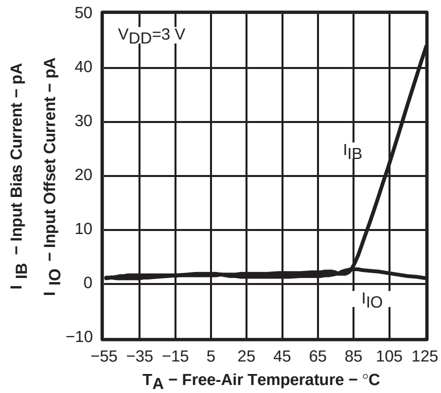


Figure 3

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

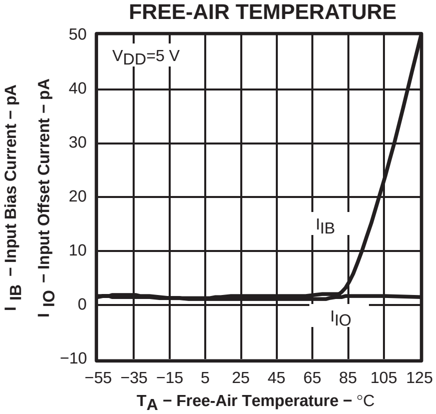


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

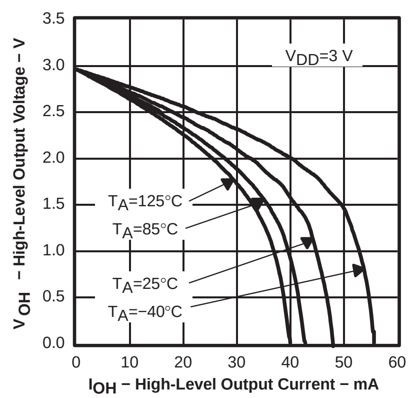


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

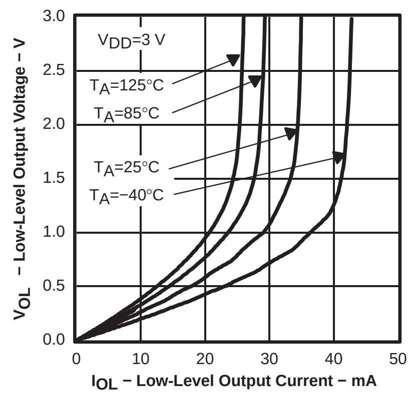


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

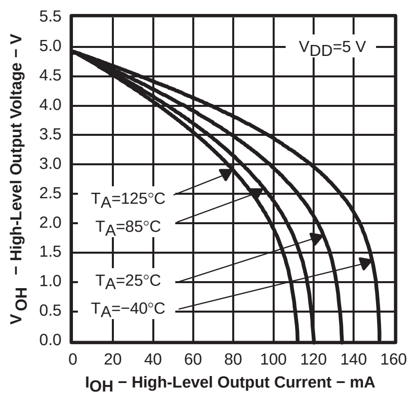


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

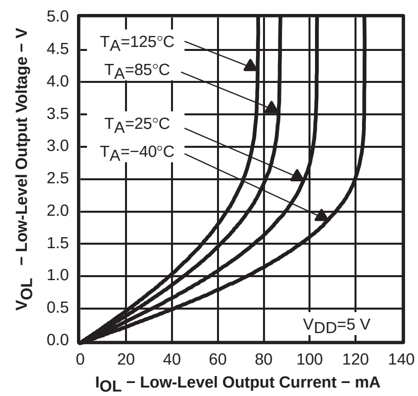


Figure 8

OUTPUT IMPEDANCE vs FREQUENCY

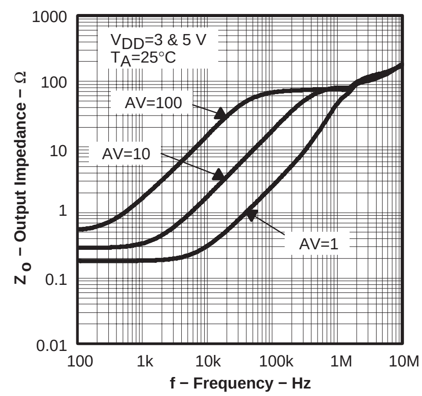


Figure 9

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

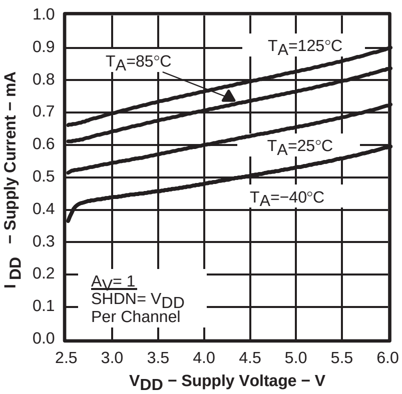


Figure 10

POWER SUPPLY REJECTION RATIO vs FREQUENCY

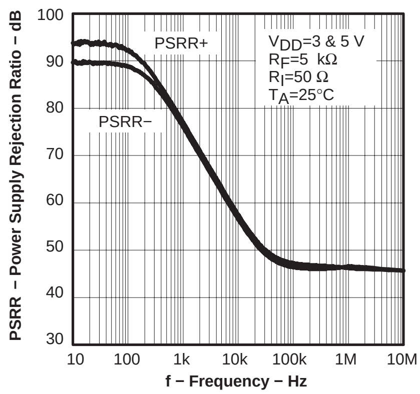


Figure 11

COMMON-MODE REJECTION RATIO vs FREQUENCY

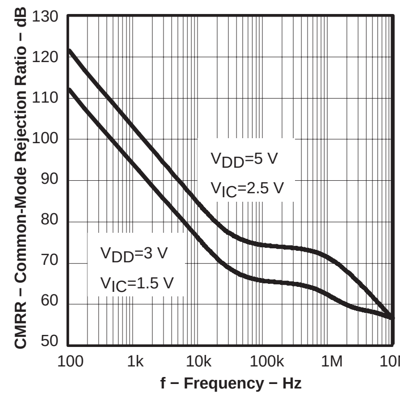


Figure 12

EQUIVALENT NOISE VOLTAGE vs FREQUENCY

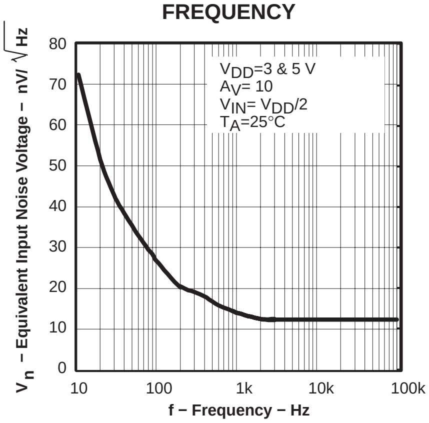


Figure 13

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

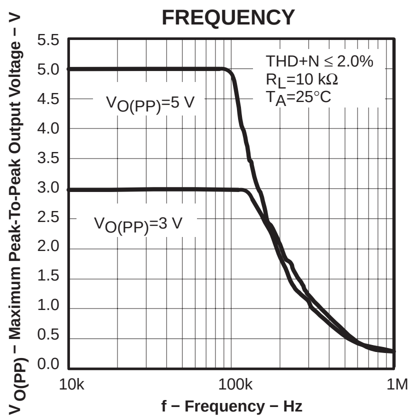


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

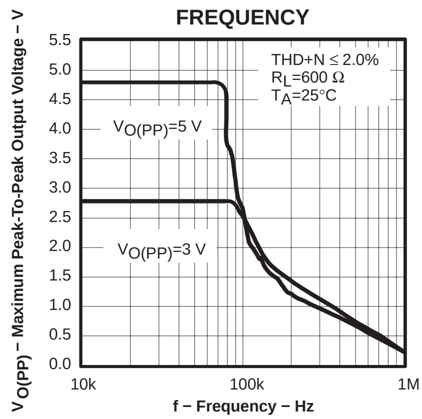


Figure 15

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

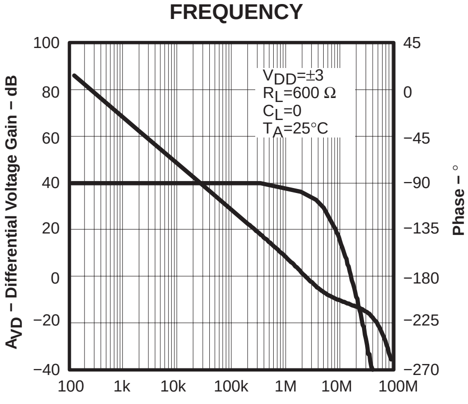


Figure 16

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

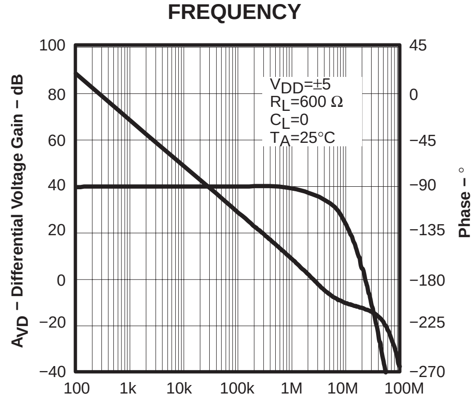


Figure 17

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

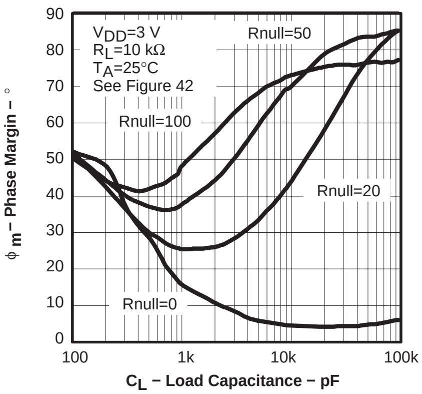


Figure 18

PHASE MARGIN vs LOAD CAPACITANCE

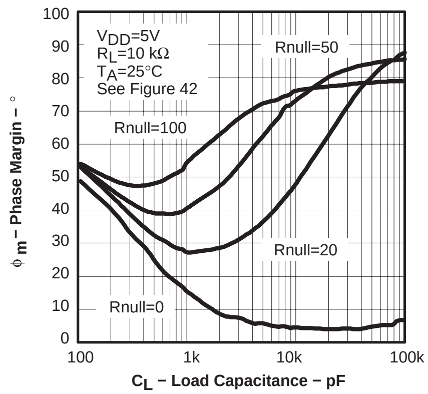


Figure 19

GAIN MARGIN vs LOAD CAPACITANCE

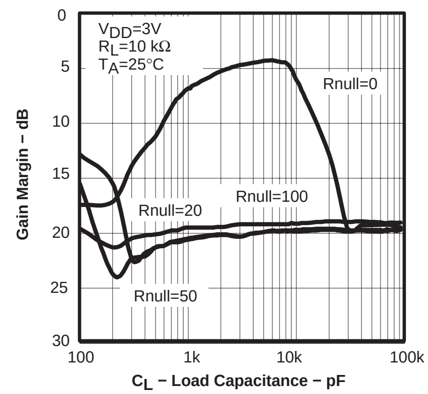


Figure 20

GAIN MARGIN vs LOAD CAPACITANCE

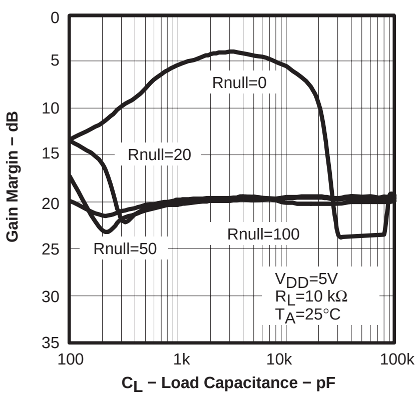


Figure 21

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

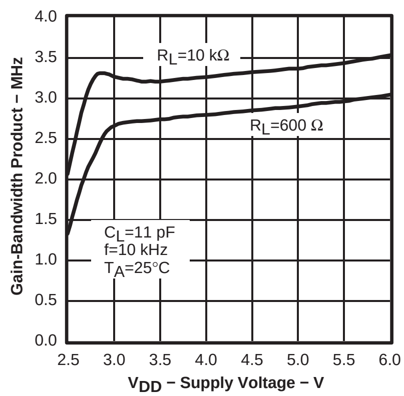


Figure 22

SLEW RATE vs SUPPLY VOLTAGE

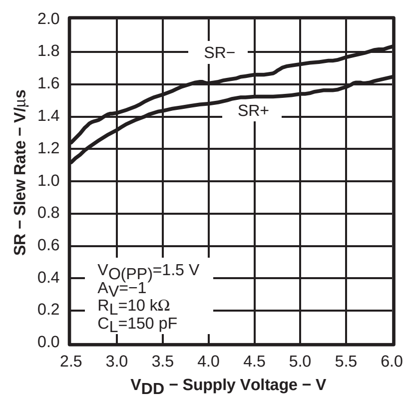


Figure 23

SLEW RATE vs FREE-AIR TEMPERATURE

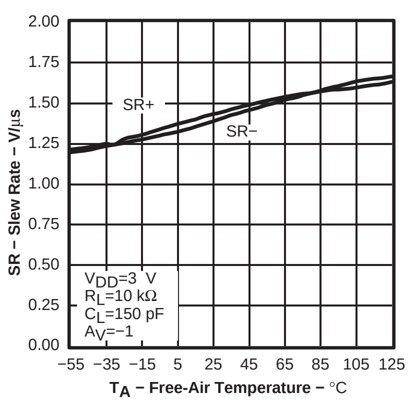


Figure 24

SLEW RATE vs FREE-AIR TEMPERATURE

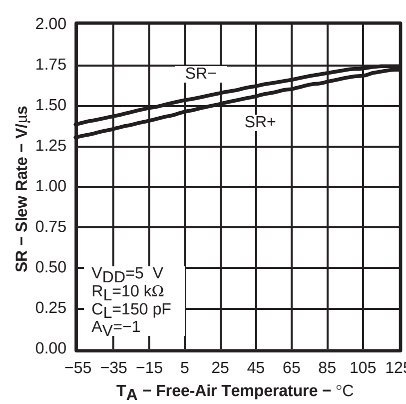


Figure 25

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

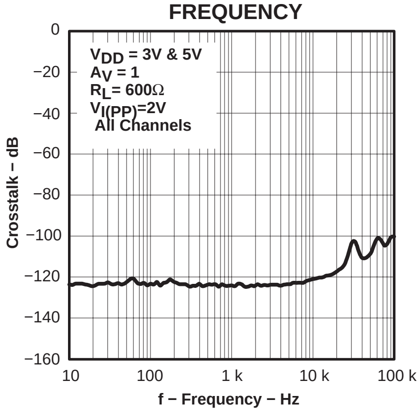


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

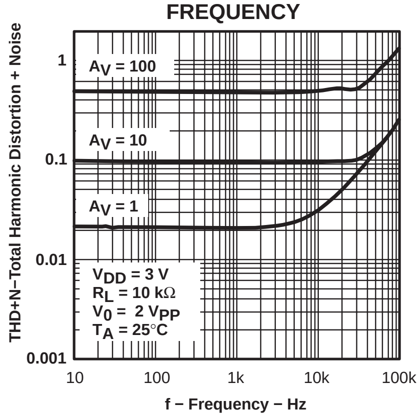


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

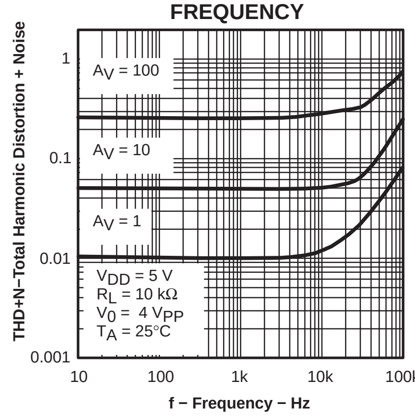


Figure 28

LARGE SIGNAL FOLLOWER PULSE RESPONSE vs TIME

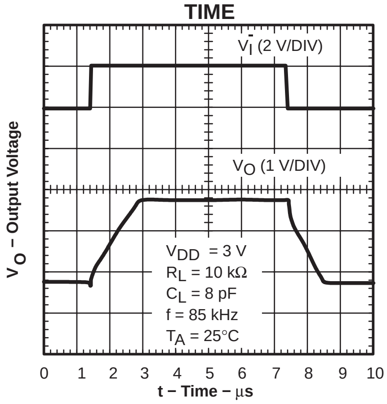


Figure 29

LARGE SIGNAL FOLLOWER PULSE RESPONSE vs TIME

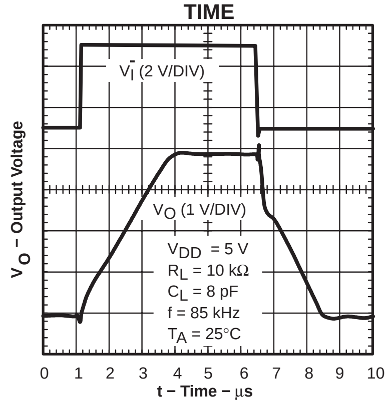


Figure 30

SMALL SIGNAL FOLLOWER PULSE RESPONSE vs TIME

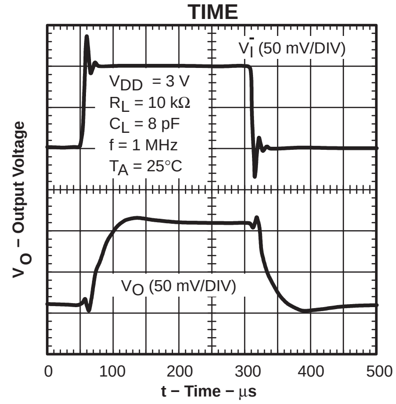


Figure 31

SMALL SIGNAL FOLLOWER PULSE RESPONSE vs TIME

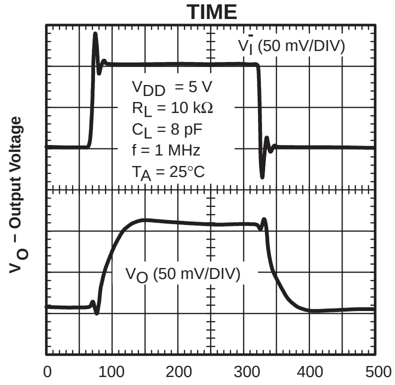


Figure 32

PARAMETER MEASUREMENT INFORMATION

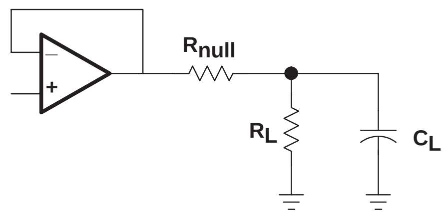


Figure 33

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 34. A minimum value of 20 Ω should work well for most applications.

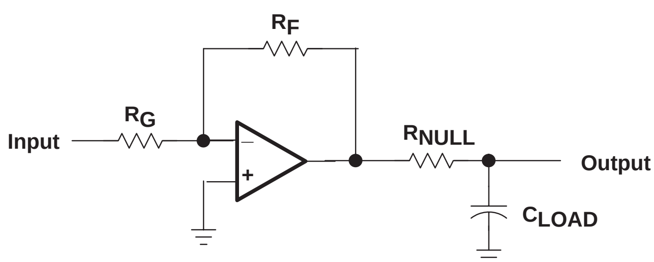
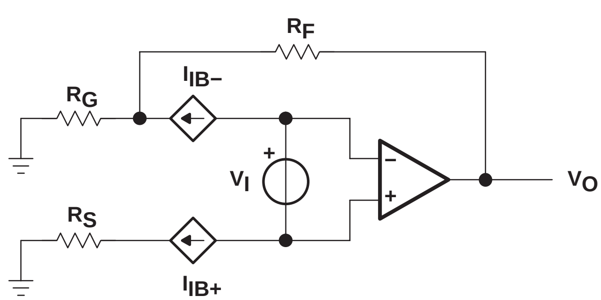


Figure 34. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage.



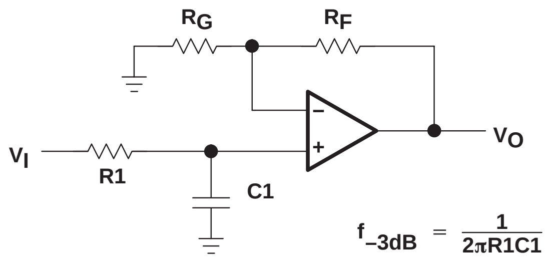
$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 35. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 36).

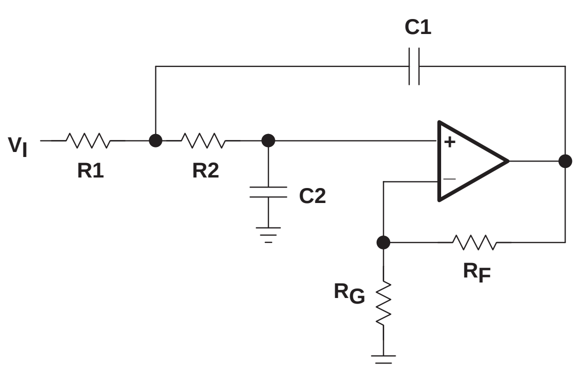


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 36. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 37. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV247x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

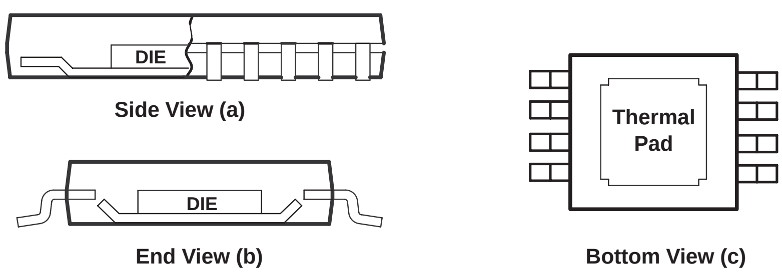
APPLICATION INFORMATION

general PowerPAD™ design considerations

The TLV247x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 38(a) and Figure 38(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 38(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 38. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

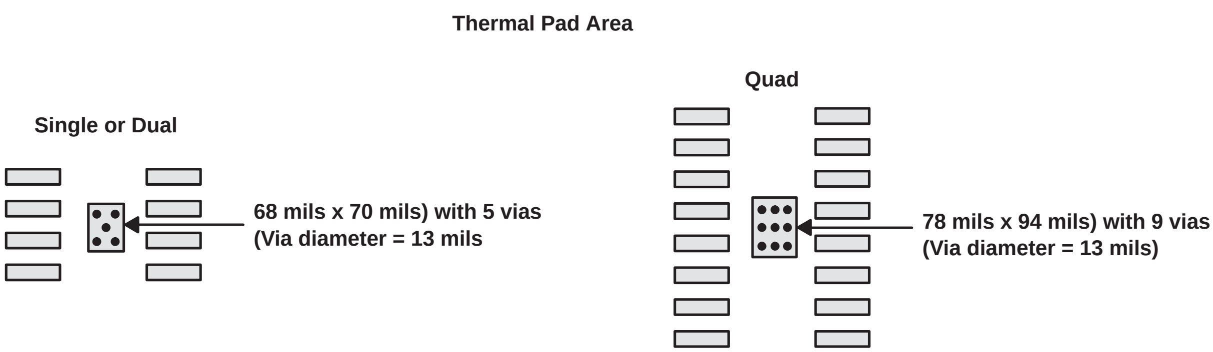


Figure 39. PowerPAD PCB Etch and Via Pattern

PowerPAD is a trademark of Texas Instruments Incorporated.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

1. Prepare the PCB with a top side etch pattern as shown in Figure 39. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV247x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV247x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLV247x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

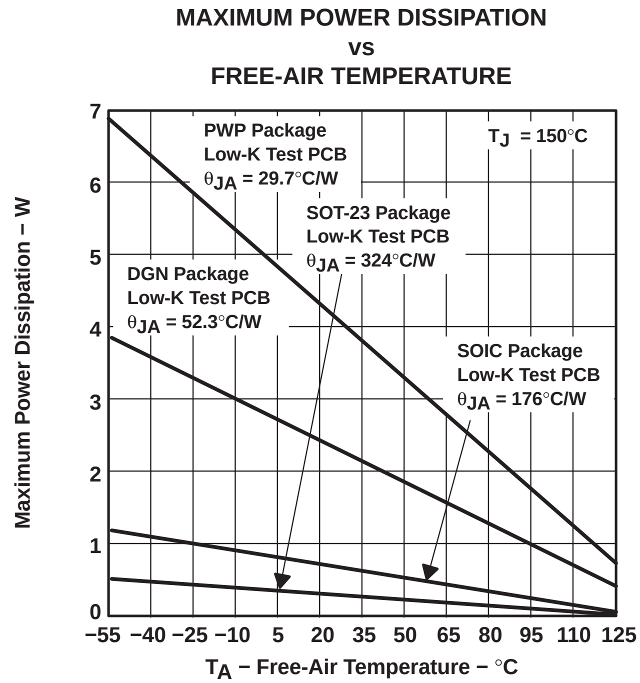
$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV247x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40.

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 41 to Figure 46 show this effect, along with the quiescent heat, with an ambient air temperature of 70°C and 125°C. When using V_{DD} = 3 V, there is generally not a heat problem with an ambient air temperature of 70°C. But, when using V_{DD} = 5 V, the packages are severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

TLV2471†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

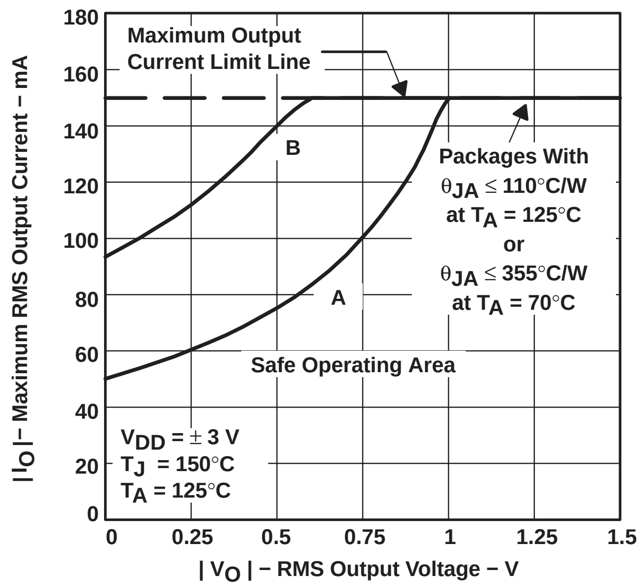


Figure 41

TLV2471†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

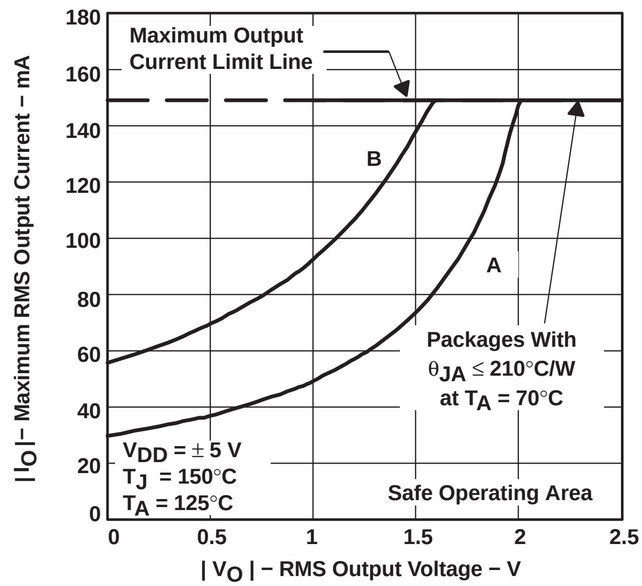


Figure 42

TLV2472†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

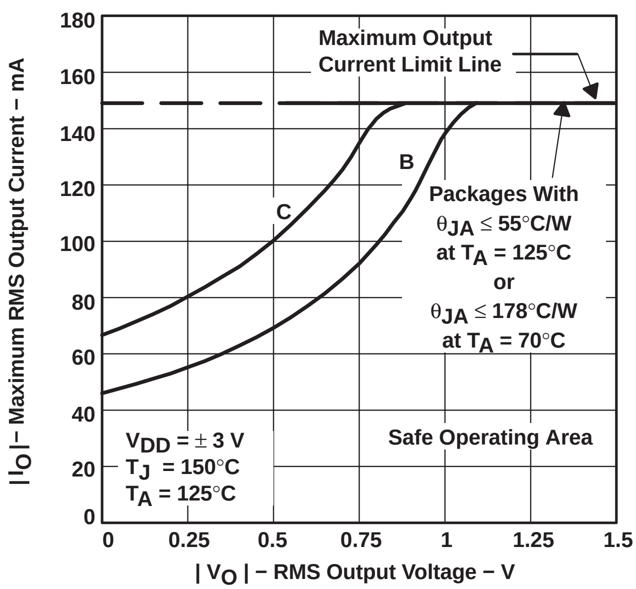


Figure 43

TLV2472†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

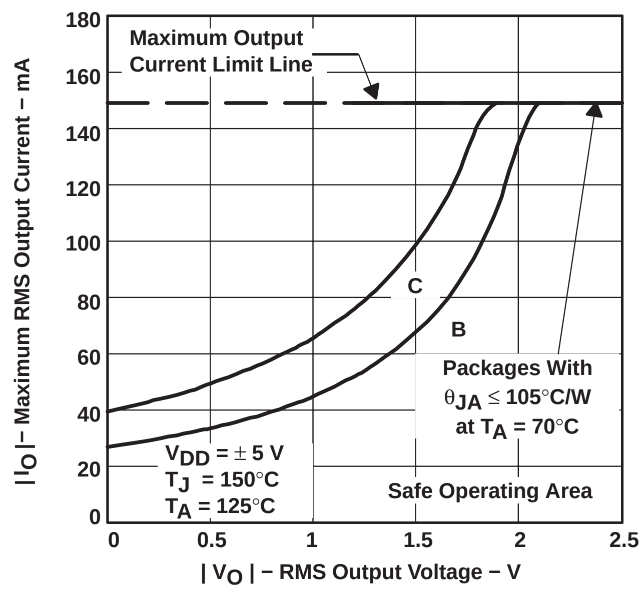


Figure 44

† A − SOT23(5); B − SOIC (8); C − SOIC (14); D − TSSOP PP (14)

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

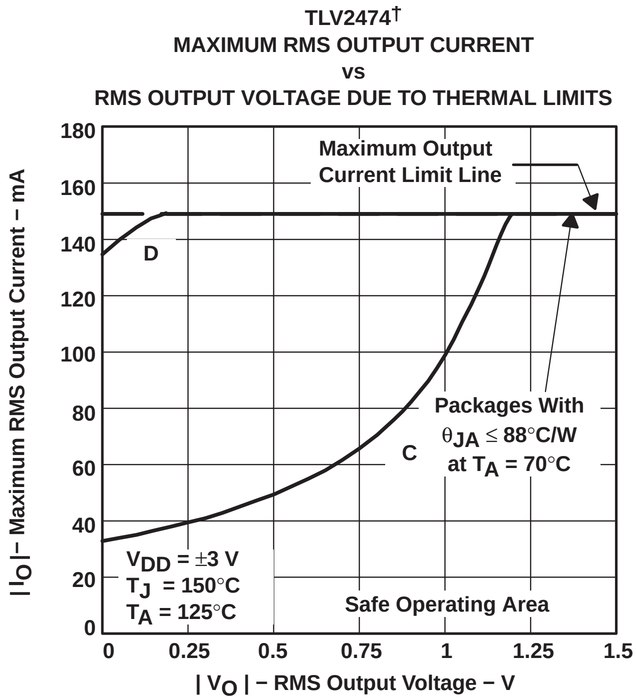


Figure 45

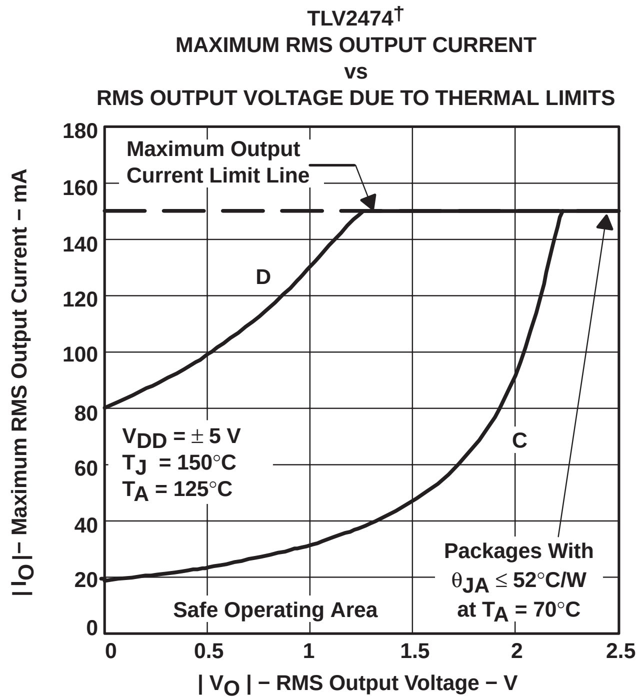


Figure 46

† A − SOT23(5); B − SOIC (8); C − SOIC (14); D − TSSOP PP (14)

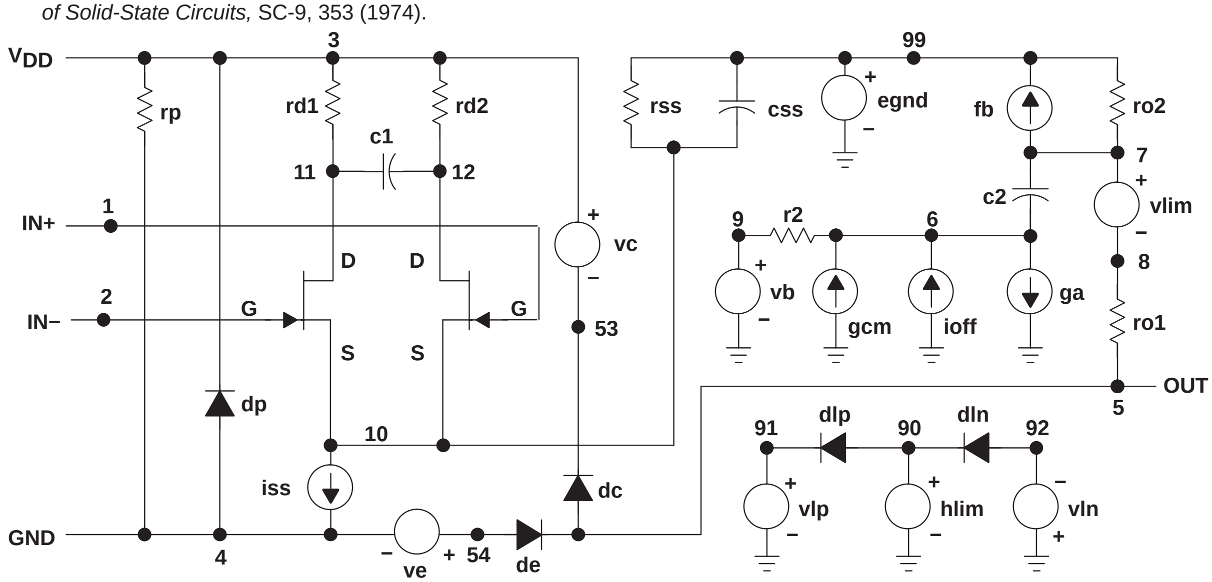
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 47 are generated using the TLV247x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
* TLV247x operational amplifier ”macromodel” subcircuit
* created using Parts release 8.0 on 4/27/99 at 14:31
* Parts is a MicroSim product.
*
* connections:   non−inverting input
*                 | inverting input
*                 | | positive power supply
*                 | | | negative power supply
*                 | | | | output
*                 | | | | |
.subckt TLV247x 1 2 3 4 5
*
   c1     11   12   1.1094E−12
   c2     6    7    5.5000E−12
   css    10   99   556.53E−15
   dc     5    53   dy
   de     54   5    dy
   dlp    90   91   dx
   dln    92   90   dx
   dp     4    3    dx
   egnd   99   0    poly(2) (3,0) (4,0) 0 .5 .5
   fb     7    99   poly(5) vb vc ve vlp vln 0
   + 39.614E6 −1E3 1E3 40E6 −40E6
   ga     6    0    11   12   79.828E−6
   gcm    0    6    10   99   32.483E−9
iss      10   4    dc    10.714E−6
hlim     90   0    vlim 1K
ioff     0    6    dc    75E−9
j1       11   2    10 jx1
j2       12   1    10 jx2
r2       6    9    100.00E3
rd1      3    11   12.527E3
rd2      3    12   12.527E3
ro1      8    5    10
ro2      7    99   10
rp       3    4    3.8023E3
rss      10   99   18.667E6
vb       9    0    dc 0
vc       3    53   dc .842
ve       54   4    dc .842
vlim     7    8    dc 0
vlp      91   0    dc 110
vln      0    92   dc 110
.model   dx   D(Is=800.00E−18)
.model   dy   D(Is=800.00E−18 Rs=1m Cjo=10p)
.model   jx1  NJF(Is=1.0825E−12 Beta=594.78E−06 + Vto=−1)
.model   jx2  NJF(Is=1.0825E−12 Beta=594.78E−06 + Vto=−1)
.ends
*$
```

Figure 47. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLV2471AQDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2471QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2472AQDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2472QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2474APWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	None	Call TI	Level-1-220C-UNLIM
TLV2474AQDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2474QDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2474QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	None	Call TI	Level-1-220C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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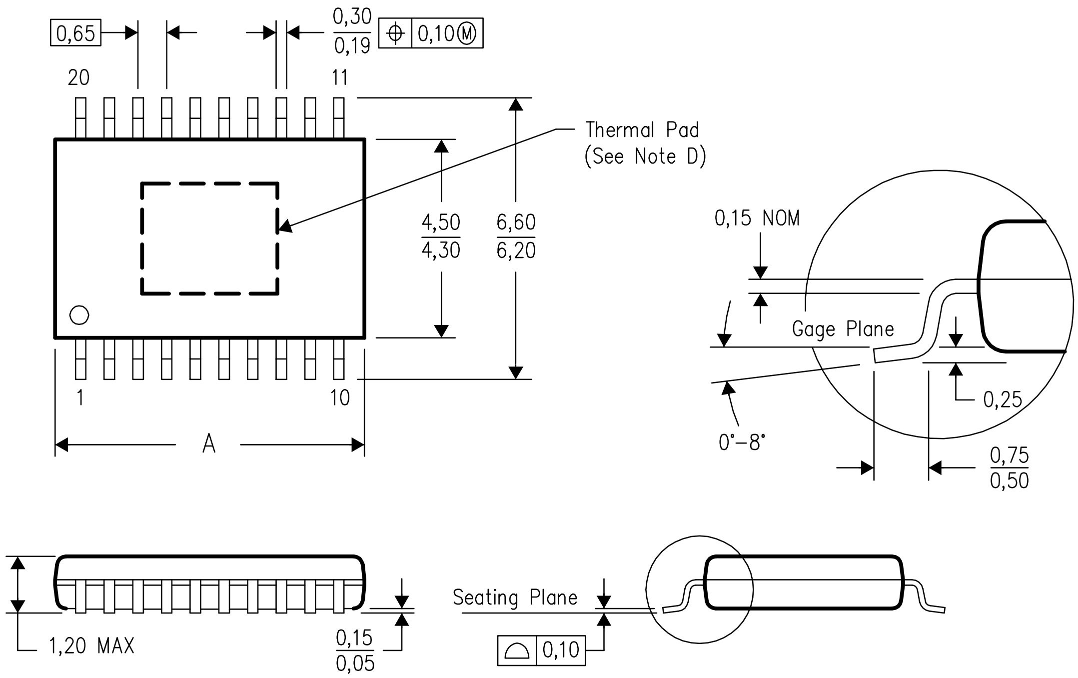
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN

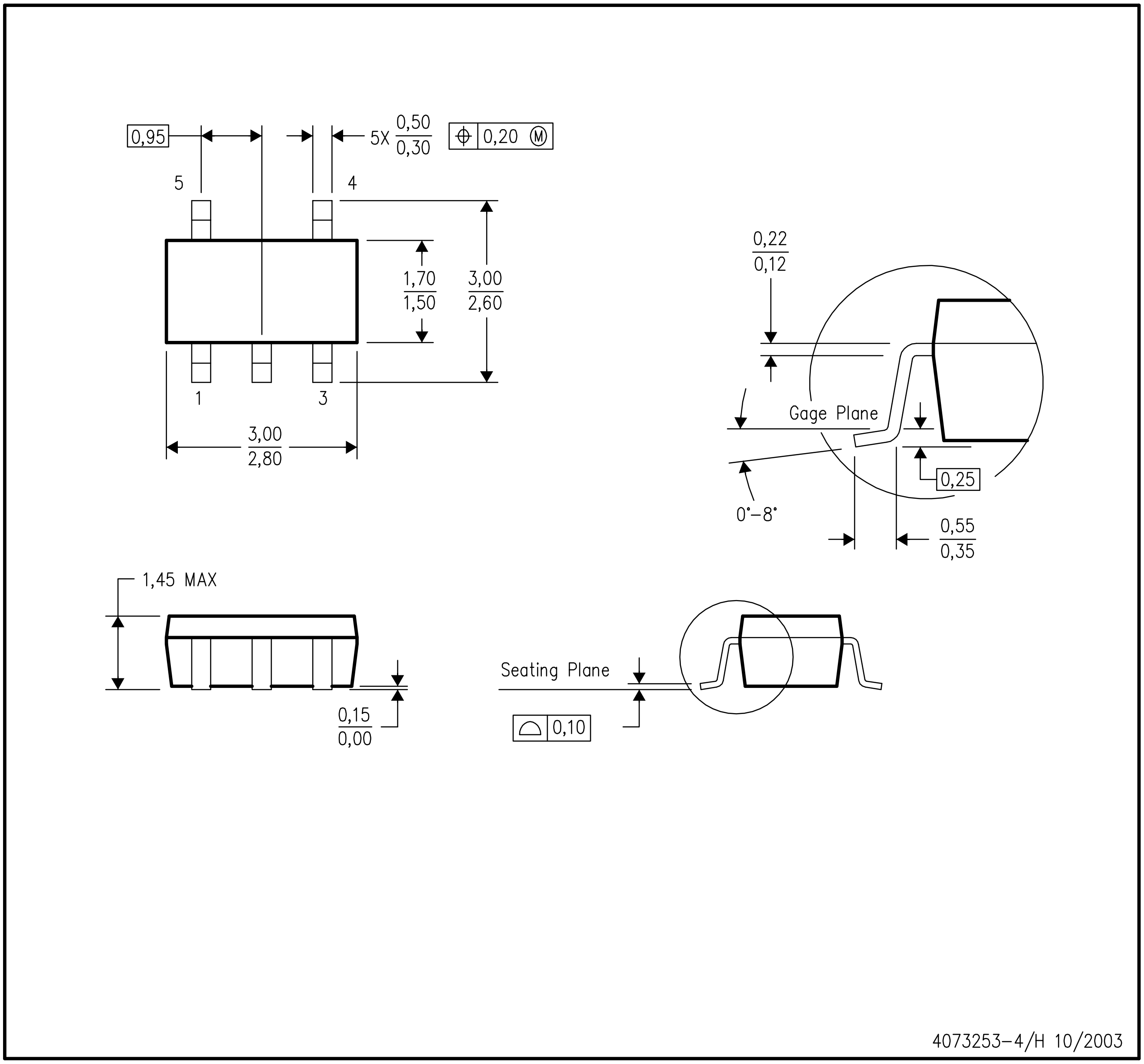


DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

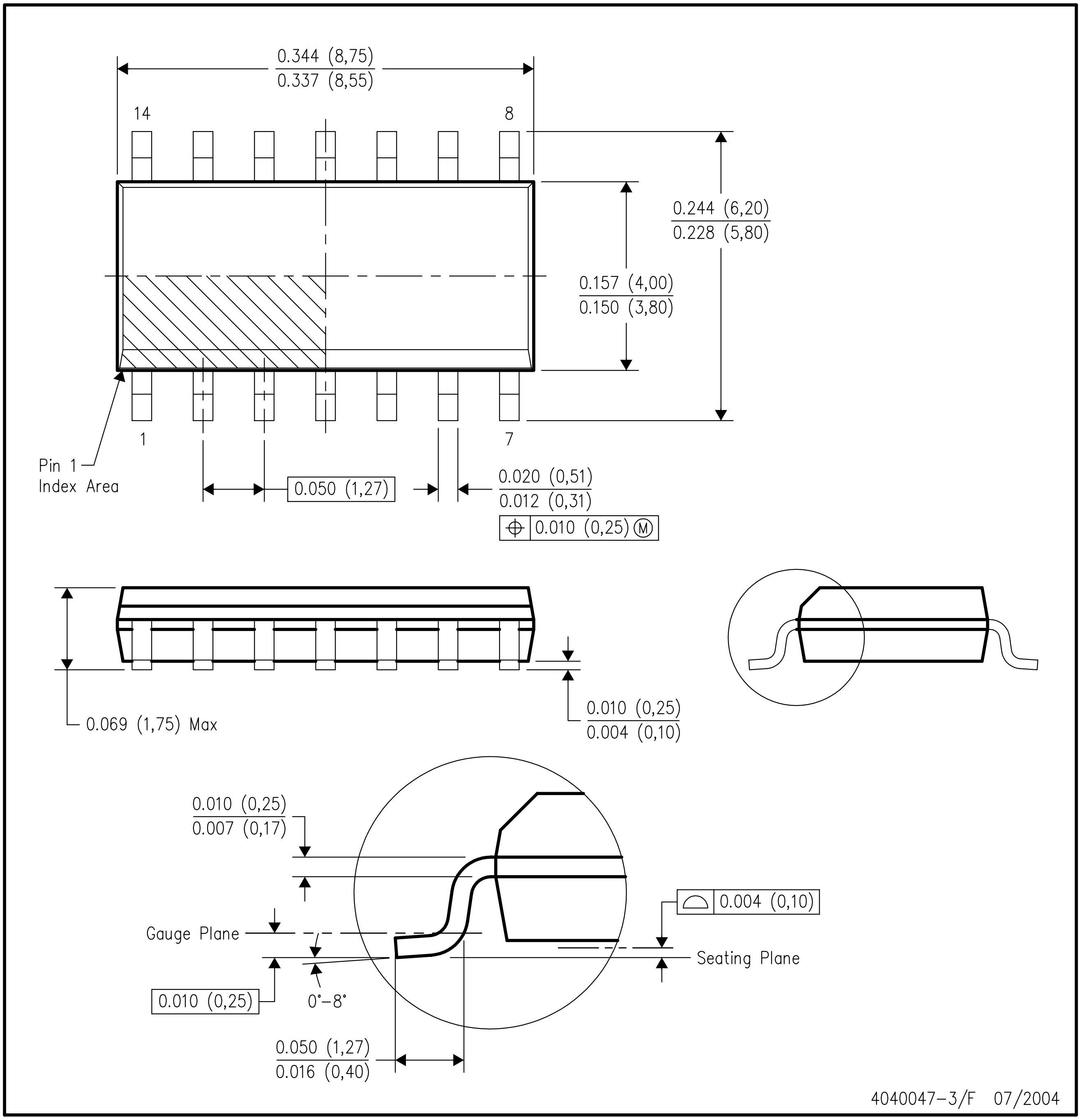
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO–153

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



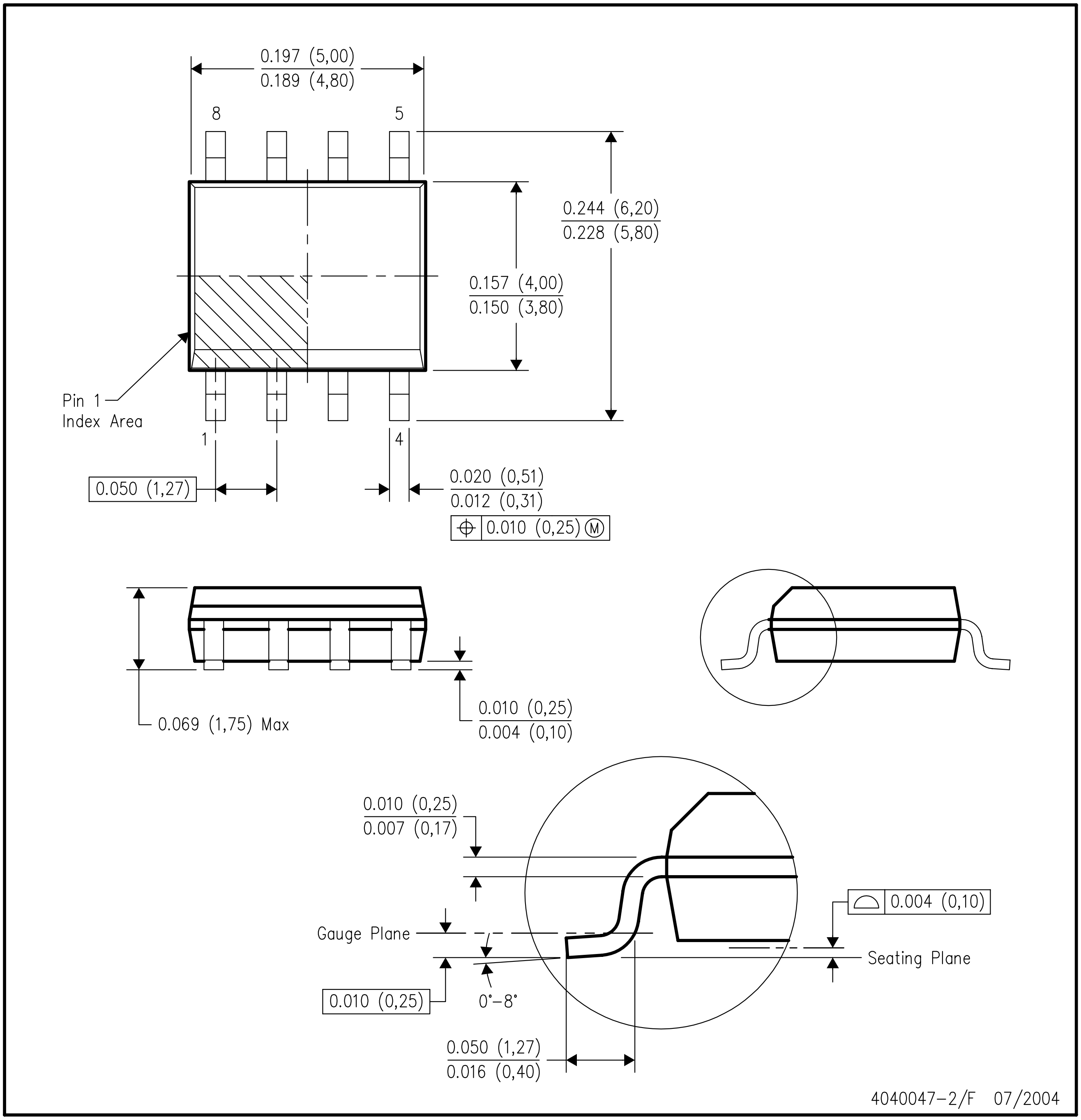
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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