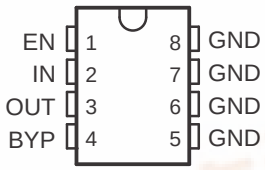
# TL5209
# 500-mA LOW-NOISE LOW-DROPOUT VOLTAGE REGULATOR WITH SHUTDOWN

SLVS581 – SEPTEMBER 2006

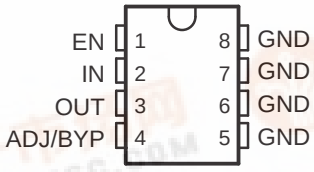
## FEATURES

- Adjustable and Fixed Voltages of 1.8 V, 2.5 V, 3 V, 3.3 V, and 5 V
- 1%/2% Accuracy (25°C/Full Range)
- 500-mV (Max) Dropout at Full Load of 500 mA
- Extremely Tight Regulation Over Temperature Range
  - 0.1%/V (Max) Line Regulation
  - 0.7% (Max) Load Regulation
- Ultra-Low Noise Capability (300 nV/$\sqrt{Hz}$ Typ)
- Shutdown Current of 3 μA (Max)
- Low Temperature Coefficient
- Current Limiting and Thermal Protection
- Stable With Minimum Load of 1 mA
- Reverse-Battery Protection
- Applications
  - Portable Applications (PDAs, Laptops, Cell Phones)
  - Consumer Electronics
  - Post-Regulation for SMPS
- Available in Convenient Surface-Mount Packages: SOT-223, SOIC-8, and TO-263

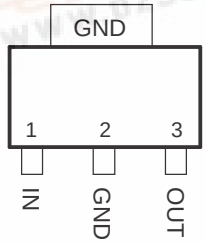
FIXED VOLTAGE . . . D PACKAGE
(TOP VIEW)



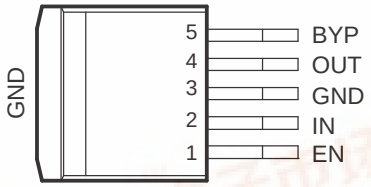

ADJUSTABLE VOLTAGE . . . D PACKAGE
(TOP VIEW)



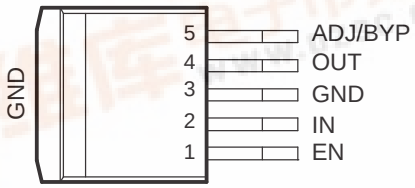

FIXED VOLTAGE . . . DCY (SOT-223) PACKAGE
(TOP VIEW)




FIXED VOLTAGE . . . KTT (TO-263) PACKAGE
(TOP VIEW)




ADJUSTABLE VOLTAGE . . . KTT (TO-263) PACKAGE
(TOP VIEW)




## DESCRIPTION/ORDERING INFORMATION

The TL5209 is an efficient PNP low-dropout (LDO) regulator that is well suited for portable applications. It has significantly lower quiescent current than previously was available from traditional PNP regulators and allows for a shutdown current (SOIC-8 and TO-263) of only 0.05 μA (typical). The TL5209 also has very good dropout voltage characteristics, requiring a maximum dropout of 60 mV at light loads and 500 mV at full load. In addition, the LDO also has 1% output voltage accuracy and extremely tight line and load regulation that is hard to match by its CMOS counterparts.

For noise-sensitive applications, the TL5209 allows for low-noise capability via an external bypass capacitor connected to the BYPASS pin (SOIC-8 and TO-263), which reduces the output noise of the regulator. Other features include current limiting, thermal shutdown, reverse-battery protection, and low temperature coefficient.

The TL5209 is available in adjustable output and fixed-output versions of 1.8 V, 2.5 V, 3 V, 3.3 V, and 5 V. Offered in surface-mount packages of SOT-223, SOIC, and TO-263, the TL5209 is characterized for operation over the virtual junction temperature ranges of –40°C to 125°C.

## ORDERING INFORMATION

| $T_J$ | $V_{OUT}$ (NOM) | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| –40°C to 125°C | 1.8 V | SOIC – D | Reel of 2000 | TL5209-18DR | TL520918 |
| | | SOT-223 – DCY | Reel of 2000 | TL5209-18DCYR | TA |
| | | TO-263 – KTT | Reel of 2000 | TL5209-18KTTR | TL5209-18 |
| | 2.5 V | SOIC – D | Reel of 2000 | TL5209-25DR | TL520925 |
| | | SOT-223 – DCY | Reel of 2000 | TL5209-25DCYR | TB |
| | | TO-263 – KTT | Reel of 2000 | TL5209-25KTTR | TL5209-25 |
| | 3 V | SOIC – D | Reel of 2000 | TL5209-30DR | TL520930 |
| | | SOT-223 – DCY | Reel of 2000 | TL5209-30DCYR | TC |
| | | TO-263 – KTT | Reel of 2000 | TL5209-30KTTR | TL5209-30 |
| | 3.3 V | SOIC – D | Reel of 2000 | TL5209-33DR | TL520933 |
| | | SOT-223 – DCY | Reel of 2000 | TL5209-33DCYR | TD |
| | | TO-263 – KTT | Reel of 2000 | TL5209-33KTTR | TL5209-33 |
| | 5 V | SOIC – D | Reel of 2000 | TL5209-50DR | TL520950 |
| | | SOT-223 – DCY | Reel of 2000 | TL5209-50DCYR | TE |
| | | TO-263 – KTT | Reel of 2000 | TL5209-50KTTR | TL5209-50 |
| | ADJ | SOIC – D | Reel of 2000 | TL5209DR | TL5209 |
| | | TO-263 – KTT | Reel of 2000 | TL5209KTTR | TL5209 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## BLOCK DIAGRAMS

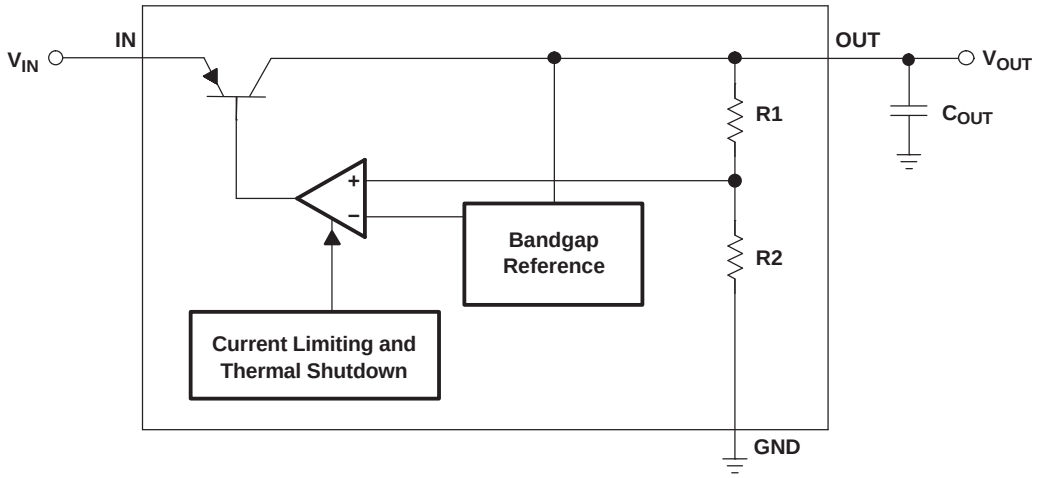



**Figure 1. Fixed Regulator (SOT-223 only)**

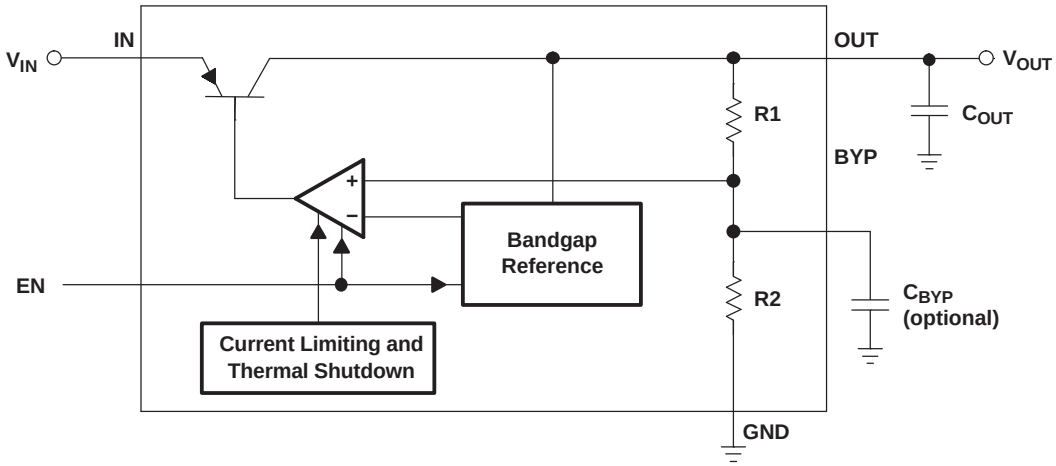



**Figure 2. Low-Noise Fixed Regulator (SOIC and TO-263 only)**

## BLOCK DIAGRAMS (continued)

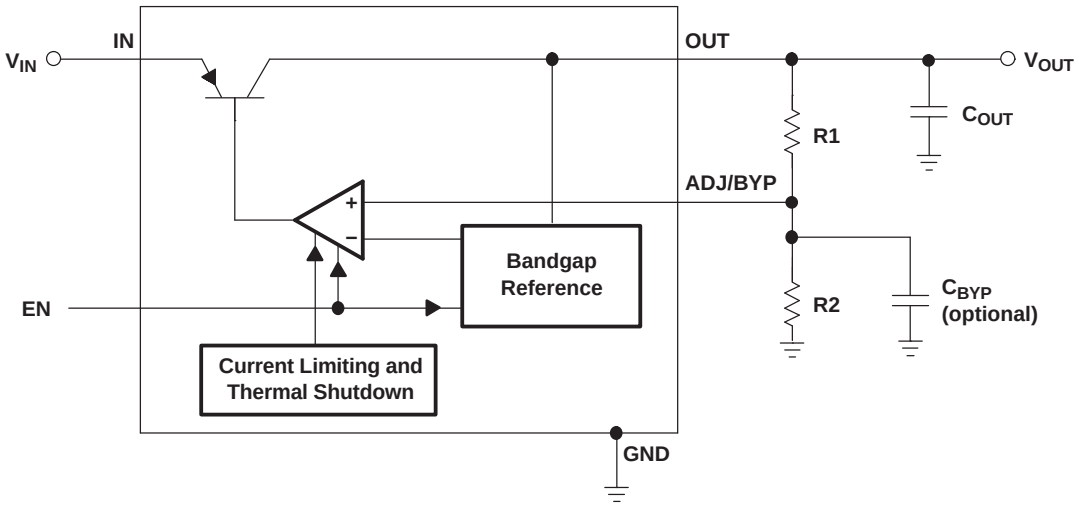



**Figure 3. Low-Noise Adjustable Regulator (SOIC and TO-263 only)**

## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_I$ | Continuous input voltage range | –20 | 20 | V |
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## Package Thermal Data(1)

| PACKAGE | BOARD | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|---|
| SOIC (D) | High K, JESD 51-7 | 97°C/W | 39°C/W |
| SOT-223 (DCY) | High K, JESD 51-7 | 53°C/W | 4°C/W |
| TO-263 (KTT) | High K, JESD 51-5 | 26.5°C/W | 31.8°C/W |

(1) Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.

## Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_I$ | Input voltage | 2.5 | 16 | V |
| $V_{EN}$ | Enable input voltage | 0 | $V_I$ | V |
| $T_J$ | Operating junction temperature range | –40 | 125 | °C |

## Electrical Characteristics

$V_{IN}$ = $V_{OUT}$ + 1 V, $C_{OUT}$ = 4.7 µF, $I_{OUT}$ = 1 mA, full range $T_J$ = –40°C to 125°C

| PARAMETER | | TEST CONDITIONS | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Output voltage accuracy | $V_{OUT}$ = 2.5 V for ADJ only | 25°C | –1 | | 1 | % |
| | | | Full range | –2 | | 2 | |
| $\alpha V_{OUT}$ | Output voltage temperature coefficient | | Full range | | 40 | | ppm/°C |
| | Line regulation | $V_{IN}$ = ($V_{OUT}$ + 1 V) to 16 V | 25°C | | 0.009 | 0.05 | %/V |
| | | | Full range | | | 0.1 | |
| | Load regulation | $I_{OUT}$ = 1 mA to 500 mA(1) | 25°C | | 0.05 | 0.5 | % |
| | | | Full range | | | 0.7 | |
| $V_{IN} – V_{OUT}$ | Dropout voltage(2) | $I_{OUT}$ = 1 mA | 25°C | | 45 | 60 | mV |
| | | | Full range | | | 80 | |
| | | $I_{OUT}$ = 50 mA | 25°C | | 115 | 175 | |
| | | | Full range | | | 250 | |
| | | $I_{OUT}$ = 100 mA | 25°C | | 150 | 250 | |
| | | | Full range | | | 300 | |
| | | $I_{OUT}$ = 500 mA | 25°C | | 350 | 500 | |
| | | | Full range | | | 600 | |
| $I_Q$ | Quiescent current | $V_{EN}$ ≥ 3 V, $I_{OUT}$ = 1 mA | 25°C | | 100 | 140 | µA |
| | | | Full range | | | 170 | |
| | | $V_{EN}$ ≥ 3 V, $I_{OUT}$ = 50 mA | 25°C | | 350 | 650 | |
| | | | Full range | | | 900 | |
| | | $V_{EN}$ ≥ 3 V, $I_{OUT}$ = 100 mA | 25°C | | 1.2 | 2 | mA |
| | | | Full range | | | 3 | |
| | | $V_{EN}$ ≥ 3 V, $I_{OUT}$ = 500 mA | 25°C | | 8 | 20 | |
| | | | Full range | | | 25 | |
| $I_{min}$ | Minimum load current(3) | | Full range | | | 1 | mA |
| $I_{SD}$ | Shutdown current | $V_{EN}$ ≤ 0.4 V | 25°C | | 0.05 | 3 | µA |
| | | $V_{EN}$ ≤ 0.18 V | 25°C | | 0.1 | | |
| | | | Full range | | | 8 | |
| | Ripple rejection | f = 120 Hz | 25°C | | 75 | | dB |
| $I_{LIMIT}$ | Current limit | $V_{OUT}$ = 0 V | 25°C | | 700 | 900 | mA |
| | | | Full range | | | 1000 | |
| $\Delta V_{OUT}/\Delta P_D$ | Thermal regulation(4) | $V_{IN}$ = 16 V, 500-mA load pulse for t = 10 ms | 25°C | | 0.05 | | %/W |
| $V_n$ | Output noise | $V_{OUT}$ = 2.5 V, $I_{OUT}$ = 50 mA, $C_{OUT}$ = 2.2 µF, $C_{BYP}$ = 0 | 25°C | | 500 | | nV/√Hz |
| | | $I_{OUT}$ = 50 mA, $C_{OUT}$ = 2.2 µF, $C_{BYP}$ = 470 pF(5) | 25°C | | 300 | | |
| $V_{EN}$ | Enable logic voltage | $V_{EN}$ = logic LOW (shutdown) | 25°C | | | 0.4 | V |
| | | | Full range | | | 0.18 | |
| | | $V_{EN}$ = logic HIGH (enabled) | 25°C | 2 | | | |

(1) Low duty cycle testing is used to maintain the junction temperature as close to the ambient temperature as possible. Changes in output voltage due to thermal effects are covered separately by the thermal regulation specification.
(2) Dropout is defined as the input to output differential at which the output drops 2% below its nominal value measured at 1-V differential.
(3) For stability across the input voltage and temperature. For ADJ versions, the minimum current can be set by R1 and R2.
(4) Thermal regulation is defined as the change in output voltage at a specified time after a change in power dissipation is applied, excluding line and load regulation effects.
(5) $C_{BYP}$ is optional and connected to the BYP/ADJ pin.

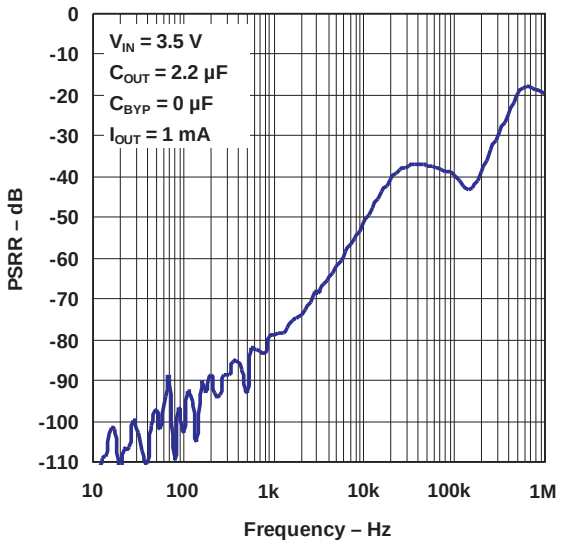
## Electrical Characteristics (continued)

$V_{IN} = V_{OUT} + 1$ V, $C_{OUT} = 4.7$ µF, $I_{OUT} = 1$ mA, full range $T_J = –40°C$ to $125°C$

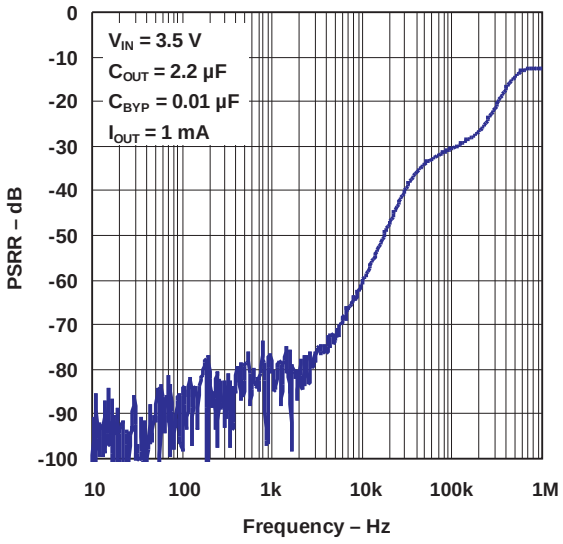
| PARAMETER | | TEST CONDITIONS | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{EN}$ | Enable input current | $V_{EN} \le 0.4$ V (shutdown) | 25°C | | 0.01 | –1 | µA |
| | | $V_{EN} \le 0.18$ V (shutdown) | Full range | | 0.01 | –2 | |
| | | $V_{EN} \ge 2$ V (enabled) | 25°C | | 5 | 20 | |
| | | | Full range | | | 25 | |

## TYPICAL CHARACTERISTICS

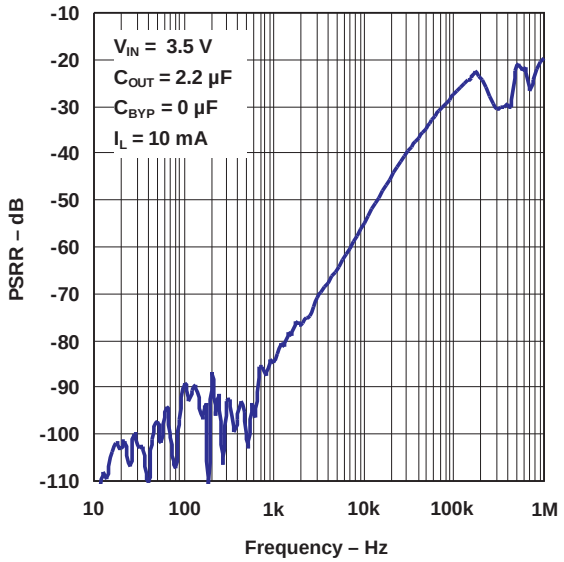
**POWER-SUPPLY REJECTION RATIO**



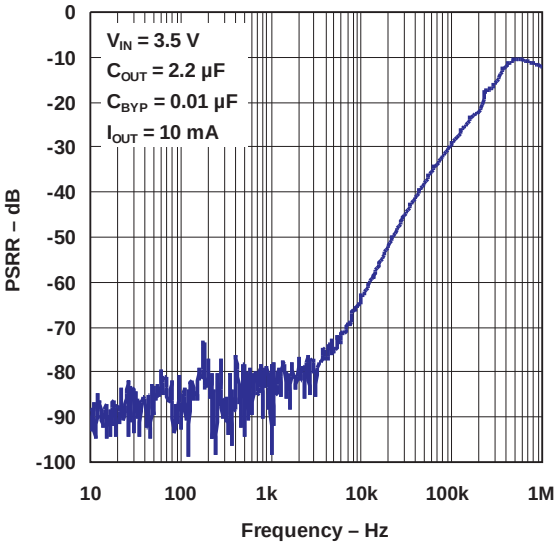

**POWER-SUPPLY REJECTION RATIO**




**POWER-SUPPLY REJECTION RATIO**

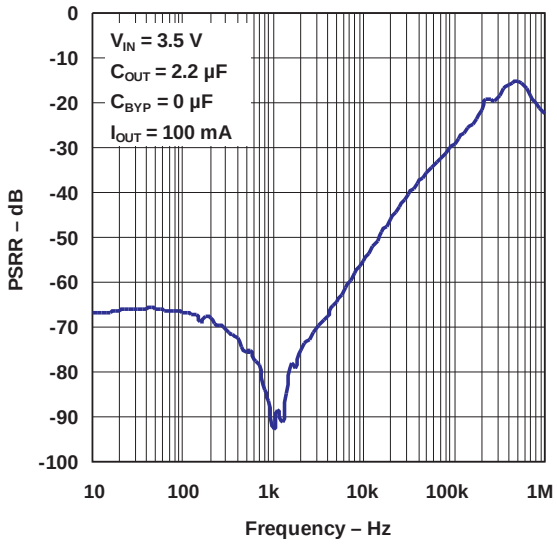



**POWER-SUPPLY REJECTION RATIO**

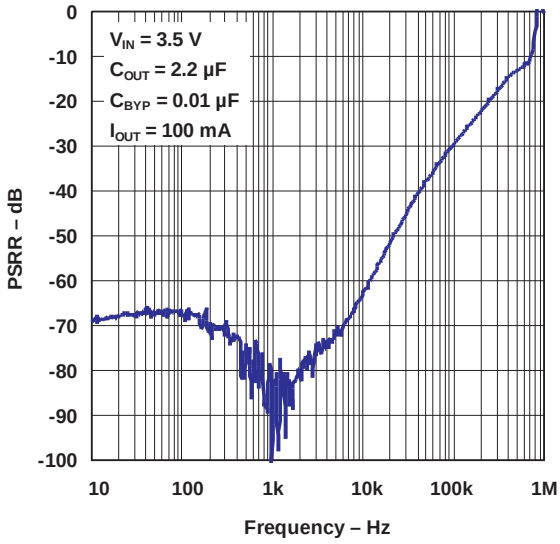


## TYPICAL CHARACTERISTICS (continued)

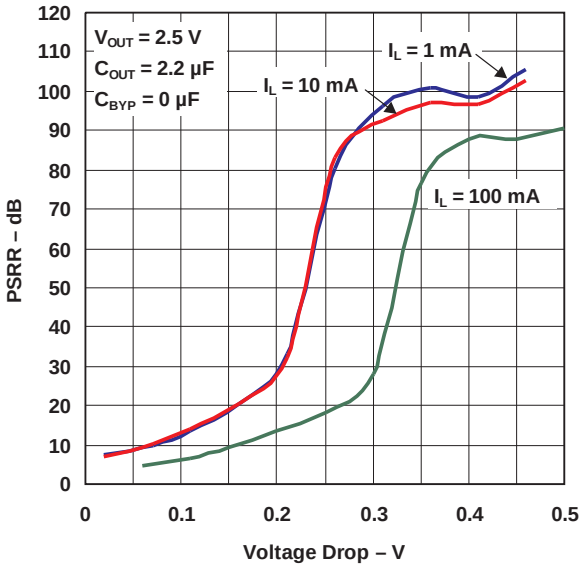
**POWER-SUPPLY REJECTION RATIO**




**POWER-SUPPLY REJECTION RATIO**




**POWER-SUPPLY RIPPLE REJECTION vs VOLTAGE DROP**




**POWER-SUPPLY RIPPLE REJECTION vs VOLTAGE DROP**

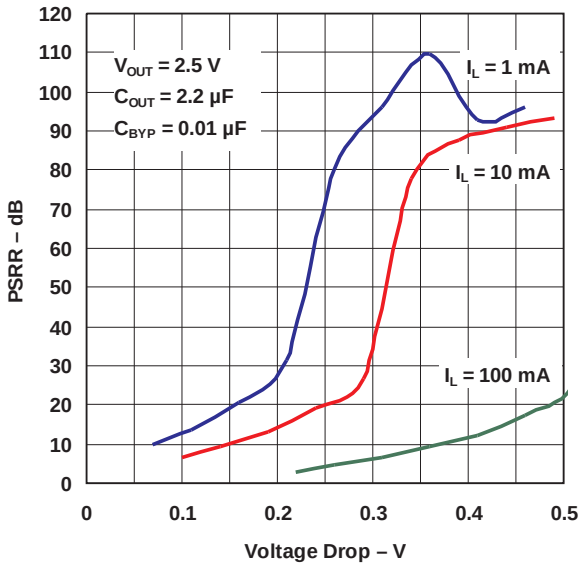
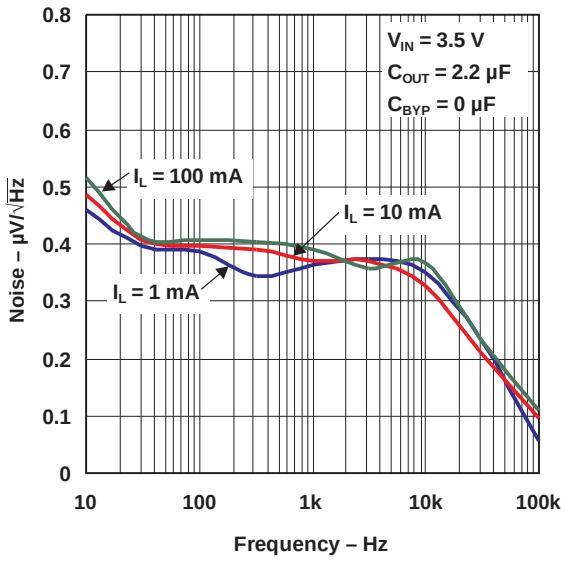


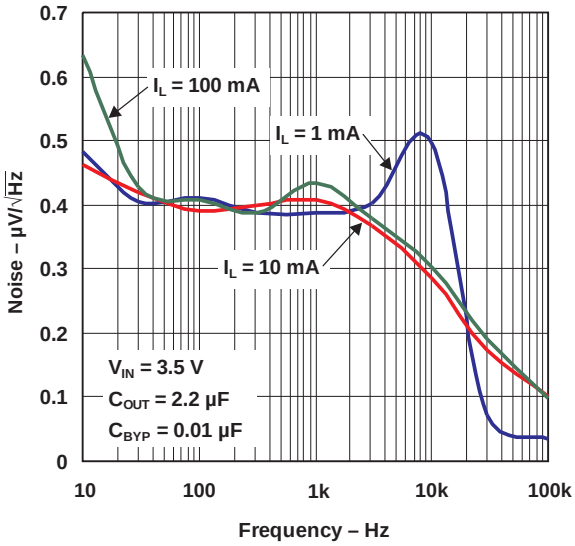

**Figure 4.**

## TYPICAL CHARACTERISTICS (continued)

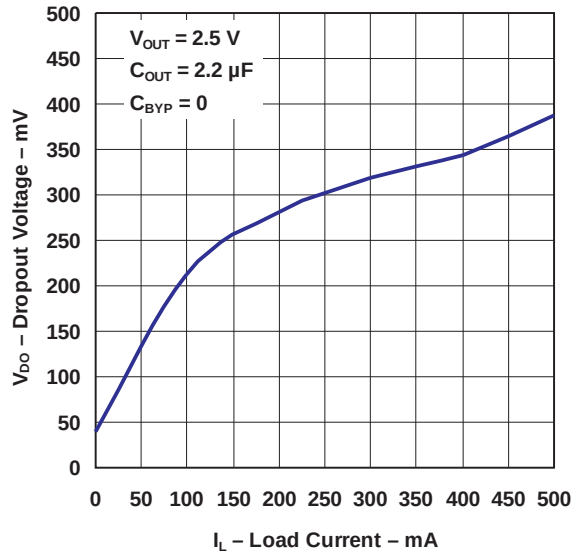
**NOISE PERFORMANCE**



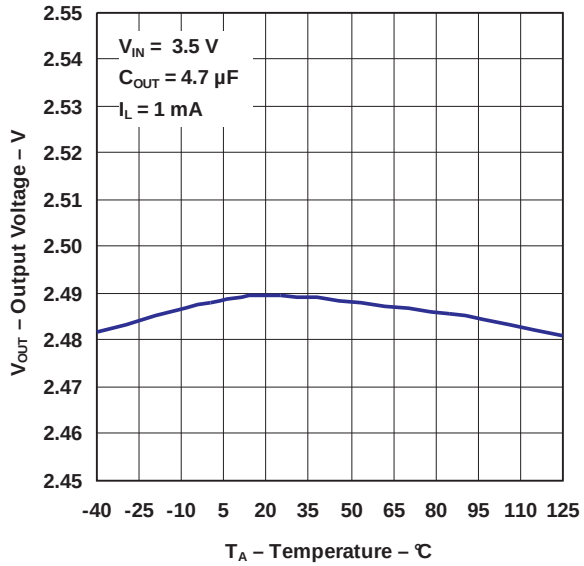

**NOISE PERFORMANCE**




**DROPOUT VOLTAGE vs LOAD CURRENT**

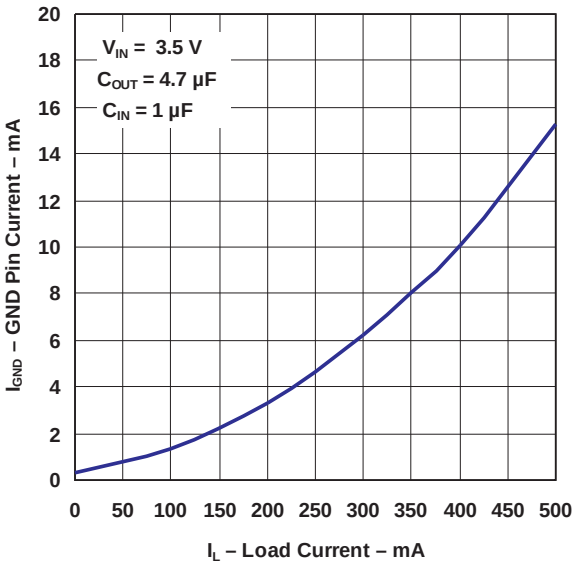



**OUTPUT VOLTAGE vs TEMPERATURE**

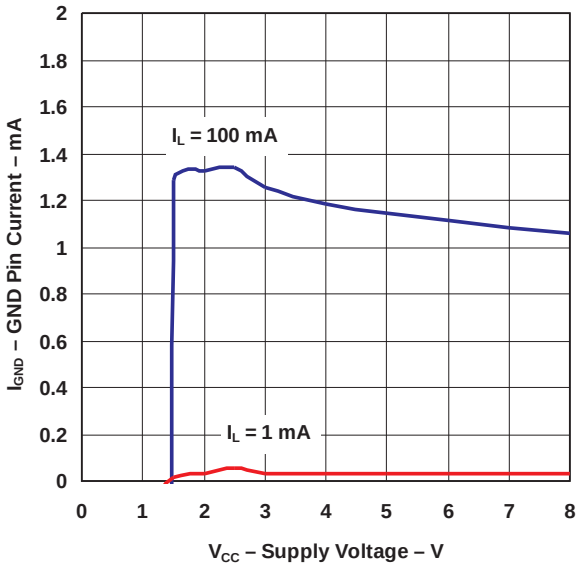


## TYPICAL CHARACTERISTICS (continued)

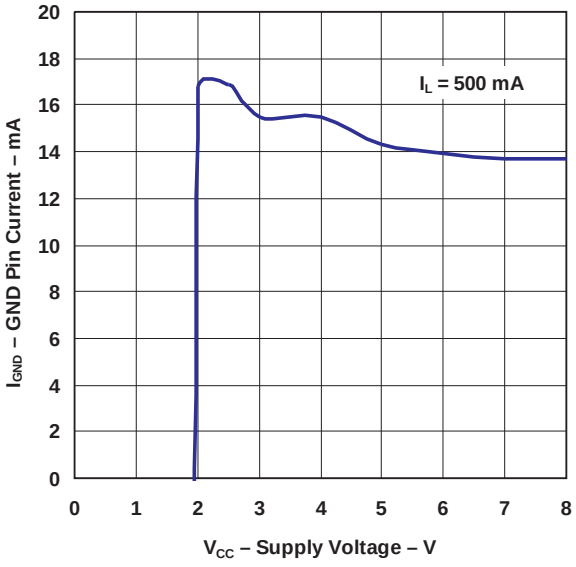
**GROUND CURRENT vs LOAD CURRENT**



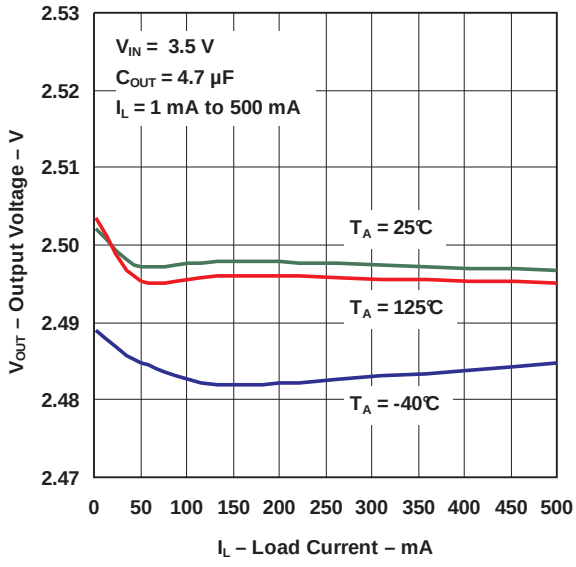

**GROUND CURRENT vs SUPPLY VOLTAGE**




**GROUND CURRENT vs SUPPLY VOLTAGE**

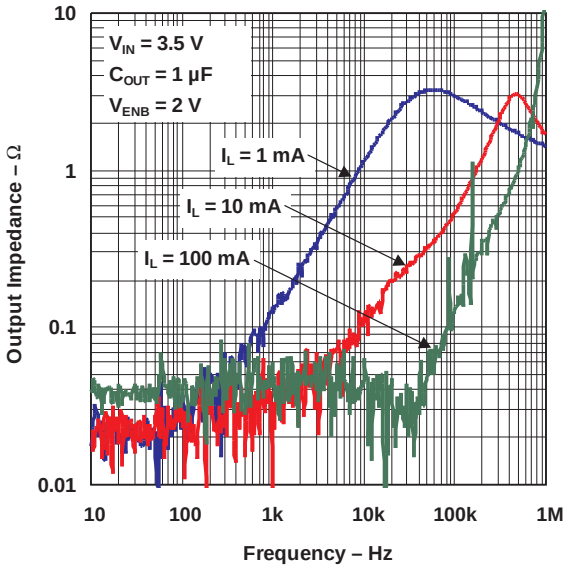



**OUTPUT VOLTAGE vs LOAD CURRENT**

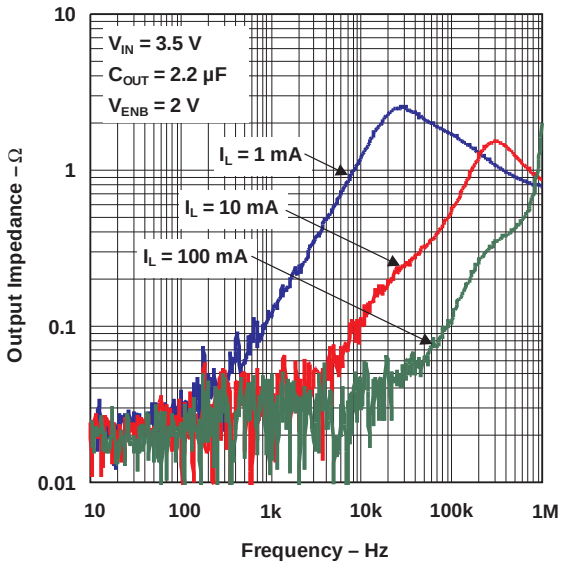


## TYPICAL CHARACTERISTICS (continued)

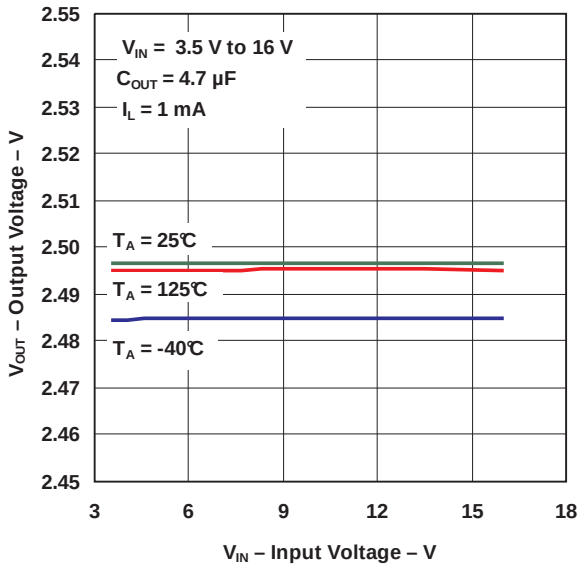
### OUTPUT IMPEDANCE vs FREQUENCY



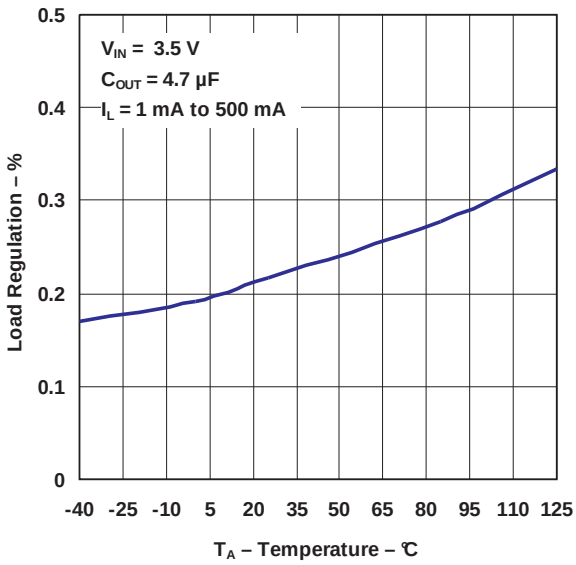

### OUTPUT IMPEDANCE vs FREQUENCY




### OUTPUT VOLTAGE vs INPUT VOLTAGE

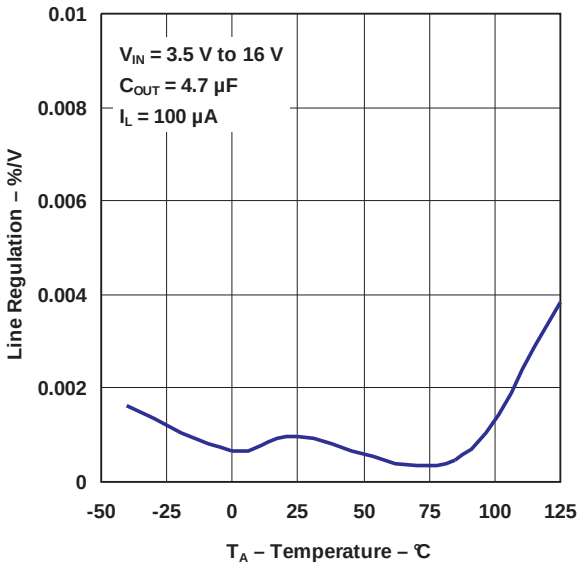



### LOAD REGULATION

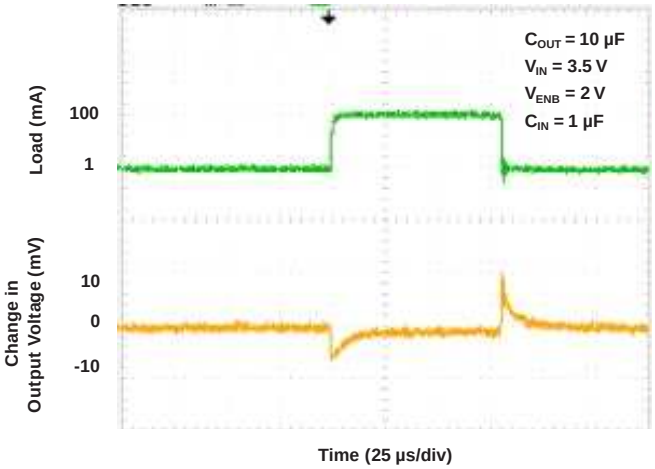


## TYPICAL CHARACTERISTICS (continued)

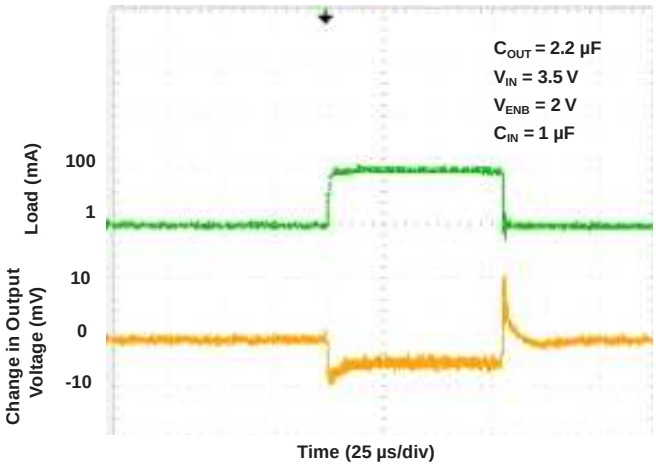
### LINE REGULATION



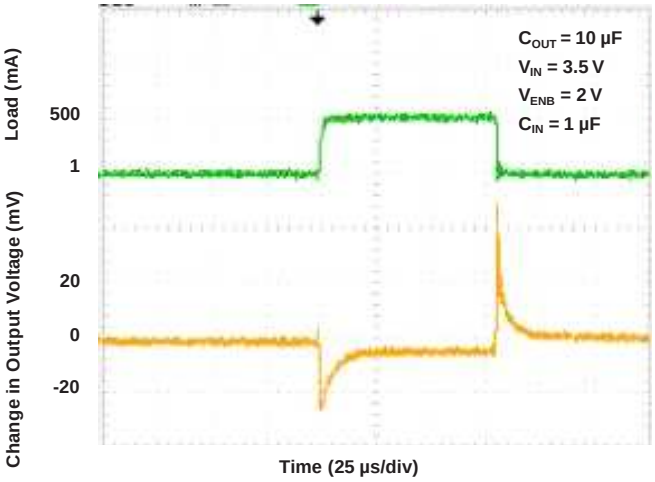

### LOAD TRANSIENT RESPONSE




### LOAD TRANSIENT RESPONSE

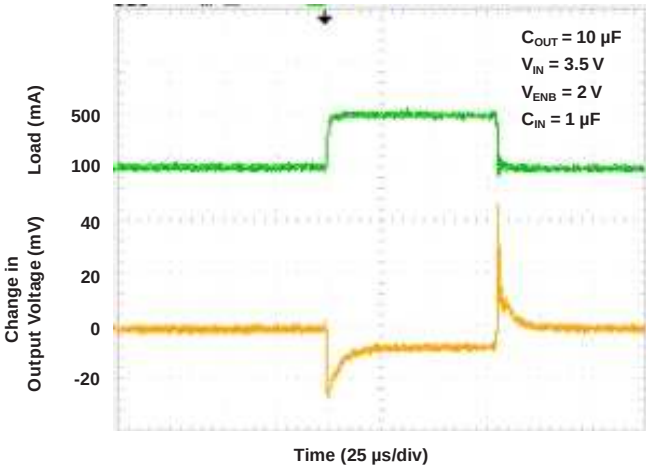



### LOAD TRANSIENT RESPONSE

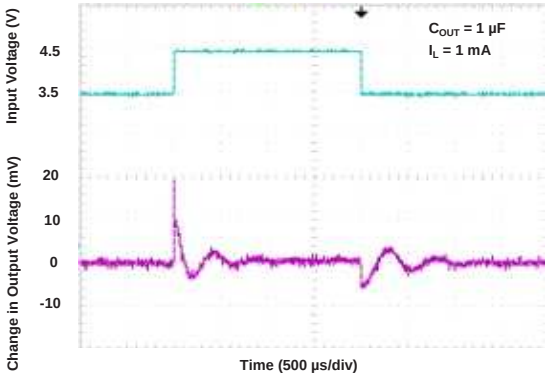


## TYPICAL CHARACTERISTICS (continued)

### LOAD TRANSIENT RESPONSE




### LINE TRANSIENT RESPONSE

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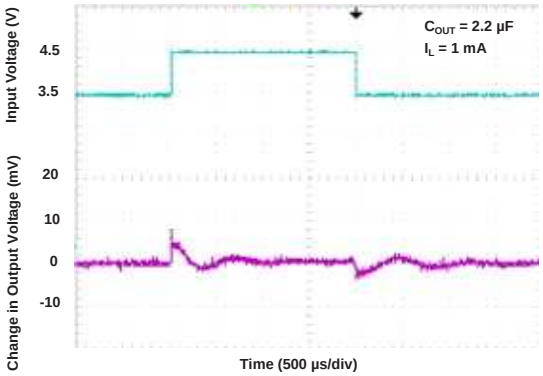


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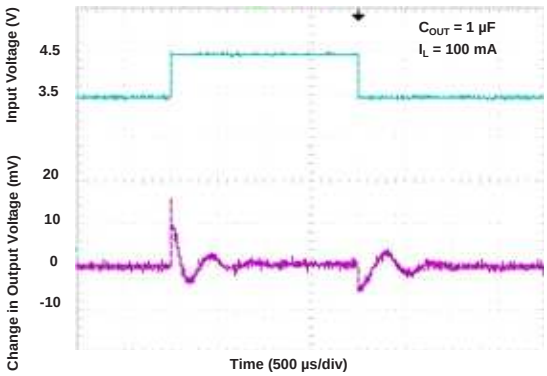


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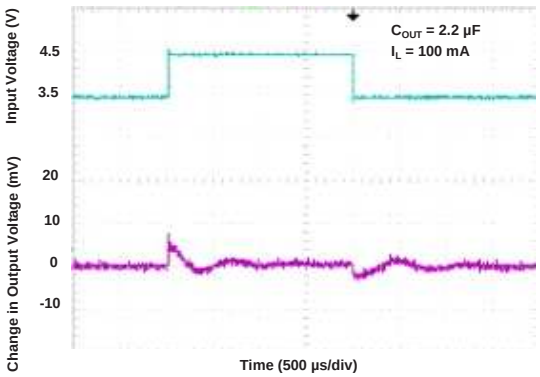


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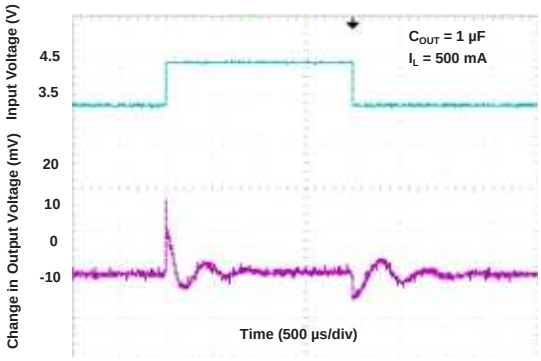
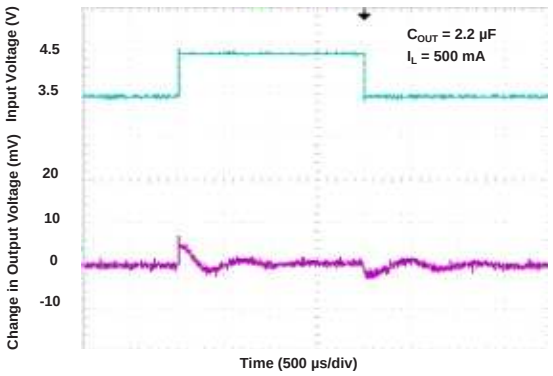
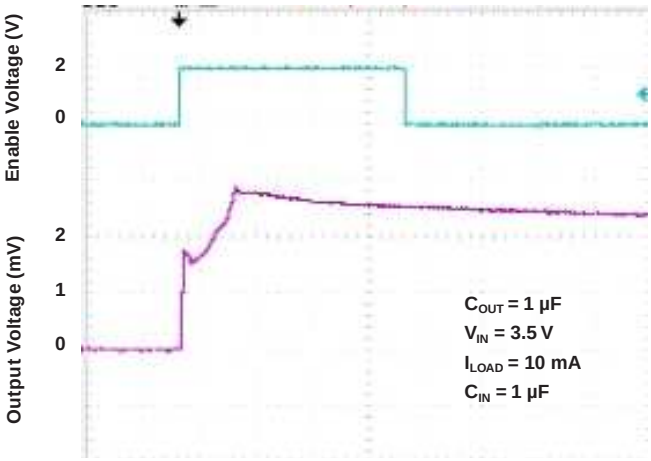


## TYPICAL CHARACTERISTICS (continued)

### LINE TRANSIENT RESPONSE




### TURN-ON TIME

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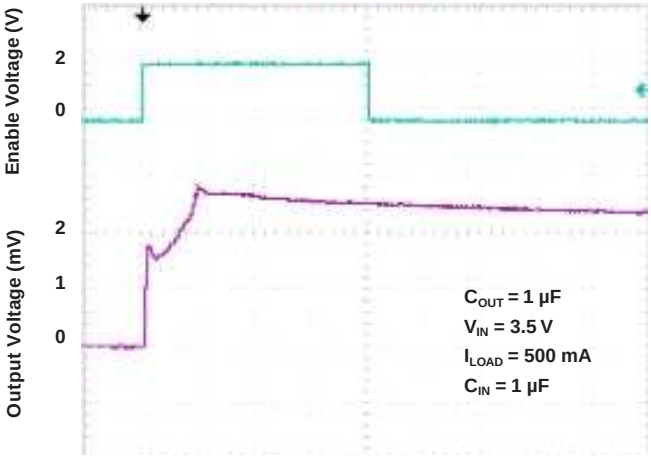


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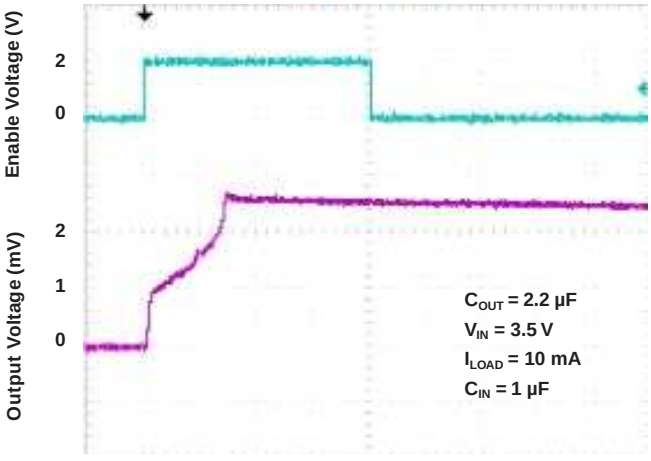
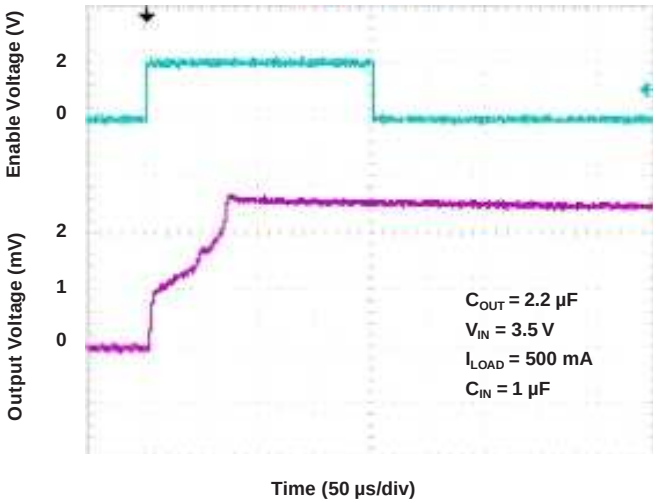
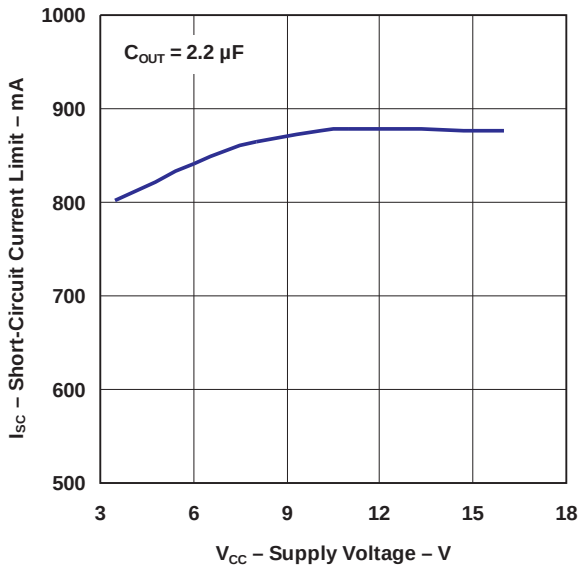


## TYPICAL CHARACTERISTICS (continued)

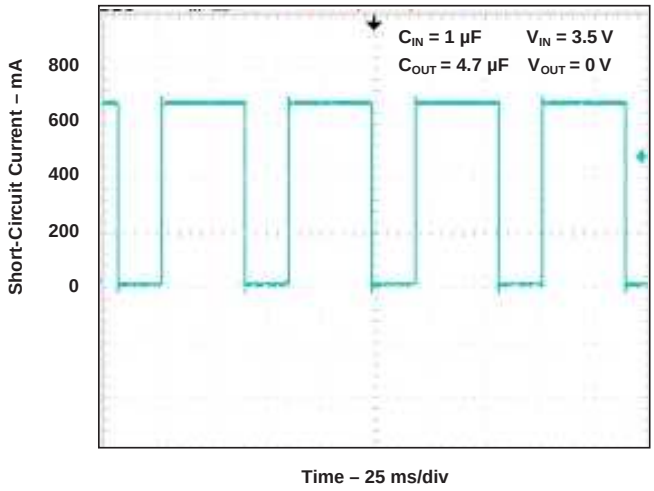
**TURN-ON TIME**



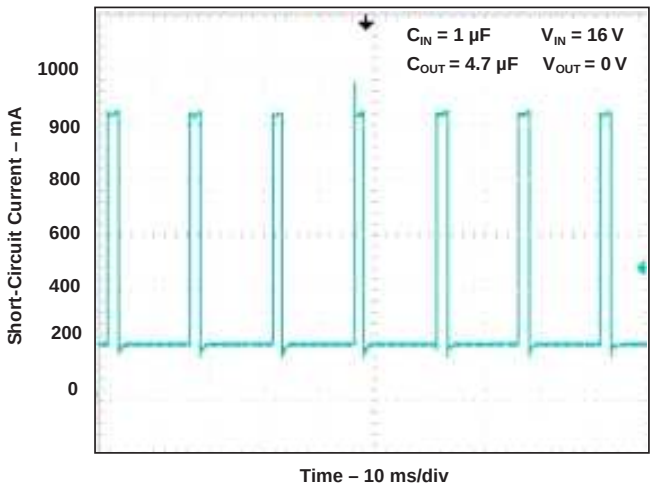

**SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE**




**SHORT-CIRCUIT CURRENT vs TIME**




**SHORT-CIRCUIT CURRENT vs TIME**



## TYPICAL APPLICATION CIRCUITS

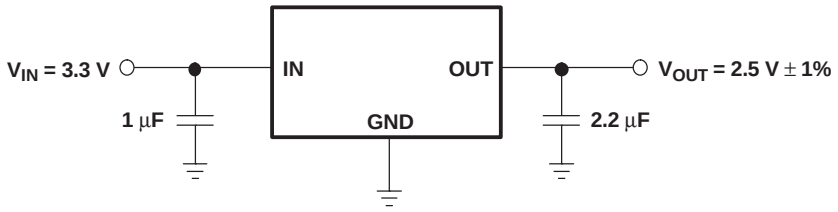



**Figure 5. Fixed 2.5-V Regulator (TL5209-25, SOT-223)**

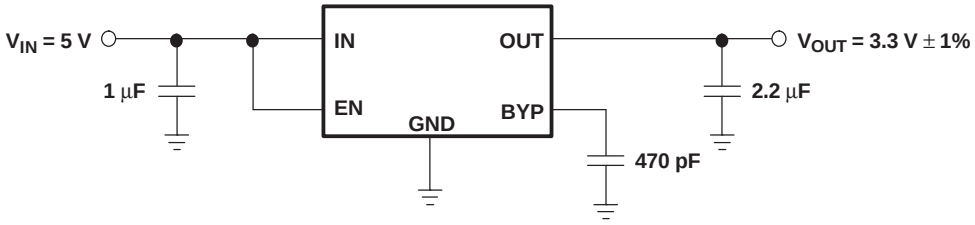
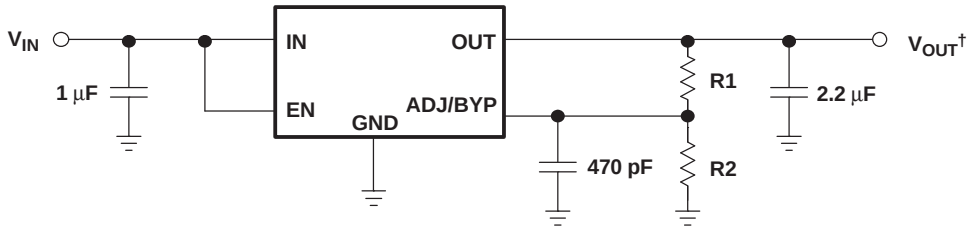



**Figure 6. Fixed 3.3-V Low-Noise Regulator (TL5209-33, SOIC-8, or TO-263)**




A. $V_{OUT}$ = 1.242 V (1 + R2/R1)

B. R2 should be ≤ 470 kΩ for optimal performance.

**Figure 7. Low-Noise Adjustable Regulator (TL5209, SOIC-8, or TO-263)**

## APPLICATION INFORMATION

### Enable/Shutdown

The enable function is only available in the SOIC (D) and TO-263 (KTT) packages. The EN pin is CMOS-logic compatible. When EN is held high (>2 V), the regulator is active. Likewise, applying a low signal (<0.4 V at 25°C) to EN or leaving it open shuts down the regulator. If the enable/shutdown feature is not needed, EN should be tied to $V_{IN}$.

### Input Capacitor

If the input of the regulator is located more than ten inches from the power-supply filter, or if a battery is used to power the regulator, a minimum 1-µF input capacitor is recommended.

### Output Capacitor

As with all PNP regulators, an output capacitor is needed for stability. The required minimum size of this output capacitor depends on several factors, one of which is whether a bypass capacitor is used.

- With no bypass capacitor, a minimum $C_{OUT}$ of 1 µF is recommended.
- With a bypass capacitor of 470 pF (see Figure 6), a minimum $C_{OUT}$ of 2.2 µF is recommended.
- Larger values of $C_{OUT}$ are beneficial, because they improve the regulator transient response.

Another factor that can determine the minimum size of the output capacitor is the load current. At low loads, a smaller output capacitor is needed for stability.

The equivalent series resistance (ESR) of the output capacitor also can affect regulator stability. $C_{OUT}$ should have an ESR of ≈1 Ω, and it should have a resonant frequency above 1 MHz. Too low an ESR can cause the output to have a low-amplitude oscillation and/or underdamped transient response. Most tantalum or aluminum electrolytic capacitors can be used for the output capacitors. However, care should be used at low temperatures, because aluminum electrolytics use electrolytes that can freeze at low temperature (≈ –30°C). Solid tantalum capacitors do not exhibit this problem and should be used below –25°C.

### Bypass Capacitor

An optional bypass capacitor, $C_{BYP}$, can be externally connected to the regulator via the BYP pin for improved noise performance (only for SOIC and TO-263 packages). Connected to the internal voltage divider and the error amplifier of the regulator, this bypass capacitor filters the noise of the internal reference and reduces the noise effects on the error amplifier. The overall result is a significant drop in output noise of the regulator. A 470-pF bypass capacitor is recommended.

Adding a bypass capacitor has several effects on the regulator that must be taken into account. First, the bypass capacitor reduces the phase margin of the regulator and, thus, the minimum $C_{OUT}$ needs to be increased to 2.2 µF, as previously mentioned. Second, upon startup of the regulator, the bypass capacitor has an effect on the regulator turn-on time. If a slow ramp-up of the output is needed, larger values of $C_{BYP}$ should be used. Conversely, if a fast ramp-up of the output is needed, use a smaller $C_{BYP}$ or none at all.

If a bypass capacitor is not needed, BYP should be left open.

### Low-Voltage Operation

When using the TL5209-18 and TL5209-25 in voltage-sensitive applications, special considerations are required. If appropriate output and bypass capacitors are not chosen properly, these devices may experience a temporary overshoot of their nominal voltages.

At start-up, the full input voltage is initially applied across the regulator pass transistor, causing it to be temporarily fully turned on. By contrast, the error amplifier and voltage-reference circuits, being powered from the output, are not powered up as fast. In order to slow down the output ramp and give the error amplifier time to respond, select larger values of output and bypass capacitors. The longer ramp time of the output allows the regulator enough time to respond and keeps the output from overshooting its nominal value.

To prevent an overshoot when starting up into a light load (≈100 µA), 4.7-µF and 470-pF capacitors are recommended for the output and bypass capacitors, respectively. At higher loads, 10-µF and 470-pF capacitors should be used.

## APPLICATION INFORMATION (continued)

If the application is not too sensitive to regulator overshoot, both the output capacitor and bypass capacitor (if applicable) can be reduced.

### Adjustable Output Version

For the adjustable version, the output voltage is set by two external resistors forming a voltage divider connected to the output and the ADJ pin (see Figure 7). $V_{OUT}$ is set based on the equation:

$V_{OUT} = 1.242\ V(1 + R2/R1)$

Although ADJ represents a high-impedance input, limit R2 to $\leq 470\ k\Omega$ for optimum performance.

# PACKAGE OPTION ADDENDUM

2-Nov-2006

## PACKAGING INFORMATION

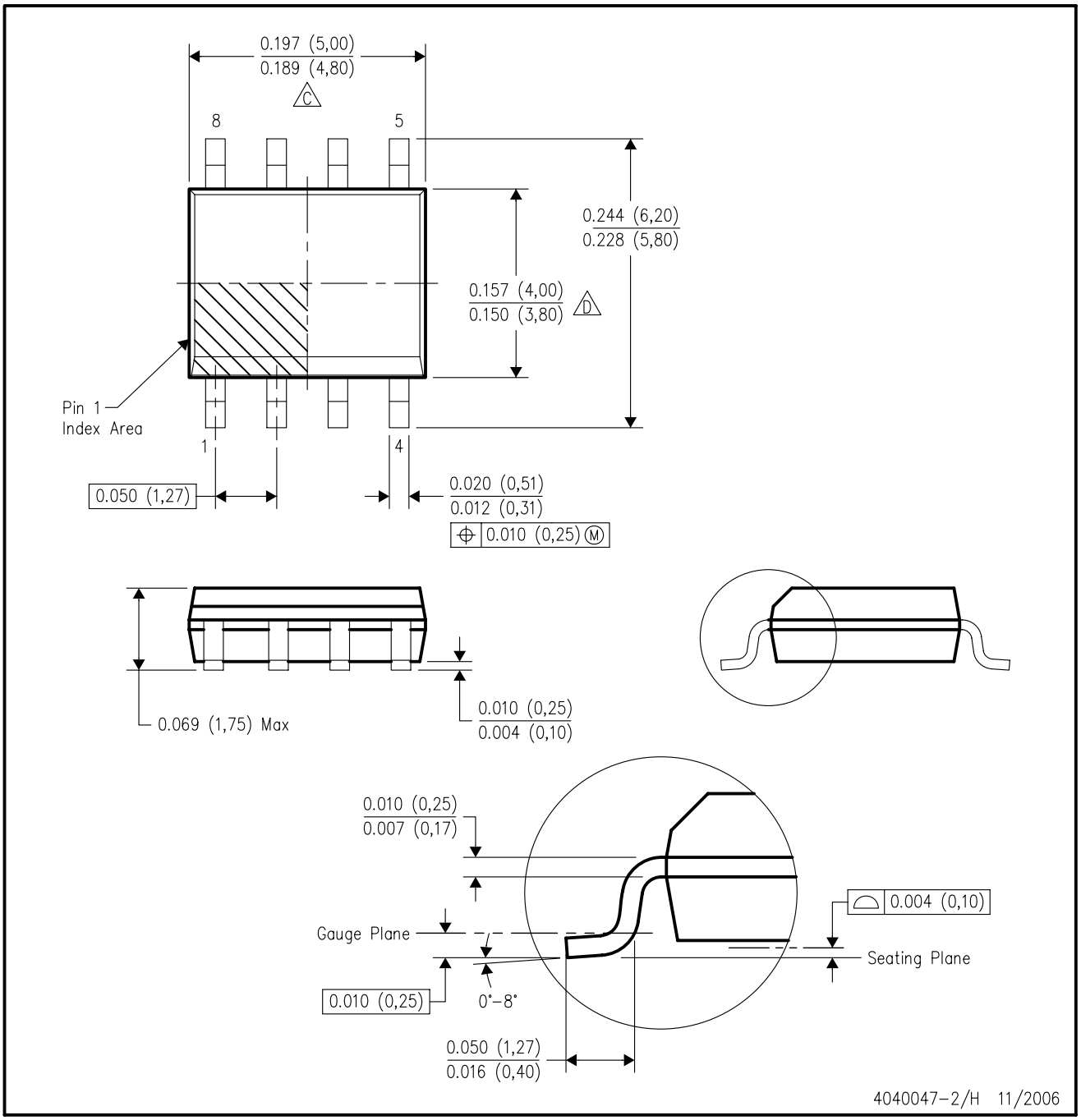
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TL5209DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5209DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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