Rev 0; 9/06

DALLAS SEMICONDUCTOR MAXIM

Two-Channel, Push-Pull CCFL Controller

General Description

The DS3992 is a low-cost, two-channel controller for cold-cathode fluorescent lamps (CCFLs) that are used to backlight liquid crystal displays (LCDs). The DS3992 can drive multiple CCFLs per channel, making it ideal for 4- and 6-lamp LCD PC monitor and TV applications.

The DS3992 uses a push-pull drive scheme to convert a DC voltage (5V to 24V) to the high voltage (300V_{RMS} to 1400V_{RMS}) AC waveform that is required to power the CCFLs. The push-pull drive scheme uses a minimal number of external components, which reduces component and assembly cost and makes the printed circuit board (PC board) design easy to implement. The push-pull drive scheme also provides an efficient DC-to-AC conversion and produces near-sinusoidal waveforms.

Applications

LCD PC Monitors

LCD-TVs

Features

- **Two-Channel CCFL Controller for Backlighting LCD Panels for PC Monitors and LCD-TVs**
- **Minimal BOM Provides Low-Cost Inverter Solution**
- **Per-Channel Lamp Fault Monitoring for Lamp-Open, Lamp Overcurrent, Failure to Strike, and Overvoltage Conditions**
- **Accurate (±10%) On-Board Oscillator for Lamp Frequency (40kHz to 80kHz)**
- **Accurate (±10%) On-Board Oscillator for DPWM Burst-Dimming Frequency (90Hz to 220Hz or 180Hz to 440Hz)**
- **Device Supply Undervoltage Lockout**
- **Inverter Supply Undervoltage Lockout**
- **Burst-Dimming Soft-Start Minimizes Audible Transformer Noise**
- **Strike Frequency Boost**
- **100% to < 10% Dimming Range**
- **4.5V to 5.5V Single-Supply Operation**
- **-40°C to +85°C Temperature Range**
- **16-Pin SO Package (150 mils)**

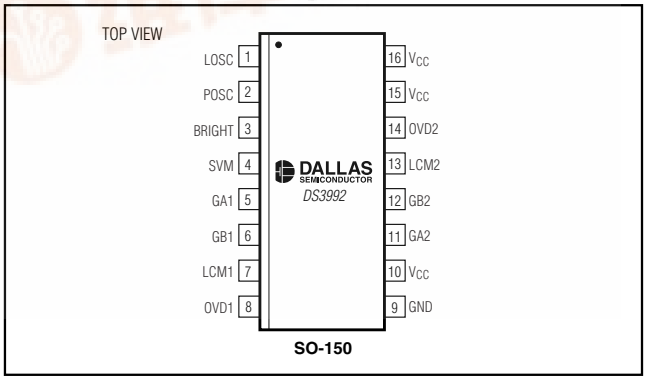
Ordering Information

PART	TEMP RANGE	DIMMING FREQUENCY RANGE	BRIGHT POLARITY	PIN-PACKAGE
DS3992Z-09P+	-40°C to +85°C	90Hz to 220Hz	Positive	16 SO-16 (150 mils)
DS3992Z-09N+	-40°C to +85°C	90Hz to 220Hz	Negative	16 SO-16 (150 mils)
DS3992Z-18P+	-40°C to +85°C	180Hz to 440Hz	Positive	16 SO-16 (150 mils)
DS3992Z-18N+	-40°C to +85°C	180Hz to 440Hz	Negative	16 SO-16 (150 mils)
DS3992Z-09P+T&R	-40°C to +85°C	90Hz to 220Hz	Positive	16 SO-16 (150 mils)
DS3992Z-09N+T&R	-40°C to +85°C	90Hz to 220Hz	Negative	16 SO-16 (150 mils)
DS3992Z-18P+T&R	-40°C to +85°C	180Hz to 440Hz	Positive	16 SO-16 (150 mils)
DS3992Z-18N+T&R	-40°C to +85°C	180Hz to 440Hz	Negative	16 SO-16 (150 mils)

+Denotes lead-free package.
T&R denotes tape-and-reel package.

Typical Operating Circuits appear at end of data sheet.

Pin Configuration



SO-150

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Relative to Ground.....-0.5V to +6.0V
Voltage on Any Leads Other
Than V_{CC} .....0.5V to (V_{CC} + 0.5V), not to exceed +6.0V

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.5		5.5	V
SVM Voltage Range	V_{SVM}		-0.3		V_{CC} + 0.3	V
BRIGHT Voltage Range	V_{BRIGHT}		-0.3		V_{CC} + 0.3	V
LCM Voltage Range	V_{LCM}	(Note 2)	-0.3		V_{CC} + 0.3	V
OVD Voltage Range	V_{OVD}	(Note 2)	-0.3		V_{CC} + 0.3	V
Gate-Driver Output Charge Loading	Q_G				20	nC

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	G_A, G_B loaded with 600pF, 2 channels active		8	16	mA
Low-Level Output Voltage (GA, GB)	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage (GA, GB)	V_{OH1}	I_{OH1} = -1mA	V_{CC} - 0.4			V
UVLO Threshold: V_{CC} Rising	V_{UVLOR}				4.3	V
UVLO Threshold: V_{CC} Falling	V_{UVLOF}		3.7			V
UVLO Hysteresis	V_{UVLOH}			100		mV
SVM Falling-Edge Threshold	V_{SVM}		1.9	2.0	2.1	V
SVM Hysteresis	V_{SVMH}			150		mV
LCM and OVD DC Bias Voltage	V_{DCB}			1.35		V
LCM and OVD Input Resistance	R_{DCB}			50		kΩ
Lamp-Off Threshold	V_{LOT}	(Note 3)	1.65	1.75	1.85	V
Lamp Over Current	V_{LOC}	(Note 3)	3.15	3.35	3.55	V
Lamp Regulation Threshold	V_{LRT}	(Note 3)	2.25	2.35	2.45	V
OVD Threshold	V_{OVDT}	(Note 3)	2.25	2.35	2.45	V
Lamp Frequency Range	$f_{LFS:OSC}$		40		80	kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Lamp Frequency Tolerance	$f_{LFS:TOL}$	LOSC resistor ±2% over temperature	-10		+10	%
DPWM Frequency Range	$f_{DSR:OSC}$	DS3992Z-09P/N	90		220	Hz
		DS3992Z-18P/N	180		440	
DPWM Frequency Tolerance	$f_{DSR:TOL}$	POSC resistor ±2% over temperature	-10		+10	%
BRIGHT Voltage: Minimum Brightness	V_{BMIN}	DS3992Z-09P / DS3992Z-18P			0.5	V
		DS3992Z-09N / DS3992Z-18N	2.0			
BRIGHT Voltage: Maximum Brightness	V_{BMAX}	DS3992Z-09P / DS3992Z-18P	2.0			V
		DS3992Z-09N / DS3992Z-18N			0.5	
Gate-Driver Output Rise/Fall Time	t_R / t_F	C_L = 600pF		50	100	ns
GAn and GBn Duty Cycle					44	%
Strike Time	t_{STRIKE}		500			ms

Note 1: All voltages are referenced to ground unless otherwise noted. Currents into the I.C. are positive, out of the I.C. negative.

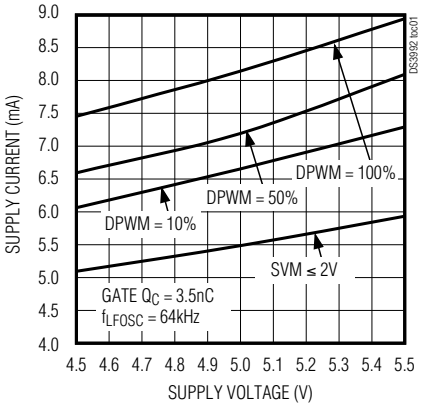
Note 2: During fault conditions, the AC-coupled feedback values are allowed to be below the Absolute Maximum Rating of the LCM or OVD pin for up to 1s.

Note 3: Voltage with respect to V_{DCB}.

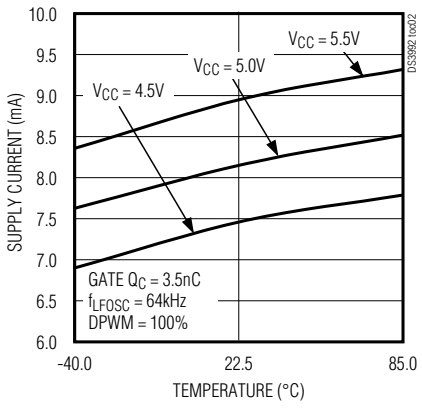
Typical Operating Characteristics

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

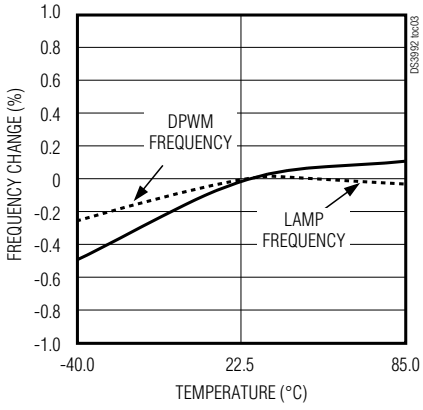
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



ACTIVE SUPPLY CURRENT vs. TEMPERATURE



INTERNAL FREQUENCY CHANGE vs. TEMPERATURE

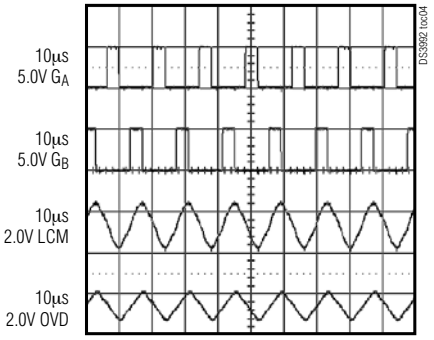


Two-Channel, Push-Pull CCFL Controller

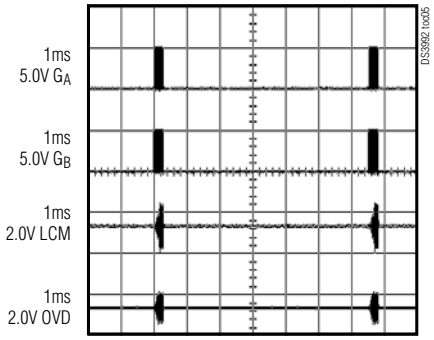
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

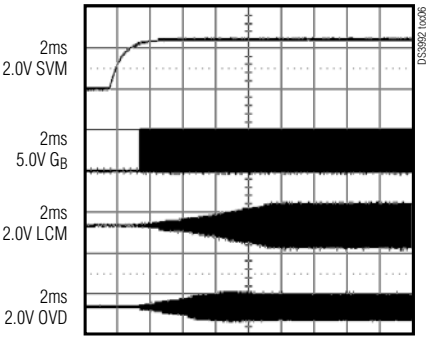
TYPICAL OPERATION AT 16V



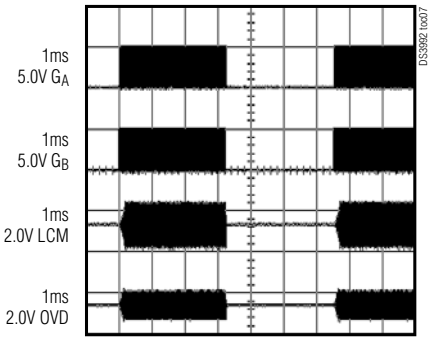
BURST DIMMING AT 150Hz AND 10%



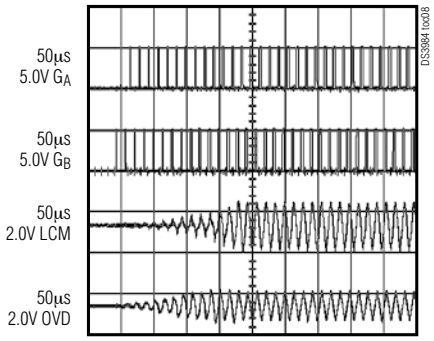
TYPICAL STARTUP WITH SVM



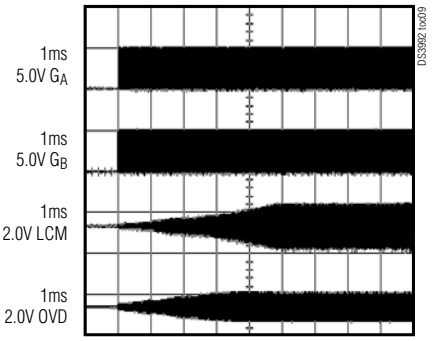
BURST DIMMING AT 150Hz AND 50%



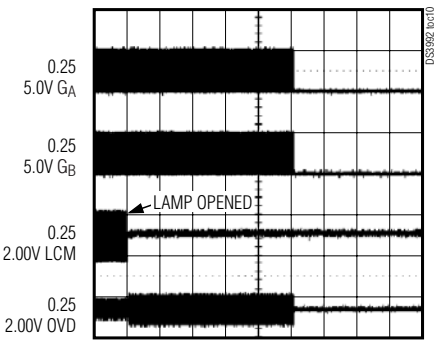
SOFT-START AT V_{INV} = 16V



LAMP STRIKE—EXPANDED VIEW



LAMP OUT (LAMP OPENED), AUTORETRY DISABLED



Pin Description

PIN NUMBER	NAME	I/O	FUNCTION
1	LOSC	—	**Lamp Oscillator Resistor Adjust.** A resistor (R_{LOSC}) to ground on this pin sets the frequency of the lamp oscillator ($f_{LFS:OSC}$). [R_{LOSC} x $f_{LFS:OSC}$ = 1.6E9].
2	POSC	—	**Burst Dimming DPWM Oscillator Resistor Adjust.** A resistor (RPOSC) to ground on this lead sets the frequency ($f_{DSR:OSC}$) of the burst-dimming DPWM oscillator. [R_{POSC} x $f_{DSR:OSC}$ = 4.0E6 for DS3992Z-09P and DS3992Z-09N and R_{POSC} x $f_{DSR:OSC}$ = 8.0E6 for DS3992Z-18P and DS3992Z-18N].
3	BRIGHT	I	**Lamp Brightness Control.** An analog voltage at this input controls the lamp brightness. See Table 1 for details.
4	SVM	I	**Supply Voltage Monitor.** The DC inverter supply voltage is monitored by an external resistor divider. The resistor-divider should be set such that it provides 2V at this pin for the minimum allowable range of the DC inverter supply. Pulling this input below 2V will turn the lamps off and reset the controller. Connect to V_{CC} if not used.
5	GA1	O	**MOSFET Gate Drive A for Channel 1.** Connect directly to the gate of a logic-level mode n-channel MOSFET.
6	GB1	O	**MOSFET Gate Drive B for Channel 1.** Connect directly to the gate of a logic-level mode n-channel MOSFET.
7	LCM1	I	**Lamp Current Monitor Input for Channel 1.** Lamp current is monitored by a resistor placed in series with the low-voltage side of the lamp.
8	OVD1	I	**Over Voltage Detection for Channel 1.** Lamp voltage is monitored by a capacitor divider placed on the high-voltage side of the lamp.
9	GND	—	**Signal Ground**
10	V_{CC}	—	**Supply.** 4.5V to 5.5V.
11	GA2	O	**MOSFET Gate Drive A for Channel 2.** Connect directly to the gate of a logic-level mode n-channel MOSFET.
12	GB2	O	**MOSFET Gate Drive B for Channel 2.** Connect directly to the gate of a logic-level mode n-channel MOSFET.
13	LCM2	I	**Lamp Current Monitor Input for Channel 2.** Lamp current is monitored by a resistor placed in series with the low-voltage side of the lamp.
14	OVD2	I	**Overvoltage Detection for Channel 2.** Lamp voltage is monitored by a capacitor divider placed on the high-voltage side of the lamp.
15	V_{CC}	—	**Supply.** 4.5V to 5.5V.
16	V_{CC}	—	**Supply.** 4.5V to 5.5V.

Two-Channel, Push-Pull CCFL Controller

Functional Diagrams

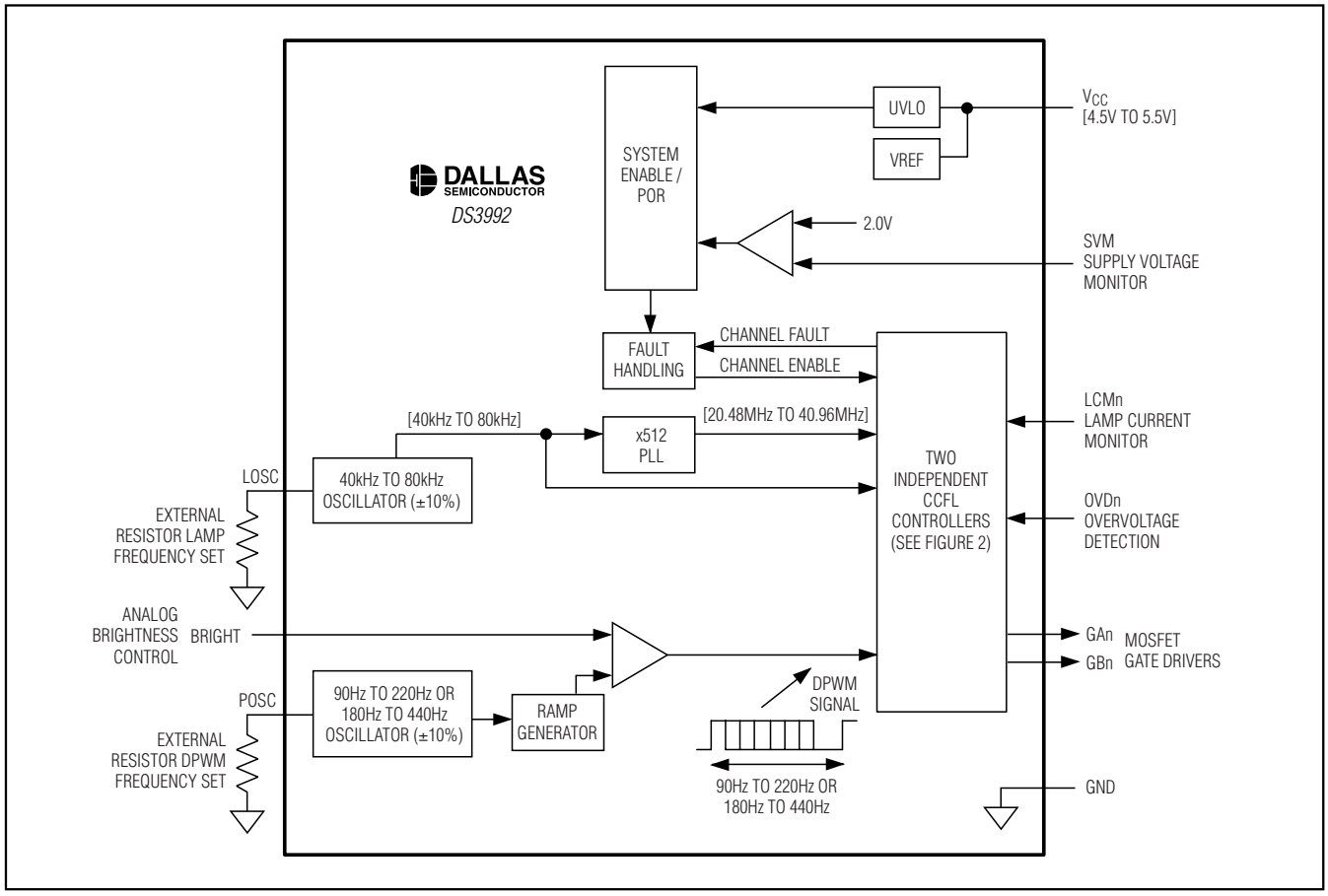


Figure 1. DS3992 Functional Diagram

Functional Diagrams (continued)

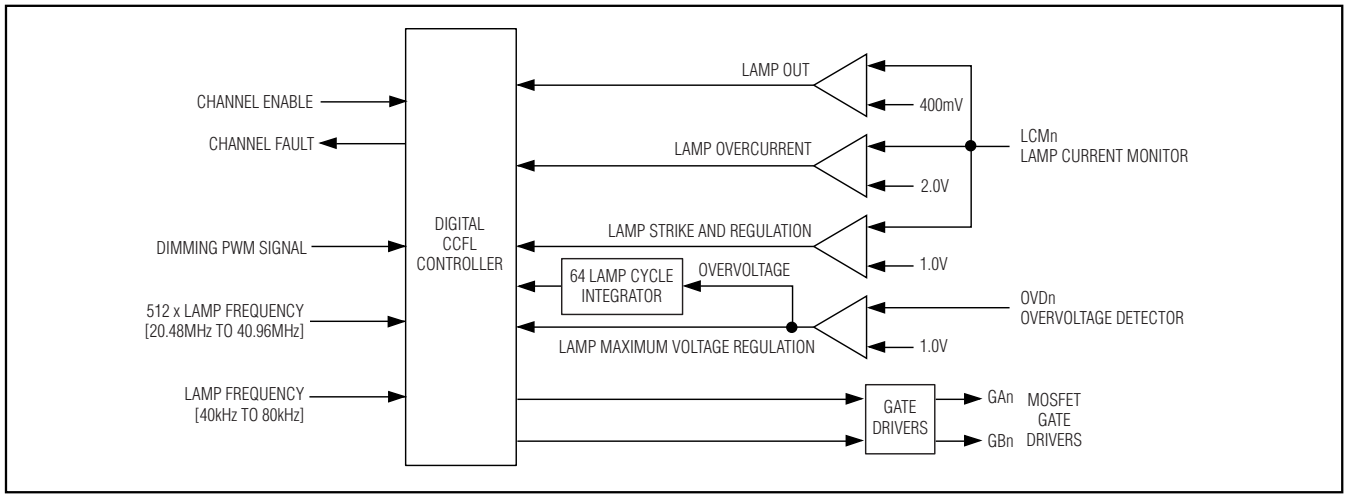


Figure 2. DS3992 Per Channel Logic Diagram

Detailed Description

Each DS3992 channel drives two logic-level n-channel MOSFETs that are connected between the ends of a step-up transformer and ground (See the *Typical Operating Circuits*). The transformer has a center tap on the primary side that is connected to the DC inverter voltage supply. The DS3992 alternately turns on the two MOSFETs to create the high-voltage AC waveform on the secondary side. By varying the duration of the MOSFET turn-on times, the DS3992 is able to accurately control the CCFL current.

A resistor in series with the CCFL's ground connection enables current monitoring. The voltage across this resistor is fed to the lamp current monitor (LCM) input and compared to an internal reference voltage to determine the duty cycle for the MOSFET gates.

The DS3992 supports a 1 lamp per channel configuration with fully independent lamp control and minimal external components. The DS3992 is also capable of controlling more than 1 lamp per channel using a wired-OR feedback circuit. See the *Typical Operating Circuits* section for more information.

Block diagrams of the DS3992 are shown in Figures 1 and 2. More operating details of the DS3992 are discussed on the following pages of this data sheet.

Dimming Control

The DS3992 uses "burst" dimming to control the lamp brightness. An analog voltage applied at the BRIGHT input pin determines the duty cycle of a digital pulse-width-modulated (DPWM) signal (90Hz to 220Hz for DS3992Z-09P/DS3992Z-09N and 180Hz to 440Hz for DS3992Z-18P/DS3992Z-18N). During the high period of the DPWM cycle, the lamp is driven at the selected lamp frequency (40kHz to 80kHz) as shown in Figure 3. This part of the cycle is also called the "burst" period because of the lamp frequency burst that occurs

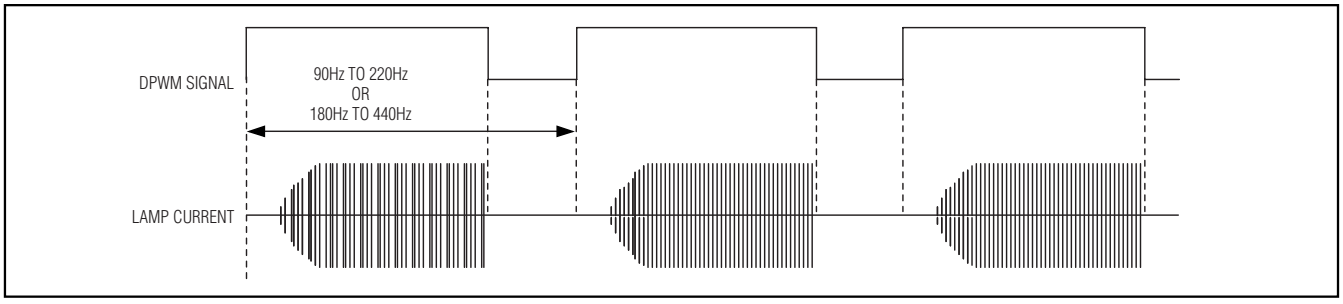


Figure 3. Digital-PWM Dimming and Soft-Start

Table 1. BRIGHT Analog Dimming Input Configuration

DEVICE	SLOPE	MINIMUM BRIGHTNESS	MAXIMUM BRIGHTNESS
DS3992Z-09P and DS3992Z-18P	Positive	BRIGHT < 0.5V	BRIGHT > 2.0V
DS3992Z-09N and DS3992Z-18N	Negative	BRIGHT > 2.0V	BRIGHT < 0.5V

during this time. During the low period of the DPWM cycle, the controller disables the MOSFET gate drivers so the lamp is not driven. This causes the current to stop flowing in the lamp, but the time is short enough to keep the lamp from de-ionizing. Dimming is increased/decreased by adjusting (i.e., modulating) the burst period duty cycle. At the beginning of each burst dimming cycle, there is a soft-start whereby the lamp current is slowly ramped to reduce the potential to create audible transformer noise.

The slope of the BRIGHT dimming input is either positive or negative as shown in Table 1. For voltages between 0.5V and 2.0V, the duty cycle will vary linearly between the minimum and 100%.

Lamp Strike

On lamp strike, the DS3992 boosts the normal operating lamp frequency by 33%. This is done to increase the voltage created and help insure that the lamp strikes. In addition, the maximum strike voltage will be applied to the lamp for over 500ms. Once the controller detects that the lamp has struck, the frequency is returned to the normal lamp frequency.

Setting the Lamp and DPWM Frequencies Using External Resistors

Both the lamp and DPWM frequencies are set using external resistors. The resistance required for either frequency can be determined using the following formula:

$$R_{OSC} = \frac{K}{f_{OSC}}$$

where K = 1600kΩ x kHz for lamp frequency calculations. When calculating the resistor value for the DPWM frequency, K will be one of two values depending on the DS3992 version. If using the -09N/P version (90Hz to 220Hz) then K = 4kΩ x kHz. K = 8kΩ x kHz for the -18N/P version (180Hz to 440Hz).

Example: Selecting the resistor values to configure the -09P version to have a 50kHz lamp frequency and a 160Hz DPWM frequency: For the DPWM resistor calculation, K = 4kΩ x kHz. For the lamp-frequency-resistor (R_{LOSC}) calculation, K = 1600kΩ x kHz, which is always the lamp frequency K value regardless of the frequency.

The previous formula can now be used to calculate the resistor values for R_{LOSC} and R_{POSC} as follows:

$$R_{LOSC} = \frac{1600k\Omega \times kHz}{50kHz} = 32k\Omega$$

$$R_{POSC} = \frac{4k\Omega \times kHz}{0.160kHz} = 25k\Omega$$

Supply Monitoring

The DS3992 has supply voltage monitors for both the inverter's DC supply (V_{INV}) and its own V_{CC} supply to ensure that both voltage levels are adequate for proper operation. The inverter supply is monitored for undervoltage conditions at the SVM pin. An external resistor-divider at the SVM input feeds into a comparator (see Figure 1) having a 2V threshold. Using the equation below to determine the resistor values, the inverter supply trip point (V_{TRIP}) can be customized to shut off the inverter when the inverter supply voltage drops below the specified value.

Operating with the inverter voltage at too high of a level can be damaging to the inverter components. Proper use of the SVM can prevent this problem. If desired, SVM can be disabled by connecting the SVM pin to GND.

$$V_{TRIP} = 2.0 \left(\frac{R_1 + R_2}{R_1} \right)$$

The V_{CC} monitor is a 5V supply undervoltage lockout (UVLO) that prevents operation when the DS3992 does not have adequate voltage for its analog circuitry to operate or to drive the external MOSFETs. The V_{CC} monitor features hysteresis to prevent V_{CC} noise from causing spurious operation when V_{CC} is near the trip point. This monitor cannot be disabled by any means.

Fault Monitoring

The DS3992 provides extensive fault monitoring for each channel. It can detect open-lamp, lamp overcurrent, failure to strike, and overvoltage conditions. Figure 4 shows a flowchart of how the DS3992 controls and monitors each channel. The steps are as follows:

The lamps will not turn on unless the DS3992 supply voltage is > 4.5V and the voltage at the supply voltage monitor (SVM) input is > 2V.

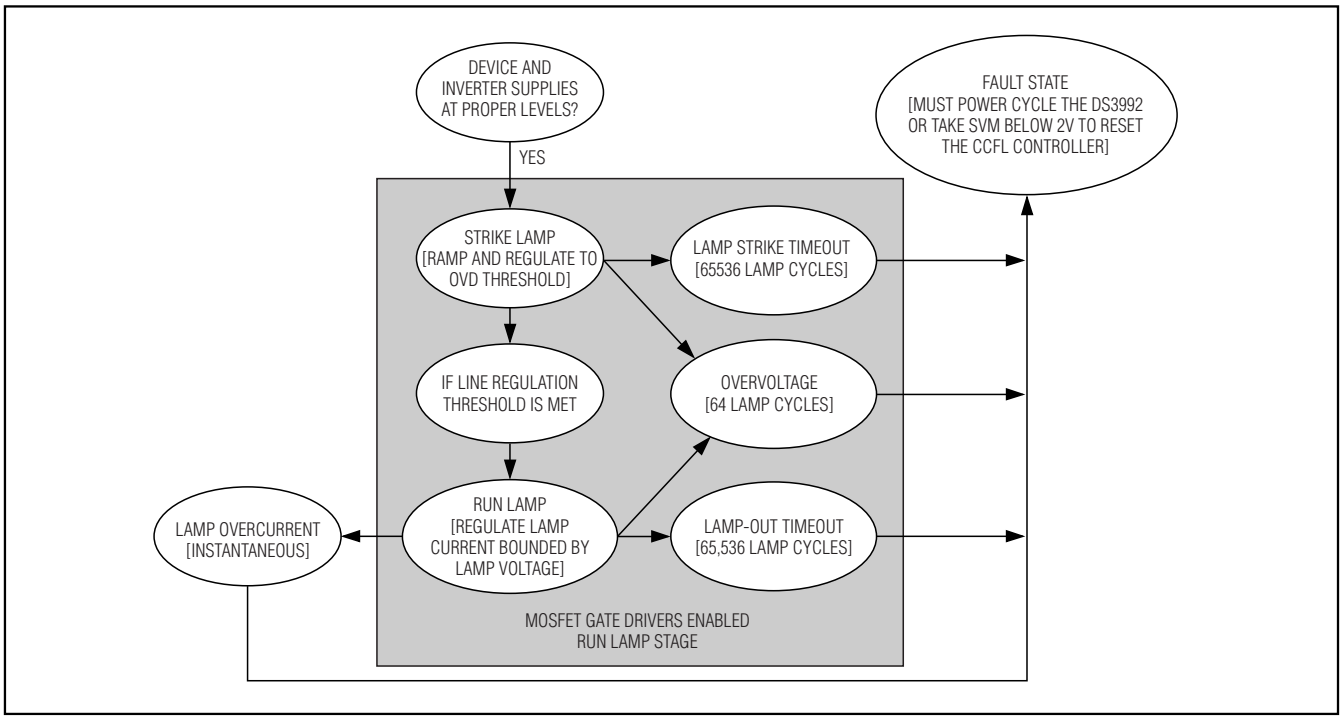


Figure 4. Fault-Handling Flowchart

When both the DS3992 and the DC inverter supplies are at acceptable levels, the DS3992 will attempt to strike the lamps. The DS3992 slowly ramps up the MOSFET gate duty cycle until the lamp strikes. The controller detects that the lamp has struck by detecting current flow in the lamp. If during the strike ramp, the maximum allowable voltage is reached, the controller will stop increasing the MOSFET gate duty cycle to keep from overstressing the system. The DS3992 will go into a fault-handling state if the lamp has not struck after 65,536 lamp cycles. If an overvoltage event is detected during the strike attempt, the DS3992 will disable the MOSFET gate drivers and go into the fault-handling state.

Once the lamp is struck, the DS3992 moves to the run lamp stage. In the run lamp stage, the DS3992 adjusts the MOSFET gate duty cycle to optimize the lamp current. The gate duty cycle is always constrained to keep the system from exceeding the maximum allowable lamp voltage. If lamp current ever drops below the lamp out reference point for 65536 lamp cycles, then the lamp is considered extinguished. In this case the MOSFET gate drivers are disabled and the device moves to the fault handling stage.

In the case of a lamp overcurrent condition, the DS3992 will instantaneously declare the controller to be in a fault state. If either channel on the DS3992 goes into the fault state, only the faulty channel will be shut down. Once a fault state is entered, the controller will remain in that state until one of the following occurs:

- V_{CC} drops below the UVLO threshold.
- The SVM input drops below 2.0V.

Applications Information

Component Selection

External component selection has a large impact on the overall system performance and cost. The two most important external components are the transformers and n-channel MOSFETs.

The transformer should be able to operate in the 40kHz to 80kHz frequency range of the DS3992, and the turns ratio should be selected so the MOSFET drivers run at 28% to 35% duty cycle during steady-state operation. The transformer must be able to withstand the high open-circuit voltage that will be used to strike the lamp. Additionally, its primary/secondary resistance and inductance characteristics must be considered because they contribute significantly to determining the

efficiency and transient response of the system. Table 2 shows a transformer specification that has been utilized for a 12V inverter supply, 438mm x 2.2mm lamp design.

The n-channel MOSFET must have a threshold voltage that is low enough to work with logic-level signals, a low on-resistance to maximize efficiency and limit the n-channel MOSFET's power dissipation, and a breakdown voltage high enough to handle the transient. The breakdown voltage should be a minimum of 3x the inverter voltage supply. Additionally, the total gate charge must be less than Q_G, which is specified in the *Recommended Operating Conditions* table. These specifications are easily met by many of the dual n-channel MOSFETs now available in SO-8 packages.

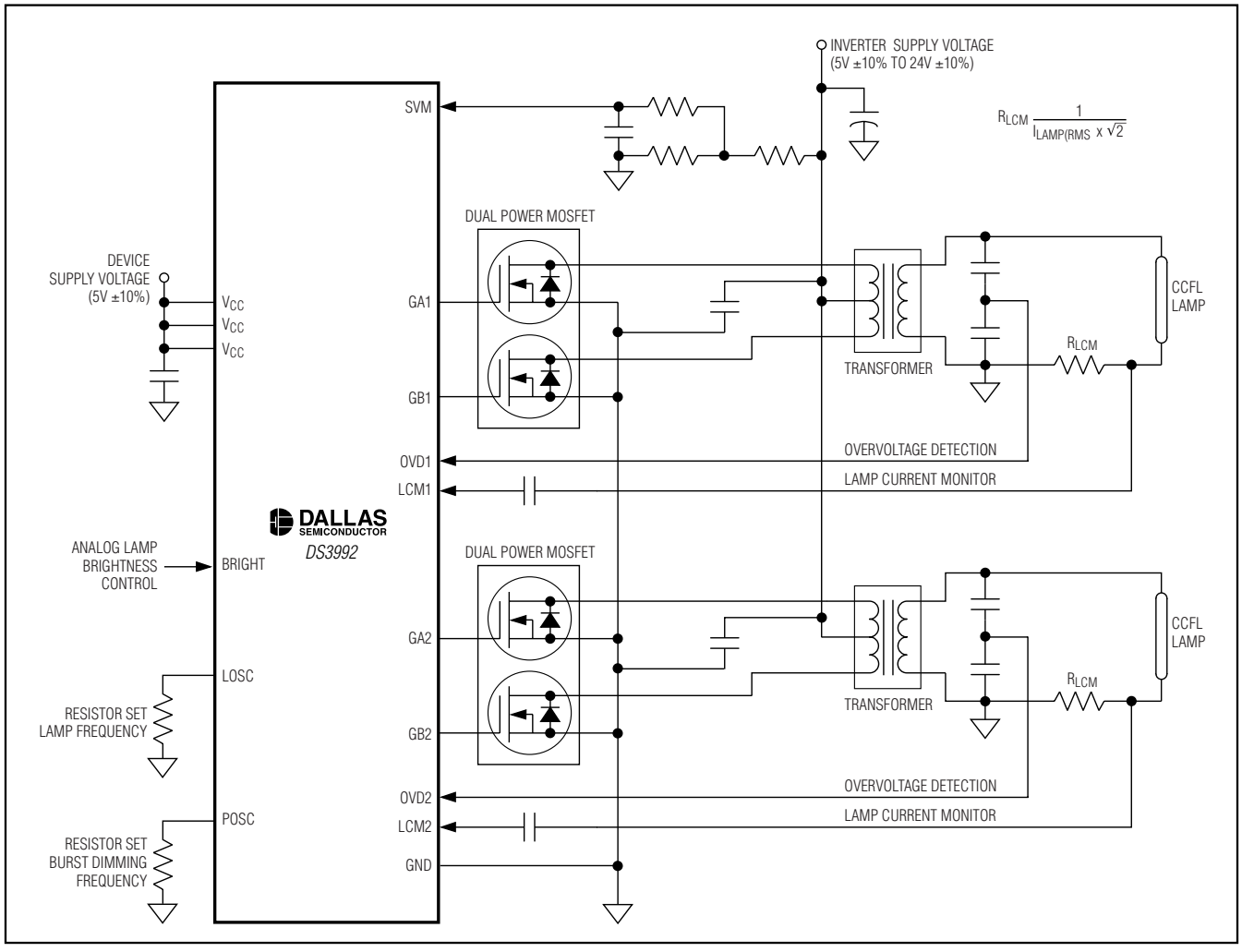
Table 2. Transformer Specifications (as Used in the *Typical Operating Circuit*)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Turns Ratio (Secondary/Primary)	(Notes 1, 2, 3)		40		
Frequency		40		80	kHz
Output Power				6	W
Output Current			5	8	mA
Primary DCR	Center tap to one end		200		mΩ
Secondary DCR			500		Ω
Primary Leakage			12		µH
Secondary Leakage			185		mH
Primary Inductance			70		µH
Secondary Inductance			500		mH
Secondary Output Voltage	1000ms minimum	2000			V_{RMS}
	Continuous	1000			

Note 1: Primary should be Bifilar wound with center tap connection.
Note 2: Turns ratio is defined as secondary winding divided by the sum of both primary windings.
Note 3: 40:1 is the nominal turns ratio for driving a 438mm x 2.2mm lamp with a 12V supply. Refer to AN3375 for more information.

Typical Operating Circuits

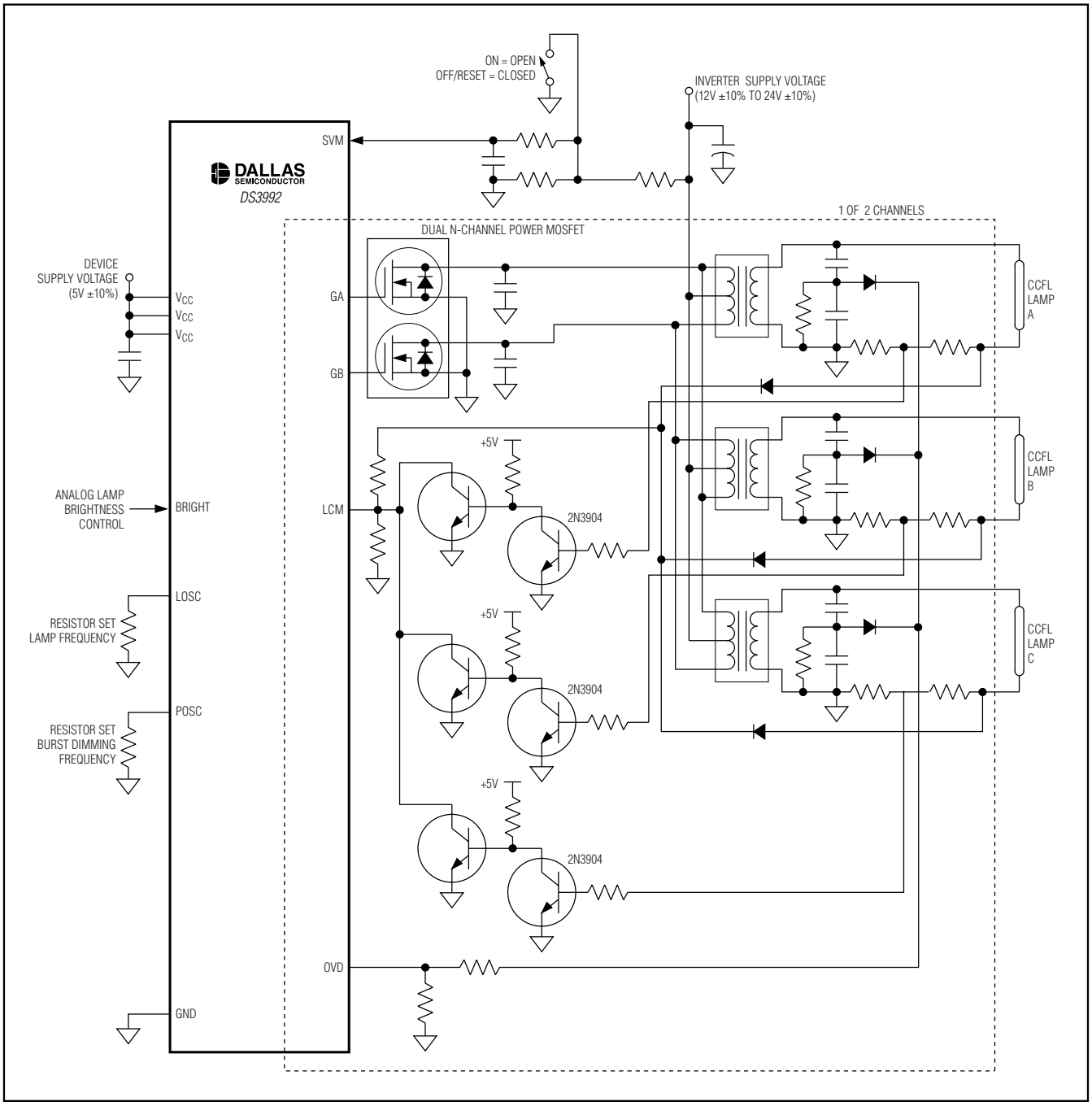
Single Per Channel Operating Circuit



Two-Channel, Push-Pull CCFL Controller

Typical Operating Circuits (continued)

Multi-Lamp Per Channel Operating Circuit



Power-Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor be used on pin 10, the IC power-supply pin. Pins 15 and 16, also V_{CC} pins, do require connection to supply voltage, but do not require any additional decoupling. Typical values of decoupling capacitors are 0.01µF or 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the IC to minimize lead inductance.

Chip Topology

TRANSISTOR COUNT: 53,000

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.