

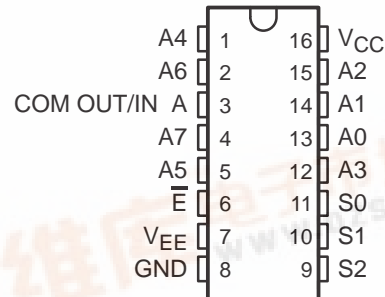
CD74HCT4051-Q1 HIGH-SPEED CMOS LOGIC ANALOG MULTIPLEXER/DEMULTIPLEXER

SCLS569A – JANUARY 2004 – FEBRUARY 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Wide Analog Input Voltage Range: ± 5 V Max
- Low ON Resistance
 - 70 Ω Typical ($V_{CC} - V_{EE} = 4.5$ V)
 - 40 Ω Typical ($V_{CC} - V_{EE} = 9$ V)
- Low Crosstalk Between Switches
- Fast Switching and Propagation Speeds
- Break-Before-Make Switching
- Wide Operating Temperature Range: -40°C to 125°C
- Operation Control Voltage: 4.5 V to 5.5 V
- Switch Voltage: 0 V to 10 V
- Direct LSTTL Input Logic Compatibility: $V_{IL} = 0.8$ V Max, $V_{IH} = 2$ V Min
- CMOS Input Compatibility: $I_I \leq 1$ μA at V_{OL} , V_{OH}

† Contact factory for details. Q100 qualification data available on request.

M PACKAGE
(TOP VIEW)



description/ordering information

This device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). It is a bidirectional switch that allows any analog input to be used as an output and vice-versa. The switch has low ON resistance and low OFF leakages. In addition, this device has an enable control that, when high, disables all switches to their OFF state.

ORDERING INFORMATION

T_A	PACKAGE‡	ORDERABLE PART NUMBER§	TOP-SIDE MARKING
-40°C to 125°C	SOIC – M Reel of 2500	CD74HCT4051QM96Q1	HCT4051Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

§ The suffix 96 denotes tape and reel.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

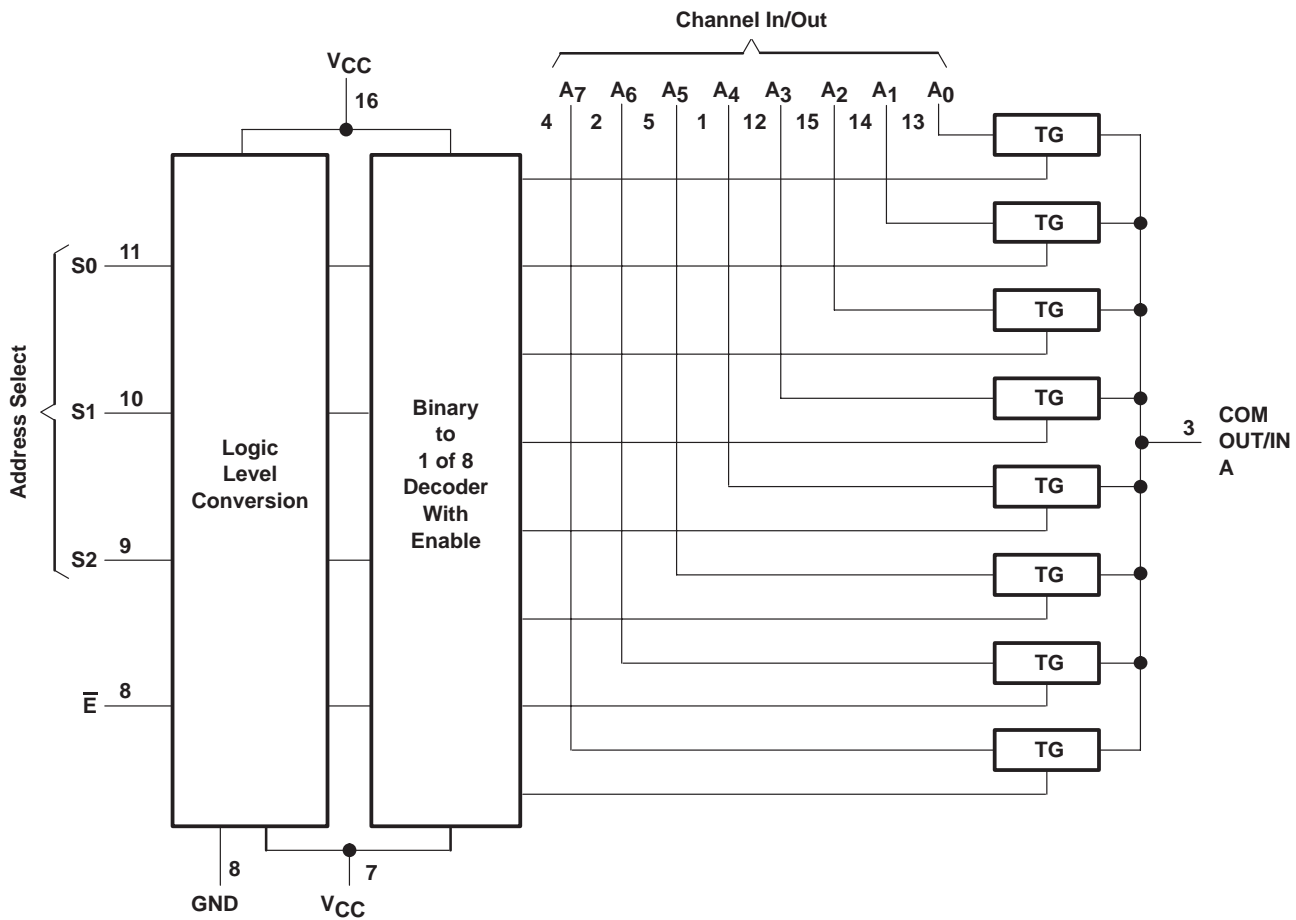
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FUNCTION TABLE

INPUTS				ON CHANNELS
ENABLE	S2	S1	S0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: $V_{CC} - V_{EE}$ (see Note 1)	-0.5 V to 10.5 V
V_{CC}	-0.5 V to +7 V
V_{EE}	0.5 V to -7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	± 20 mA
Output clamp current, I_{OK} ($V_O < V_{EE} - 0.5$ V or $V_O > V_{CC} + 0.5$ V)	± 20 mA
Switch current ($V_I > V_{EE} - 0.5$ V or $V_I < V_{CC} + 0.5$ V)	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
V_{EE} current, I_{EE}	-20 mA
Package thermal impedance, θ_{JA} (see Note 2)	73°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ($1,59 \pm 0,79$ mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
	Supply voltage, $V_{CC} - V_{EE}$ (see Figure 1)	2	10	V
V_{EE}	Supply voltage (see Note 4 and Figure 2)	0	-6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input control voltage	0	V_{CC}	V
V_{IS}	Analog switch I/O voltage	V_{EE}	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 4.5$ V		0 500 ns
T_A	Operating free-air temperature	-40	125	°C

- NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{ON} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

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recommended operating area as a function of supply voltages

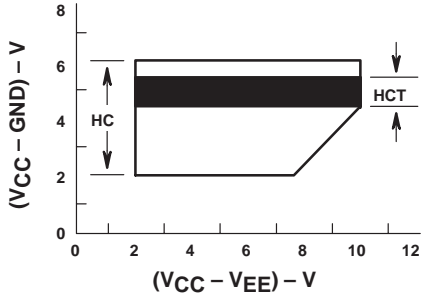


Figure 1

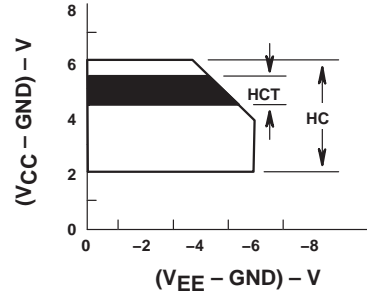


Figure 2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{EE}	V _{CC}	T _A = 25°C		T _A = -40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	
r _{on}	I _O = 1 mA, V _I = V _{IH} or V _{IL} , See Figure 9	V _{IS} = V _{CC} or V _{EE}	0 V	4.5 V	70	160	240	Ω
			-4.5 V	4.5 V	40	120	180	
		V _{IS} = V _{CC} to V _{EE}	0 V	4.5 V	90	180	270	
			-4.5 V	4.5 V	45	130	195	
Δr _{on}	Between any two channels	0 V	4.5 V	10			Ω	
		-4.5 V	4.5 V	5				
I _{Iz}	For switch OFF: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For switch ON: All applicable combinations of V _{IS} and V _{OS} voltage levels, V _I = V _{IH} or V _{IL}	0 V	6 V		±0.2	±2	μA	
		-5 V	5 V		±0.4	±4		
I _{IL}	V _I = V _{CC} or GND	Control input		5.5 V		±0.1	±1	μA
I _{CC}	I _O = 0, V _I = V _{CC} or GND	When V _{IS} = V _{EE} , V _{OS} = V _{CC}	0 V	5.5 V		8	160	μA
		When V _{IS} = V _{CC} , V _{OS} = V _{EE}	-4.5 V	5.5 V		16	320	
ΔI _{CC}	Per input pin: 1 unit load, See Note 5, V _{IN} = V _{CC} - 2.1 V		4.5 V to 5.5 V		100	360	490	μA

NOTE 5: For dual-supply systems, theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

TYPE	INPUT	UNIT LOADS [†]
4051	All	0.5

[†]Unit load is ΔI_{CC} limit specified in the electrical characteristics table, e.g., 360 μA max at 25°C.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{EE}	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t _{pd}	IN	OUT	C _L = 15 pF		5 V		4				ns
			C _L = 50 pF	0 V	4.5 V			12	18		
			C _L = 50 pF	-4.5 V	4.5 V			8	12		
t _{en}	S or \bar{E}	OUT	C _L = 15 pF		5 V		23				ns
			C _L = 50 pF	0 V	4.5 V			55	83		
			C _L = 50 pF	-4.5 V	4.5 V			39	59		
t _{dis}	S or \bar{E}	OUT	C _L = 15 pF		5 V		19				ns
			C _L = 50 pF	0 V	4.5 V			45	68		
			C _L = 50 pF	-4.5 V	4.5 V			32	48		
C _I	Control						10	10		pF	

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see Note 6)	52	pF

NOTE 6: C_{pd} is used to determine the dynamic power consumption (P_D), per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L + C_S) V_{CC}^2 \times f_O$$

f_O = output frequency

f_i = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

analog channel characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{EE}	V _{CC}	TYP	UNIT
C _I	Switch input capacitance			5	pF
C _{COM}	Common output capacitance			25	pF
f _{max}	Minimum switch frequency response at -3 dB	-2.25 V	2.25 V	145	MHz
		-4.5 V	4.5 V	180	
Sine-wave distortion	See Figure 5	-2.25 V	2.25 V	0.035	%
		-4.5 V	4.5 V	0.018	
\bar{E} or address select (S0, S1, S2) to switch feedthrough noise	See Figure 6 and Notes 8 and 9	-2.25 V	2.25 V	TBE	mV
		-4.5 V	4.5 V	TBE	
Switch OFF signal feedthrough	See Figure 7 and Figure 11 and Notes 8 and 9	-2.25 V	2.25 V	-73	dB
		-4.5 V	4.5 V	-75	

NOTES: 7. Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz.

8. V_{IS} is centered at (V_{CC} - V_{EE})/2.

9. Adjust input for 0 dBm.

PARAMETER MEASUREMENT INFORMATION

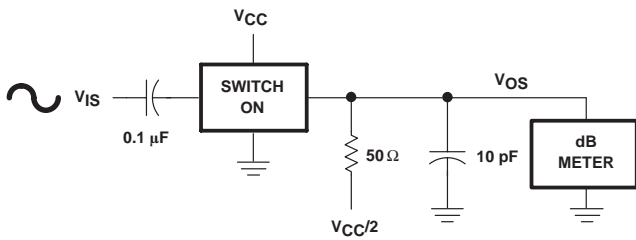
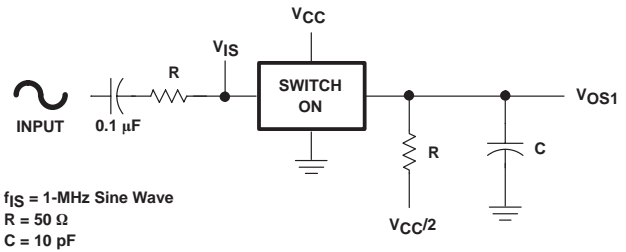


Figure 3. Frequency-Response Test Circuit

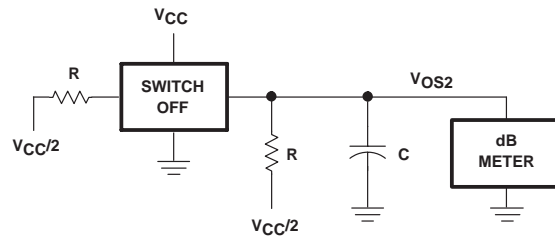


Figure 4. Crosstalk Between Two Switches Test Circuit

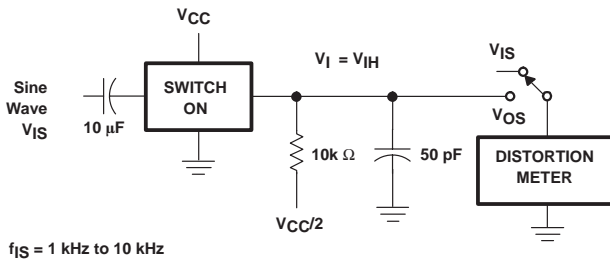


Figure 5. Sine-Wave Distortion Test Circuit

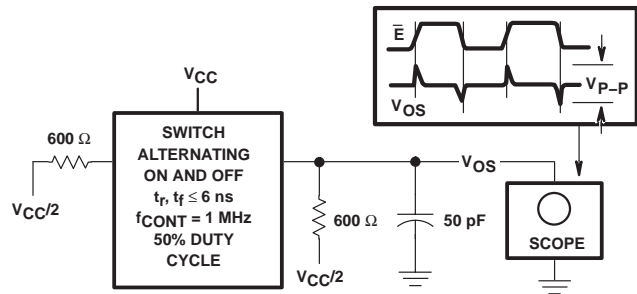


Figure 6. Control-to-Switch Feedthrough Noise Test Circuit

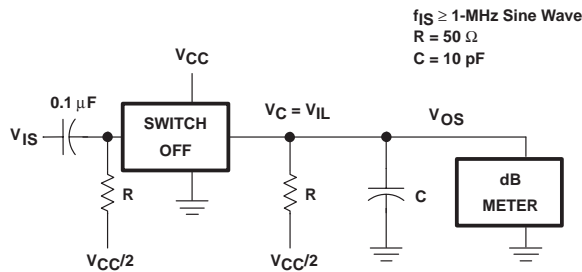
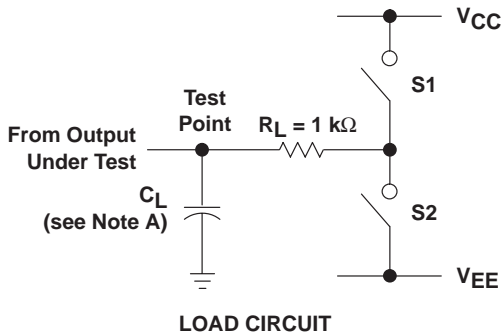
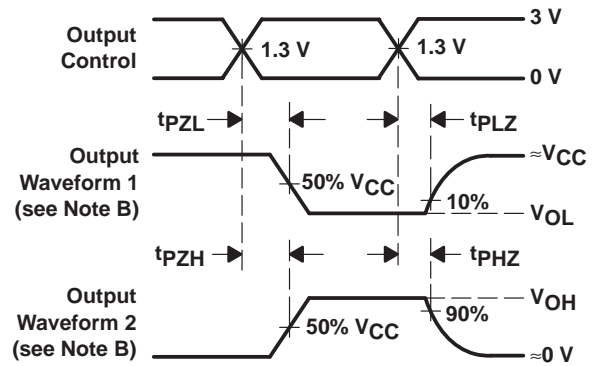
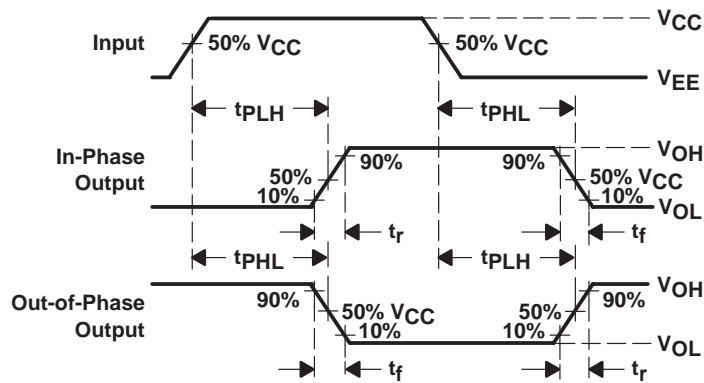


Figure 7. Switch OFF Signal Feedthrough Test Circuit

PARAMETER MEASUREMENT INFORMATION



PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 8. Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

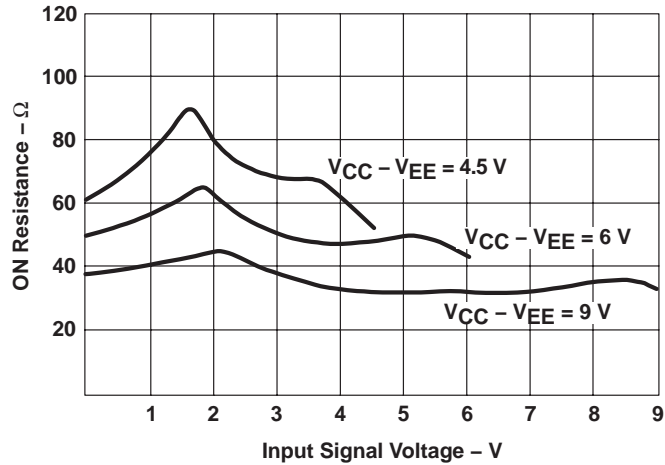


Figure 9. Typical ON Resistance vs Input Signal Voltage

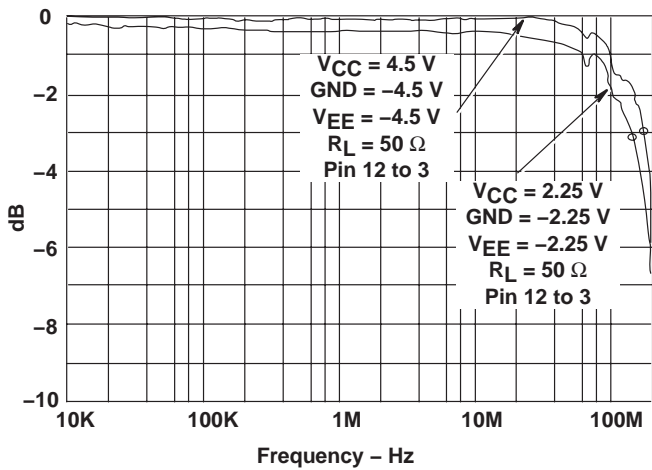


Figure 10. Channel ON Bandwidth

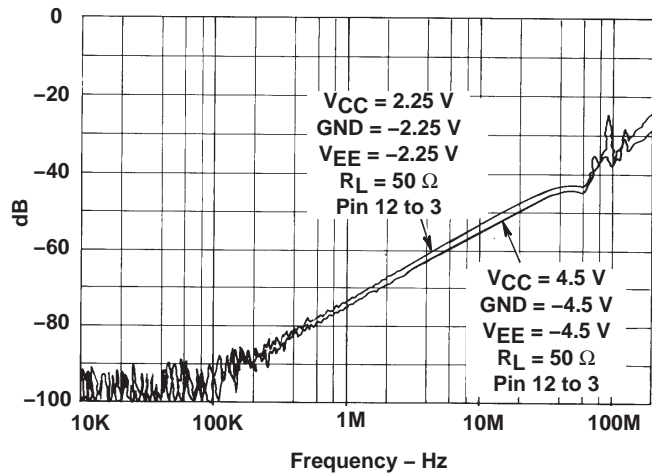


Figure 11. Channel OFF Feedthrough

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HCT4051QM96Q1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

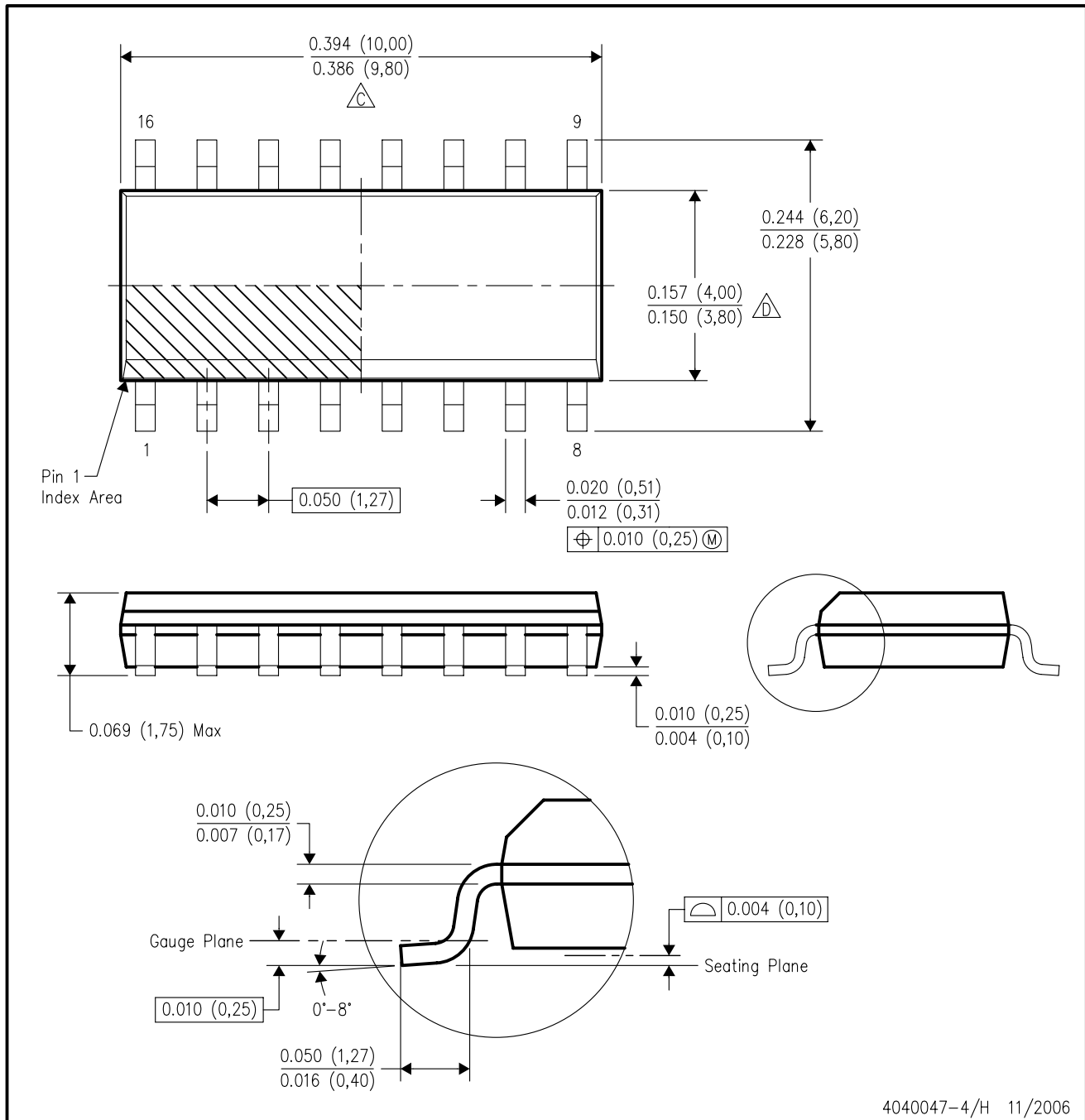
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MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

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