



**HIGH-SPEED 3.3V 16K x 36  
SYNCHRONOUS PIPELINED  
DUAL-PORT STATIC RAM  
WITH 3.3V OR 2.5V INTERFACE**

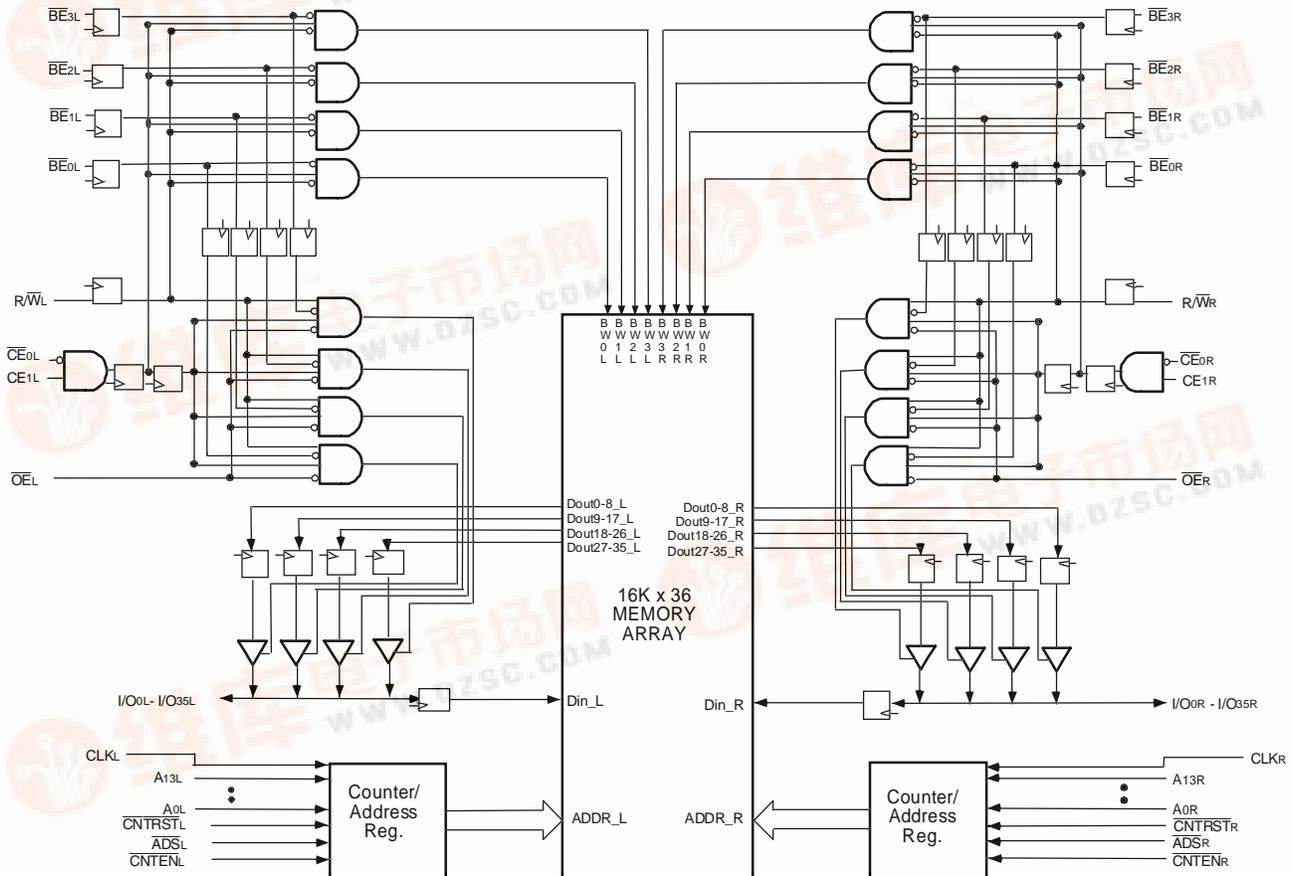
**IDT70V3569S**

**Features:**

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
  - Commercial: 4.2/5/6ns (max.)
  - Industrial: 5/6ns (max)
- ◆ Pipelined output mode
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
  - Fast 4.2ns clock to data out
  - 1.8ns setup to clock and 0.7ns hold on all control, data, and

- address inputs @ 133MHz
  - Data input, address, byte enable and control registers
  - Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 3.3V (±150mV) power supply for core
- ◆ LVTTTL-compatible, selectable 3.3V (±150mV)/2.5V (±125mV) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-ball fine-pitch Ball Grid Array, and 256-pin Ball Grid Array

**Functional Block Diagram**



4831 tbi 01



**Description:**

The IDT70V3569 is a high-speed 16K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3569 has been optimized for applications having unidirectional or bidirectional data flow

in bursts. An automatic power down feature, controlled by  $\overline{CE0}$  and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3569 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

**Pin Configuration<sup>(1,2,3,4)</sup>**

A1 IO19L	A2 IO18L	A3 VSS	A4 NC	A5 NC	A6 NC	A7 A12L	A8 A8L	A9 $\overline{BE1L}$	A10 VDD	A11 CLKL	A12 $\overline{CNTENL}$	A13 A4L	A14 A0L	A15 OPTL	A16 IO17L	A17 VSS	
B1 IO20R	B2 VSS	B3 IO18R	B4 VSS	B5 NC	B6 A13L	B7 A9L	B8 $\overline{BE2L}$	B9 $\overline{CE0L}$	B10 VSS	B11 $\overline{ADS}$	B12 A5L	B13 A1L	B14 VSS	B15 VDDQR	B16 IO16L	B17 IO15R	
C1 VDDQL	C2 IO19R	C3 VDDQR	C4 VDD	C5 NC	C6 NC	C7 A10L	C8 $\overline{BE3L}$	C9 CE1L	C10 VSS	C11 R/WL	C12 A6L	C13 A2L	C14 VDD	C15 IO16R	C16 IO15L	C17 VSS	
D1 IO22L	D2 VSS	D3 IO21L	D4 IO20L	D5 NC	D6 A11L	D7 A7L	D8 $\overline{BE0L}$	D9 VDD	D10 $\overline{OEL}$	D11 $\overline{CNTRSTL}$	D12 A3L	D13 VDD	D14 IO17R	D15 VDDQL	D16 IO14L	D17 IO14R	
E1 IO23L	E2 IO22R	E3 VDDQR	E4 IO21R	<p style="text-align: center;">70V3569BF BF-208<sup>(5)</sup></p> <p style="text-align: center;">208-Pin fpBGA Top View<sup>(6)</sup></p>										E14 IO12L	E15 IO13R	E16 VSS	E17 IO13L
F1 VDDQL	F2 IO23R	F3 IO24L	F4 VSS											F14 VSS	F15 IO12R	F16 IO11L	F17 VDDQR
G1 IO26L	G2 VSS	G3 IO25L	G4 IO24R											G14 IO9L	G15 VDDQL	G16 IO10L	G17 IO11R
H1 VDD	H2 IO26R	H3 VDDQR	H4 IO25R											H14 VDD	H15 IO9R	H16 VSS	H17 IO10R
J1 VDDQL	J2 VDD	J3 VSS	J4 VSS											J14 VSS	J15 VDD	J16 VSS	J17 VDDQR
K1 IO28R	K2 VSS	K3 IO27R	K4 VSS											K14 IO7R	K15 VDDQL	K16 IO8R	K17 VSS
L1 IO29R	L2 IO28L	L3 VDDQR	L4 IO27L											L14 IO6R	L15 IO7L	L16 VSS	L17 IO8L
M1 VDDQL	M2 IO29L	M3 IO30R	M4 VSS											M14 VSS	M15 IO6L	M16 IO5R	M17 VDDQR
N1 IO31L	N2 VSS	N3 IO31R	N4 IO30L											N14 IO3R	N15 VDDQL	N16 IO4R	N17 IO5L
P1 IO32R	P2 IO32L	P3 VDDQR	P4 IO35R											P5 NC	P6 NC	P7 A12R	P8 A8R
R1 VSS	R2 IO33L	R3 IO34R	R4 NC	R5 NC	R6 A13R	R7 A9R	R8 $\overline{BE2R}$	R9 $\overline{CE0R}$	R10 VSS	R11 $\overline{ADSR}$	R12 A5R	R13 A1R	R14 VSS	R15 VDDQL	R16 IO1R	R17 VDDQR	
T1 IO33R	T2 IO34L	T3 VDDQL	T4 VSS	T5 NC	T6 NC	T7 A10R	T8 $\overline{BE3R}$	T9 CE1R	T10 VSS	T11 R/WR	T12 A6R	T13 A2R	T14 VSS	T15 IO0R	T16 VSS	T17 IO2R	
U1 VSS	U2 IO35L	U3 VDD	U4 NC	U5 NC	U6 A11R	U7 A7R	U8 $\overline{BE0R}$	U9 VDD	U10 $\overline{OER}$	U11 $\overline{CNTRSTR}$	U12 A3R	U13 A0R	U14 VDD	U15 OPTR	U16 IO0L	U17 IO1L	

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**NOTES:**

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

**Pin Configuration<sup>(1,2,3,4)</sup> (con't.)**70V3569BC  
BC-256<sup>(5)</sup>256-Pin BGA  
Top View<sup>(6)</sup>

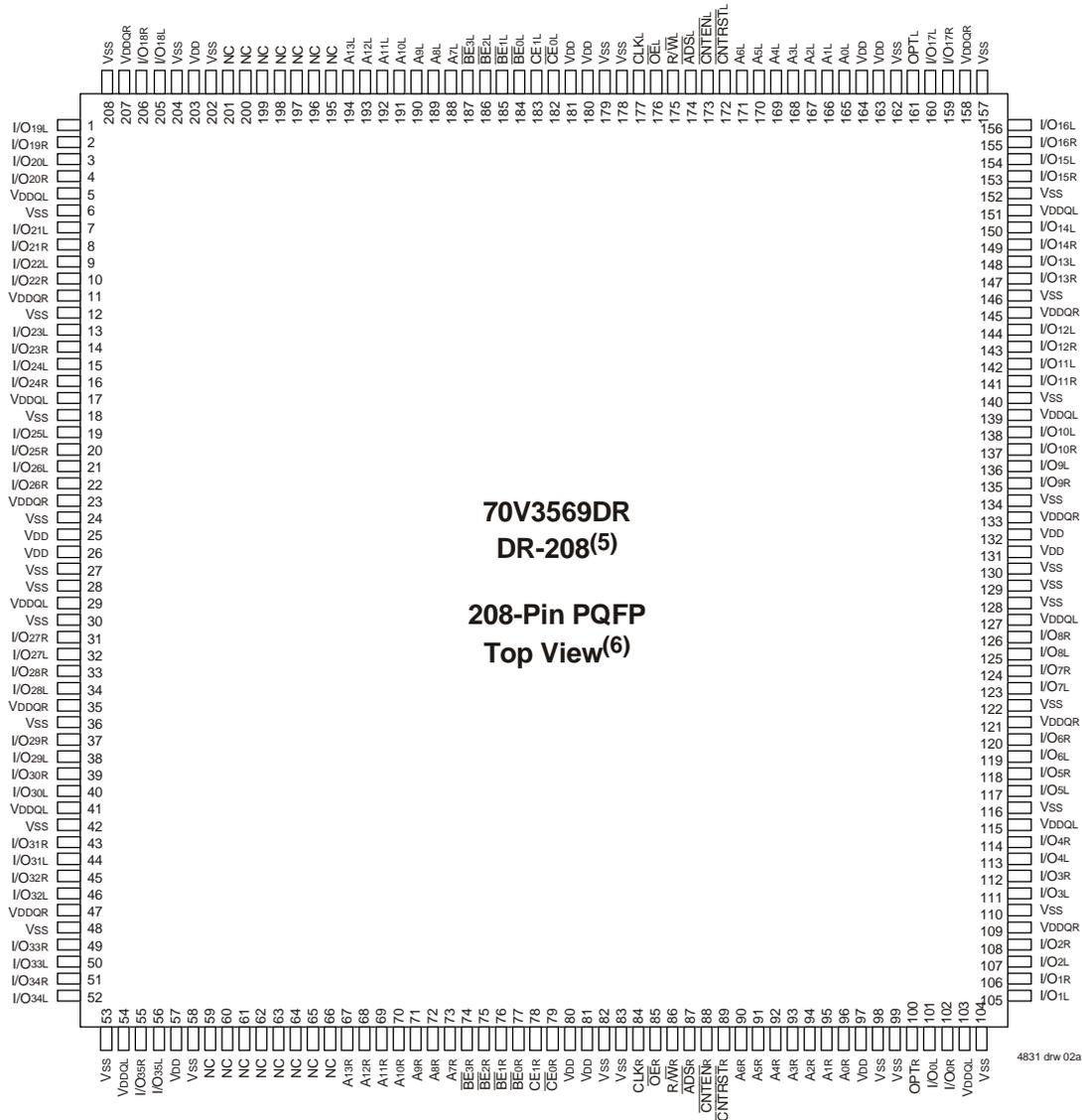
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	NC	NC	NC	NC	A11L	A8L	$\overline{BE}_{2L}$	CE1L	$\overline{OE}_{L}$	$\overline{CNTEN}_{L}$	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
I/O18L	NC	NC	NC	NC	A12L	A9L	$\overline{BE}_{3L}$	$\overline{CE}_{0L}$	R/WL	$\overline{CNTRST}_{L}$	A4L	A1L	VDD	I/O17L	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
I/O18R	I/O19L	VSS	NC	A13L	A10L	A7L	$\overline{BE}_{1L}$	$\overline{BE}_{0L}$	CLKL	$\overline{ADSL}_{L}$	A6L	A3L	OPTL	I/O17R	I/O16L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
I/O20R	I/O19R	I/O20L	VDD	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	I/O15R	I/O15L	I/O16R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O21R	I/O21L	I/O22L	VDDQL	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQR	I/O13L	I/O14L	I/O14R
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O23L	I/O22R	I/O23R	VDDQL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O12R	I/O13R	I/O12L
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
I/O24R	I/O24L	I/O25L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O10L	I/O11L	I/O11R
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
I/O26L	I/O25R	I/O26R	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O9R	I/O9L	I/O10R
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O27L	I/O28R	I/O27R	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O8R	I/O7R	I/O8L
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
I/O29R	I/O29L	I/O28L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O6R	I/O6L	I/O7L
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O30L	I/O31R	I/O30R	VDDQR	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O5L	I/O4R	I/O5R
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O32R	I/O32L	I/O31L	VDDQR	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O3R	I/O3L	I/O4L
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
I/O33L	I/O34R	I/O33R	VDD	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	I/O2L	I/O1R	I/O2R
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
I/O35R	I/O34L	NC	NC	A13R	A10R	A7R	$\overline{BE}_{1R}$	$\overline{BE}_{0R}$	CLKR	$\overline{ADSR}_{R}$	A6R	A3R	I/O0L	I/O0R	I/O1L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
I/O35L	NC	NC	NC	NC	A12R	A9R	$\overline{BE}_{3R}$	$\overline{CE}_{0R}$	R/WR	$\overline{CNTRST}_{R}$	A4R	A1R	OPTR	NC	NC
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	NC	NC	NC	NC	A11R	A8R	$\overline{BE}_{2R}$	CE1R	$\overline{OE}_{R}$	$\overline{CNTEN}_{R}$	A5R	A2R	A0R	NC	NC

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**NOTES:**

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration<sup>(1,2,3,4)</sup> (con't.)



NOTES:

1. All V<sub>DD</sub> pins must be connected to 3.3V power supply.
2. All V<sub>DDQ</sub> pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V<sub>IH</sub> (3.3V), and 2.5V if OPT pin for that port is set to V<sub>IL</sub> (0V).
3. All V<sub>SS</sub> pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$ , $CE_{1L}$	$\overline{CE}_{0R}$ , $CE_{1R}$	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}$ - $A_{13L}$	$A_{0R}$ - $A_{13R}$	Address
$I/O_{0L}$ - $I/O_{35L}$	$I/O_{0R}$ - $I/O_{35R}$	Data Input/Output
$CLK_L$	$CLK_R$	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes)
$V_{DDQL}$	$V_{DDQR}$	Power (I/O Bus) (3.3V or 2.5V) <sup>(1)</sup>
$OPT_L$	$OPT_R$	Option for selection $V_{DDOX}^{(1,2)}$
$V_{DD}$		Power (3.3V) <sup>(1)</sup>
$V_{SS}$		Ground (0V)

4831 tbl 01

### NOTES:

- $V_{DD}$ ,  $OPT_x$ , and  $V_{DDOX}$  must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- $OPT_x$  selects the operating voltage levels for the I/Os and controls on that port. If  $OPT_x$  is set to  $V_{IH}$  (3.3V), then that port's I/Os and controls will operate at 3.3V levels and  $V_{DDOX}$  must be supplied at 3.3V. If  $OPT_x$  is set to  $V_{IL}$  (0V), then that port's I/Os and controls will operate at 2.5V levels and  $V_{DDOX}$  must be supplied at 2.5V. The  $OPT$  pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

## Truth Table I—Read/Write and Enable Control<sup>(1,2,3,4)</sup>

$\overline{OE}$	CLK	$\overline{CE}_0$	$CE_1$	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	$R/\overline{W}$	Byte 3 I/O <sub>27-35</sub>	Byte 2 I/O <sub>18-26</sub>	Byte 1 I/O <sub>9-17</sub>	Byte 0 I/O <sub>0-8</sub>	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	High-Z	D <sub>IN</sub>	Write to Byte 0 Only
X	↑	L	H	H	L	H	H	L	High-Z	High-Z	D <sub>IN</sub>	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	D <sub>IN</sub>	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	D <sub>IN</sub>	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	D <sub>IN</sub>	D <sub>IN</sub>	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	D <sub>IN</sub>	D <sub>IN</sub>	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D <sub>OUT</sub>	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	D <sub>OUT</sub>	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	D <sub>OUT</sub>	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	D <sub>OUT</sub>	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	D <sub>OUT</sub>	D <sub>OUT</sub>	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	D <sub>OUT</sub>	D <sub>OUT</sub>	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	Read All Bytes
H	↑	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

### NOTES:

- "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care.
- $\overline{ADS}$ ,  $\overline{CNTEN}$ ,  $\overline{CNTRST}$  =  $V_{IH}$ .
- OE is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

4831 tbl 02

**Truth Table II—Address Counter Control<sup>(1,2)</sup>**

Address	Previous Address	Addr Used	CLK <sup>(6)</sup>	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNRST}$	I/O <sup>(3)</sup>	MODE
X	X	0	↑	X	X	L <sup>(4)</sup>	Dvo(0)	Counter Reset to Address 0
An	X	An	↑	L <sup>(4)</sup>	X	H	Dvo (n)	External Address Used
An	Ap	Ap	↑	H	H	H	Dvo(p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L <sup>(5)</sup>	H	Dvo(p+1)	Counter Enabled—Internal Address generation

4831 tbl 03

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R $\overline{W}$ ,  $\overline{CE_0}$ , CE<sub>1</sub>,  $\overline{BEn}$  and  $\overline{OE}$ .
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- $\overline{ADS}$  and  $\overline{CNRST}$  are independent of all other memory control signals including  $\overline{CE_0}$ , CE<sub>1</sub> and  $\overline{BEn}$ .
- The address counter advances if  $\overline{CNTEN} = V_{IL}$  on the rising edge of CLK, regardless of all other memory control signals including  $\overline{CE_0}$ , CE<sub>1</sub>,  $\overline{BEn}$ .

**Recommended Operating Temperature and Supply Voltage<sup>(1,2)</sup>**

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4831 tbl 04

**NOTES:**

- Industrial temperature: for specific speeds, packages and powers contact your sales office.
- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

**Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

4831 tbl 06

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>DD</sub> + 150mV.

**Recommended DC Operating Conditions with V<sub>DDQ</sub> at 2.5V**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	2.375	2.5	2.625	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage <sup>(3)</sup> (Address & Control Inputs)	1.7	—	V <sub>DDQ</sub> + 125mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	1.7	—	V <sub>DDQ</sub> + 125mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

4831 tbl 05a

**NOTES:**

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10 ns.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IL</sub> (0V), and V<sub>DDQx</sub> for that port must be supplied as indicated above.

**Recommended DC Operating Conditions with V<sub>DDQ</sub> at 3.3V**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	3.15	3.3	3.45	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage (Address & Control Inputs) <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

4831 tbl 05b

**NOTES:**

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10 ns.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IH</sub> (3.3V), and V<sub>DDQx</sub> for that port must be supplied as indicated above.

**Capacitance<sup>(1)</sup>****(TA = +25°C, F = 1.0MHz) PQFP ONLY**

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>OUT<sup>(3)</sup></sub>	Output Capacitance	V <sub>OUT</sub> = 3dV	10.5	pF

4831 tbl 07

**NOTES:**

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C<sub>OUT</sub> also references C<sub>I/O</sub>.

**DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V ± 150mV)**

Symbol	Parameter	Test Conditions	70V3569S		Unit
			Min.	Max.	
I <sub>L</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DDQ</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}_D = V_{IH}$ or CE <sub>1</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
V <sub>OL</sub> (3.3V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +4mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (3.3V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -4mA, V <sub>DDQ</sub> = Min.	2.4	—	V
V <sub>OL</sub> (2.5V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +2mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (2.5V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -2mA, V <sub>DDQ</sub> = Min.	2.0	—	V

4831 tbl 08

**NOTE:**

- At V<sub>DD</sub> ≤ -2.0V input leakages are undefined.
- V<sub>DDQ</sub> is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(3)</sup> ( $V_{DD} = 3.3V \pm 150mV$ )

Symbol	Parameter	Test Condition	Version	70V3569S4 Com'l Only		70V3569S5 Com'l & Ind		70V3569S6 Com'l & Ind		Unit	
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	375	460	285	360	245	310	mA
			IND	S	—	—	285	415	245	360	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	145	190	105	145	95	125	mA
			IND	S	—	—	105	175	95	150	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	265	325	190	260	175	225	mA
			IND	S	—	—	190	300	175	260	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L	S	6	15	6	15	6	15	mA
			IND	S	—	—	6	30	6	30	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A \leq 0.2V$ and $\overline{CE}^B \geq V_{DD} - 0.2V^{(5)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	265	325	180	260	170	225	mA
			IND	S	—	—	180	300	170	260	

4831 tbl 09

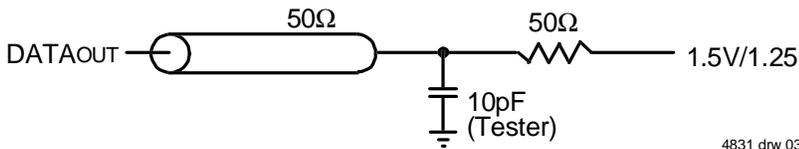
**NOTES:**

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cyc}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  for Typ, and are not production tested.  $I_{DD} dc(f=0) = 120mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{CC} - 0.2V$   
 $\overline{CE}_X \geq V_{CC} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{CC} - 0.2V$  or  $CE_{1X} \leq 0.2V$   
"X" represents "L" for left port or "R" for right port.

**AC Test Conditions**

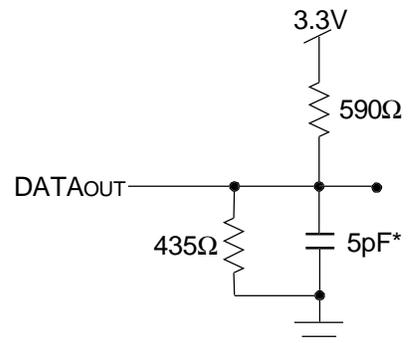
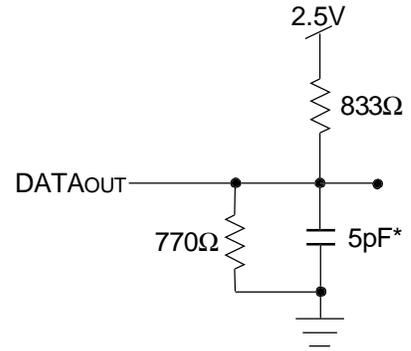
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4831 tbl 10



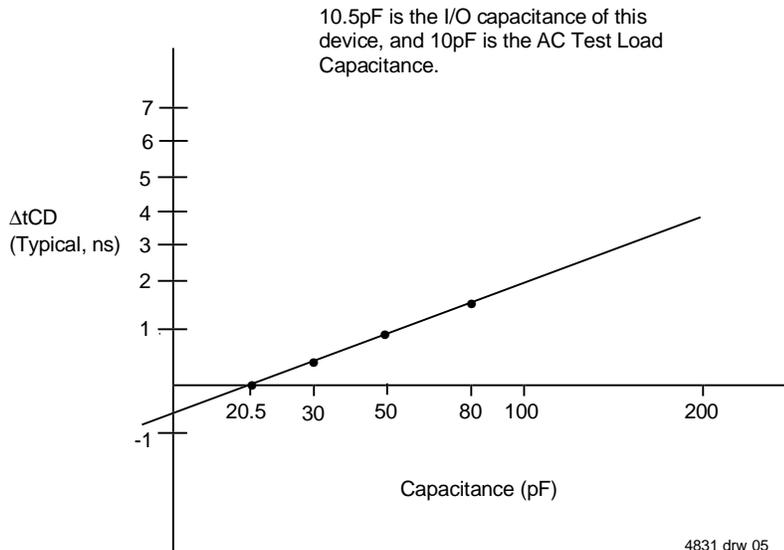
4831 drw 03

Figure 1. AC Output Test load.



4831 drw 04

Figure 2. Output Test Load  
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).  
\*Including scope and jig.



4831 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(1,2)</sup>

(V<sub>DD</sub> = 3.3V ± 150mV, T<sub>A</sub> = 0°C to +70°C)

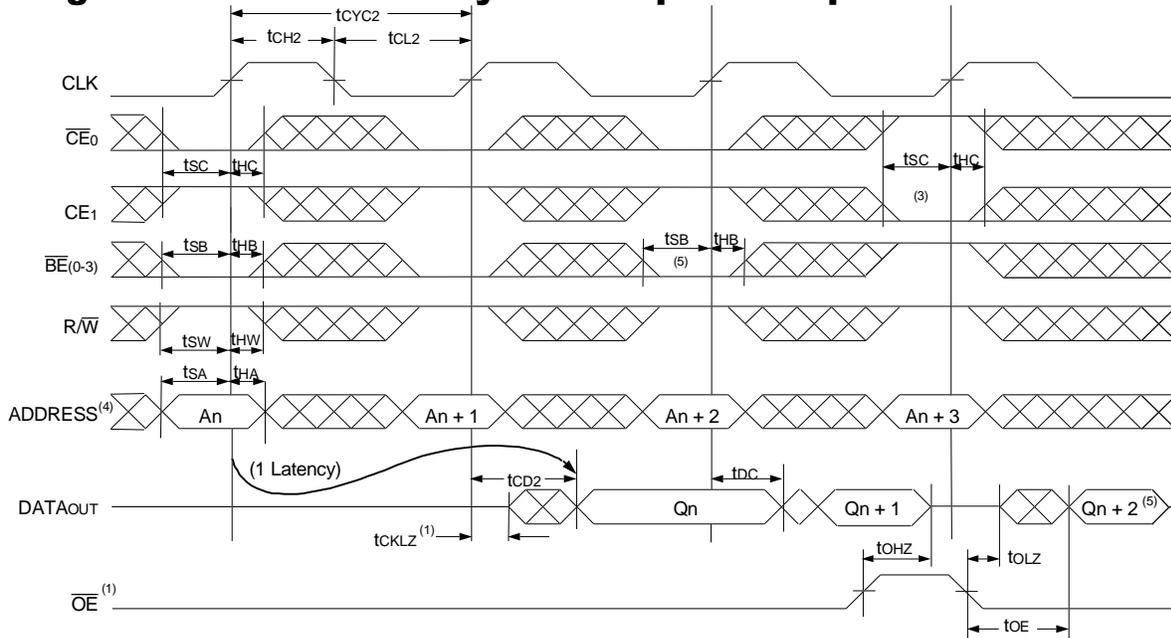
Symbol	Parameter	70V3569S4 Com'l Only		70V3569S5 Com'l & Ind		70V3569S6 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC2</sub>	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t <sub>CH2</sub>	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t <sub>CL2</sub>	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t <sub>R</sub>	Clock Rise Time	—	3	—	3	—	3	ns
t <sub>F</sub>	Clock Fall Time	—	3	—	3	—	3	ns
t <sub>SA</sub>	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HA</sub>	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SC</sub>	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HC</sub>	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SB</sub>	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HB</sub>	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SW</sub>	R/ $\bar{W}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HW</sub>	R/ $\bar{W}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SD</sub>	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HD</sub>	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SAD</sub>	$\bar{ADS}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HAD</sub>	$\bar{ADS}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SCN</sub>	$\bar{CNTEN}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HCN</sub>	$\bar{CNTEN}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>SRST</sub>	$\bar{CNTRST}$ Setup Time	1.8	—	2.0	—	2.0	—	ns
t <sub>HRST</sub>	$\bar{CNTRST}$ Hold Time	0.7	—	0.7	—	1.0	—	ns
t <sub>OE</sub> <sup>(1)</sup>	Output Enable to Data Valid	—	4	—	5	—	6	ns
t <sub>OLZ</sub>	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t <sub>OHZ</sub>	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t <sub>CD2</sub>	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t <sub>DC</sub>	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t <sub>CKHZ</sub>	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t <sub>CKLZ</sub>	Clock High to Output Low-Z	1	—	1	—	1	—	ns
<b>Port-to-Port Delay</b>								
t <sub>CO</sub>	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4831 tbl 11

### NOTES:

- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\bar{OE}$ ).
- These values are valid for either level of V<sub>DD</sub> (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

### Timing Waveform of Read Cycle for Pipelined Operation<sup>(2)</sup>

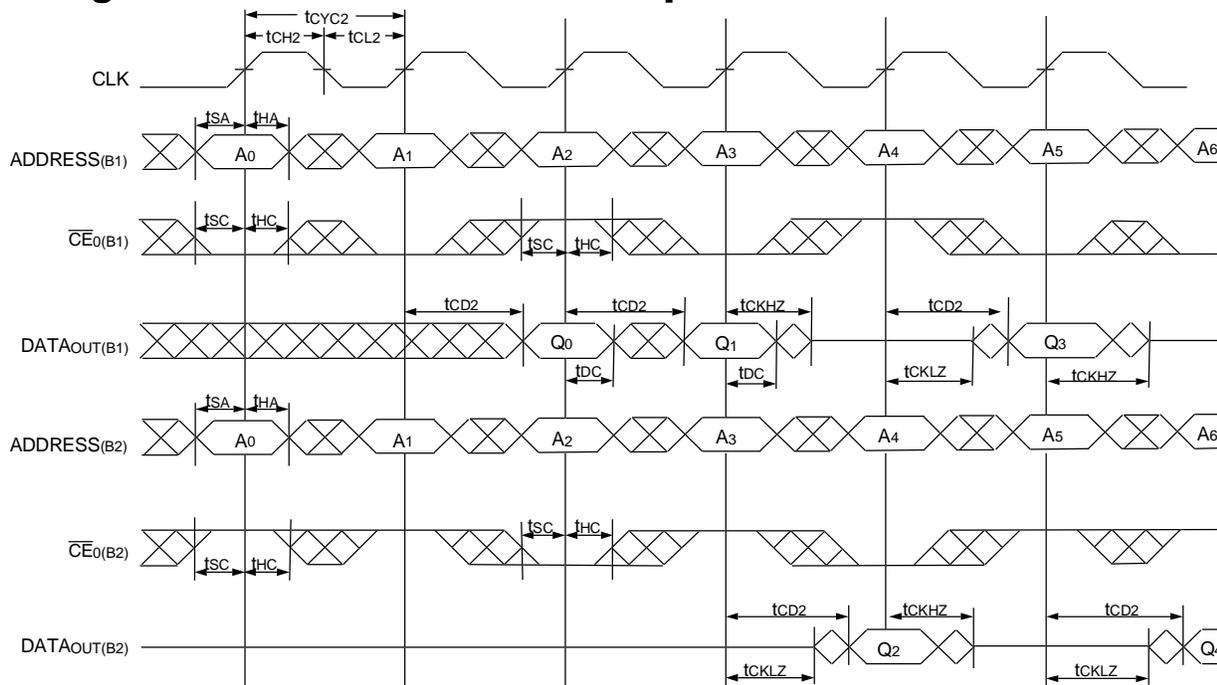


**NOTES:**

1.  $\overline{OE}$  is asynchronously controlled: all other inputs are synchronous to the rising clock edge.
2.  $\overline{ADS} = V_{IL}$ ,  $\overline{CNTEN}$  and  $\overline{CNTRST} = V_{IH}$ .
3. The output is disabled (High-Impedance state) by  $\overline{CE}_0 = V_{IH}$ ,  $CE_1 = V_{IL}$ ,  $\overline{BE}_n = V_{IH}$  following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If  $\overline{BE}_n$  was HIGH, then the appropriate Byte of DATAout for  $Q_{n+2}$  would be disabled (High-Impedance state).

4831 drw 06

### Timing Waveform of a Multi-Device Pipelined Read<sup>(1,2)</sup>

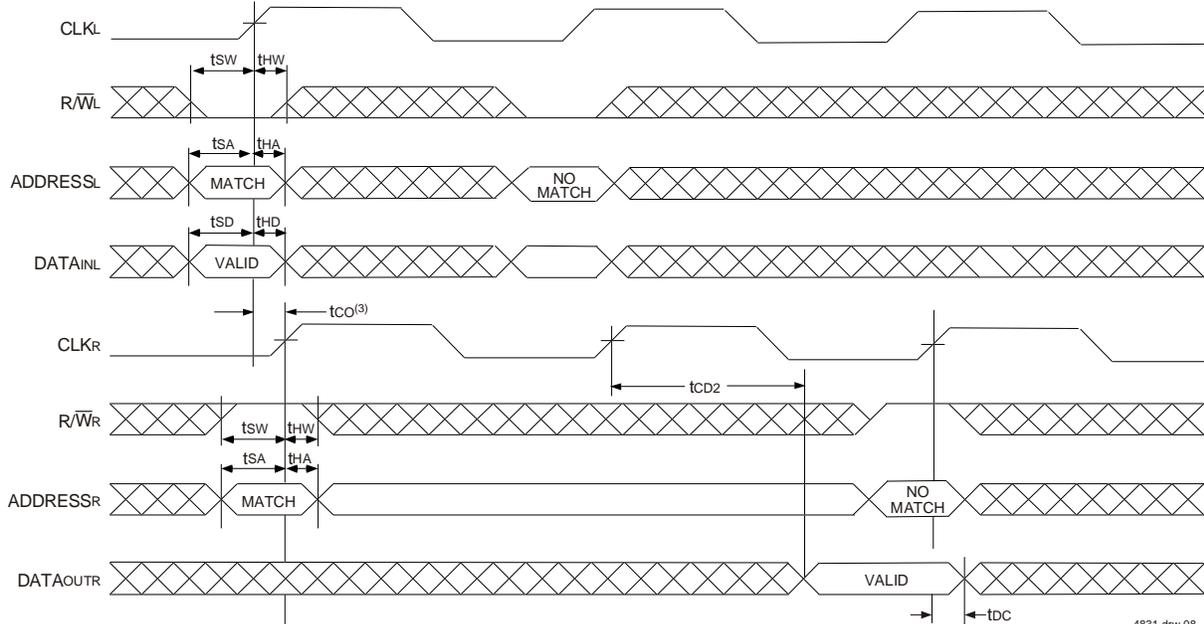


**NOTES:**

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3569 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2.  $\overline{BE}_n$ ,  $\overline{OE}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1(B1)$ ,  $CE_1(B2)$ ,  $R/\overline{W}$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .

4831 drw 07

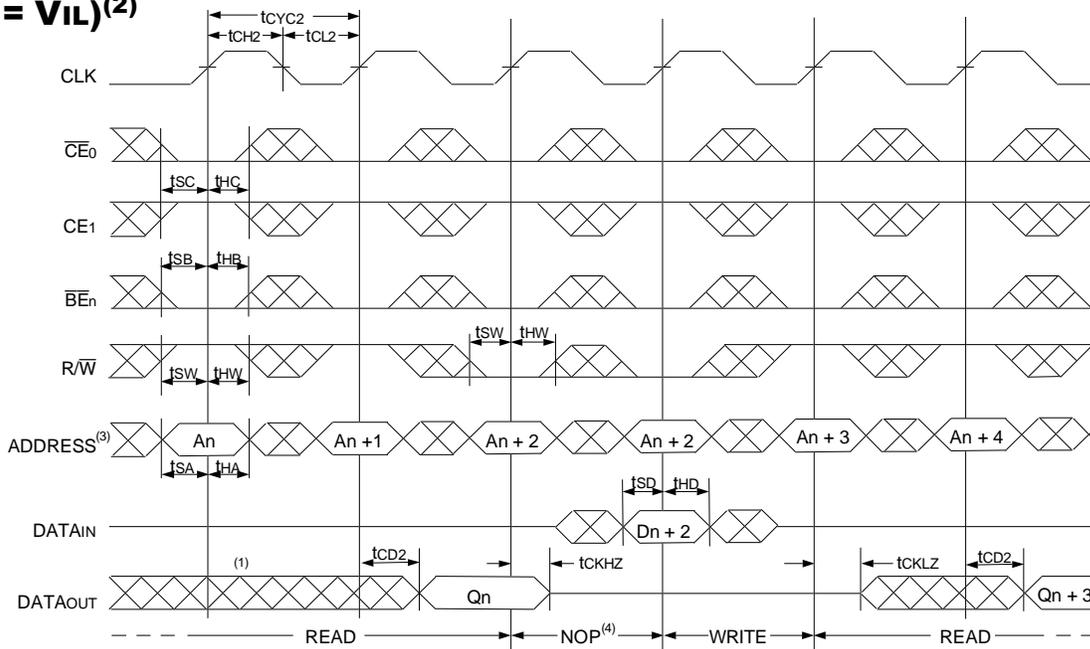
### Timing Waveform of Left Port Write to Pipelined Right Port Read<sup>(1,2)</sup>



**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNRST} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
3. If  $t_{CO} \leq$  minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + 2 t_{CYC2} + t_{CD2}$ ). If  $t_{CO} >$  minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + t_{CYC} + t_{CD2}$ ).

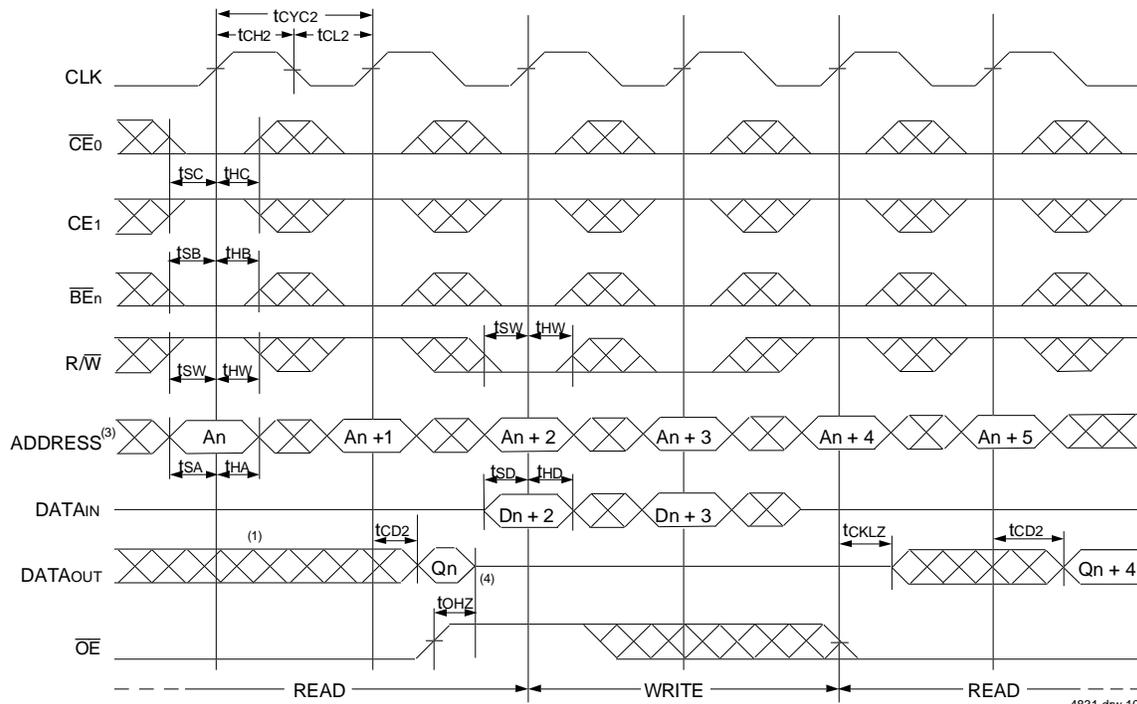
### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>



**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNRST} = V_{IH}$ . "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

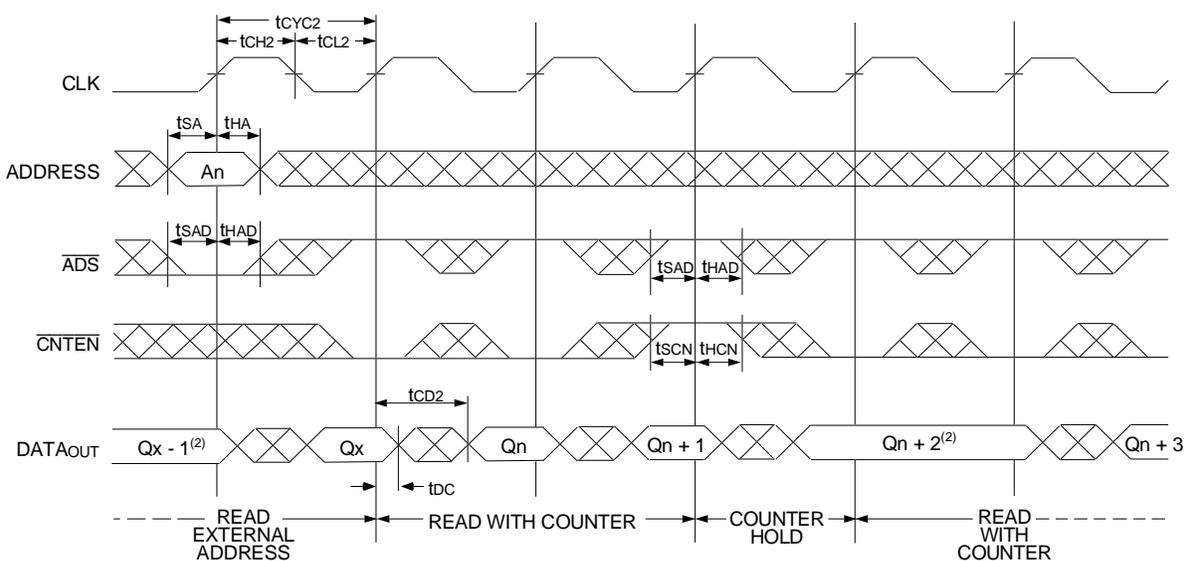
## Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(2)</sup>



### NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNRST} = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

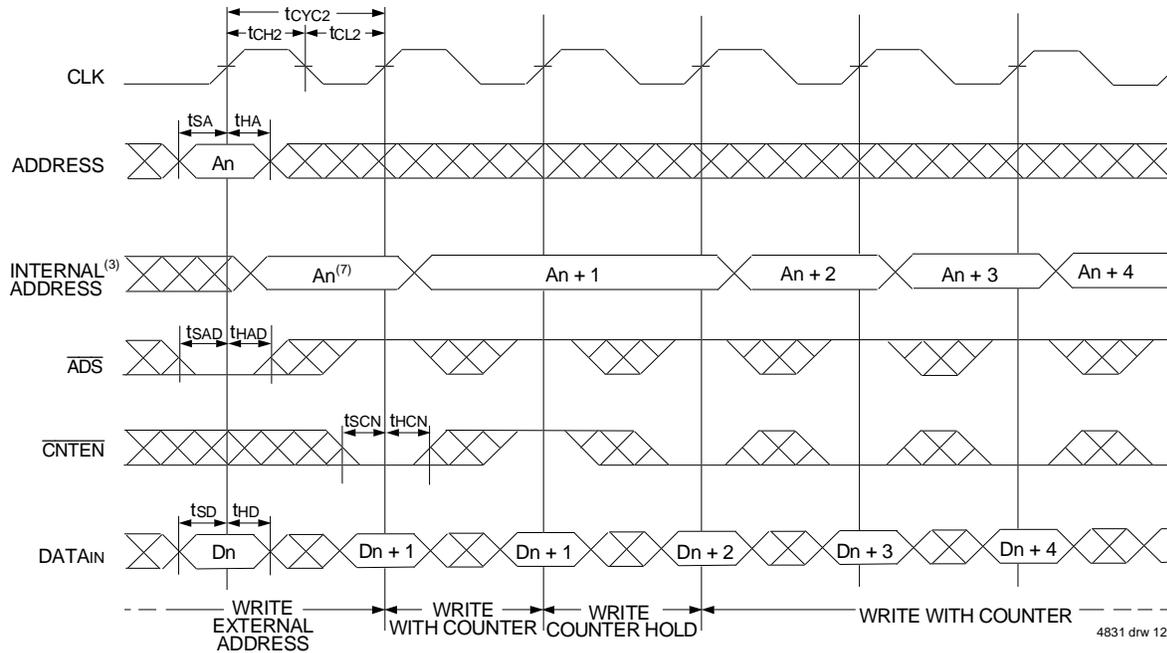
## Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



### NOTES:

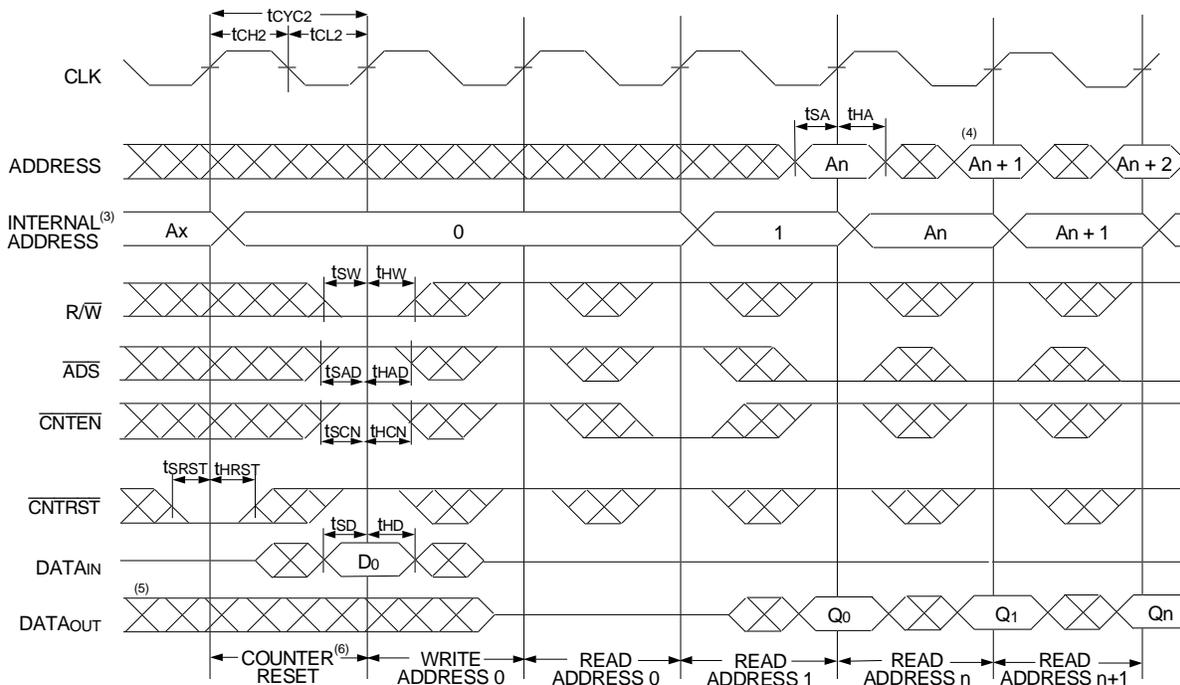
1.  $\overline{CE}_0$ ,  $\overline{OE}$ ,  $\overline{BE}_n = V_{IL}$ ;  $CE_1$ ,  $R/\overline{W}$ , and  $\overline{CNRST} = V_{IH}$ .
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance<sup>(1)</sup>



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## Timing Waveform of Counter Reset<sup>(2)</sup>



4831 drw 13

### NOTES:

- $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $R/\overline{W}$  =  $V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST}$  =  $V_{IH}$ .
- $\overline{CE}_0$ ,  $\overline{BE}_n$  =  $V_{IL}$ ;  $CE_1$  =  $V_{IH}$ .
- The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
- Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: ADDR 0 will be accessed. Extra cycles are shown here simply for clarification.
- $\overline{CNTEN} = V_{IL}$  advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

## Functional Description

The IDT70V3569 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on  $\overline{CE_0}$  or a LOW on  $CE_1$  for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3569s for depth expansion configurations. Two cycles are required with  $\overline{CE_0}$  LOW and  $CE_1$  HIGH to re-activate the outputs.

## Depth and Width Expansion

The IDT70V3569 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3569 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

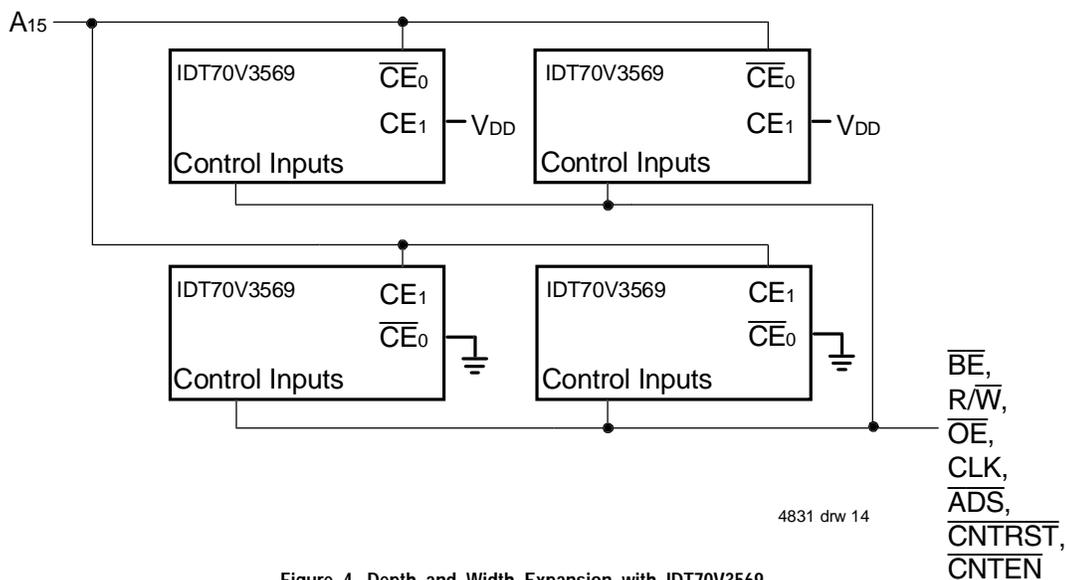


Figure 4. Depth and Width Expansion with IDT70V3569

## Ordering Information

IDT	XXXXX	A	99	A	A	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
					BF DR BC	208-pin fpBGA (BF-208) 208-pin PQFP (DR-208) 256-pin BGA (BC-256)
			4 5 6			Commercial Only Commercial & Industrial Commercial & Industrial
		S				Standard Power
						70V3569 576Kbit (16K x 36-Bit) Synchronous Dual-Port RAM

Speed in nanoseconds

4831 drw 15A

## Datasheet Document History

1/8/99:	Initial Public Release
3/12/99:	Added fpBGA package
4/28/99:	Fixed typo on page 10
6/8/99:	Changed drawing format
	Page 2 Changed package body dimensions
	Page 3 Fixed typo
6/15/99:	Page 5 Deleted note 6 for Table II
8/4/99:	Page 2 Fixed typographical error
	Page 6 Improved power number
10/14/99:	Upgraded speed to 133MHz, added 2.5V I/O capability
10/19/99:	Page 4 Corrected I/O numbers in Truth Table I
11/12/99:	Replaced IDT logo
4/10/00:	Added new BGA packages, added full 2.5V interface capability
1/12/01:	Page 6 Updated Truth Table II
	Increased storage temperature parameter
	Clarified TA Parameter
	Page 8 DC Electrical parameters—changed wording from "open" to "disabled"
	Removed note 7 on DC Electrical Characteristics table
	Removed Preliminary status
4/10/01:	Added Industrial Temperature Ranges and removed related notes



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