

**38-640MHz Low Phase Noise XO**

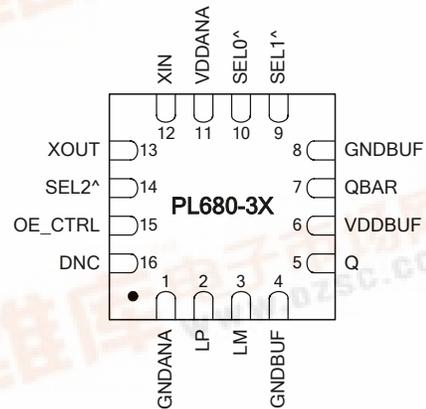
**FEATURES**

- Less than 0.4ps RMS (12KHz-20MHz) phase jitter for all frequencies.
- Less than 25ps peak to peak jitter for all frequencies.
- Low phase noise output (@ 1MHz frequency offset)
  - \* -144dBc/Hz for 106.25MHz
  - \* -144dBc/Hz for 156.25MHz
  - \* -144dBc/Hz for 212.5MHz
  - \* -140dBc/Hz for 312.5MHz,
  - \* -131dBc/Hz for 622.08MHz
- 19MHz-40MHz crystal input.
- 38MHz-640MHz output.
- Available in PECL, LVDS, or CMOS outputs.
- Output Enable selector.
- 2.5V & 3.3V operation.
- Available in 3x3 QFN or 16-pin TSSOP packages.

**PACKAGE PIN ASSIGNMENT**



**16-pin TSSOP**



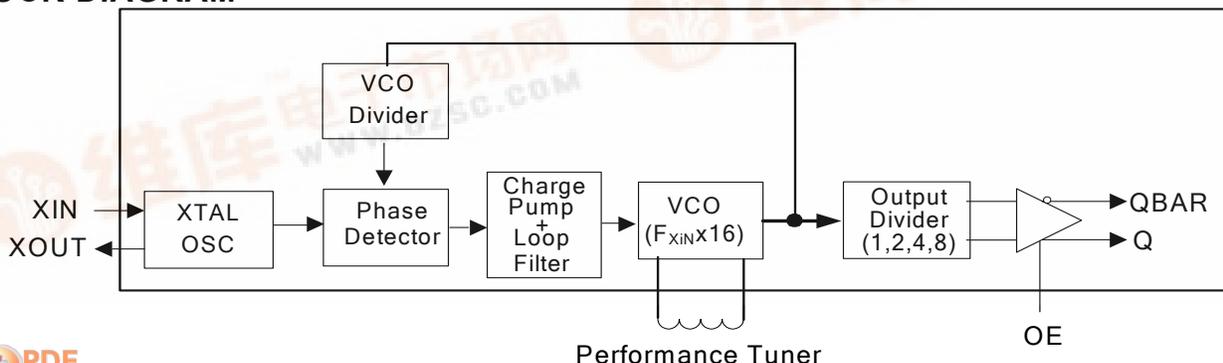
**3x3 QFN**

Note1: QBAR is used for single ended CMOS output.  
Note2: ^ Denotes internal pull up resistor.

**DESCRIPTION**

The PL680-3X is a monolithic low jitter and low phase noise high performance clock, capable of maintaining 0.4ps RMS phase jitter and CMOS, LVDS or PECL outputs, covering a wide frequency output range up to 640MHz. It allows high performance and high frequency output, using a low cost fundamental crystal of between 19-40MHz. The frequency selector pads of PL680-3X enable output frequencies of (2, 4, 8, or 16) \* F<sub>XIN</sub>. The PL680-3X is designed to address the demanding requirements of high performance applications such Fiber Channel, serial ATA, Ethernet, SAN, etc.

**BLOCK DIAGRAM**



**38-640MHz Low Phase Noise XO**

**OUTPUT ENABLE LOGICAL LEVELS**

Part #	OE	State
PL680-38 (PECL)	0 (Default)	Output enabled
	1	Tri-state
PL680-37 & 39 (CMOS or LVDS)	0	Tri-state
	1 (Default)	Output enabled

**PIN DESCRIPTIONS**

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
VDDANA	1	11	P	VDD for analog Circuitry.
XIN	2	12	I	Crystal input pin. (See Crystal Specifications on page 3).
XOUT	3	13	O	Crystal output pin. (See Crystal Specifications on page 3).
SEL2	4	14	I	Output frequency Selector pin.
OE_CTRL	5	15	I	Output enable control pin. (See OE_CTRL Logic Levels on page 1).
DNC	6	16	-	Do Not Connect
GNDANA	7	1	P	Ground for analog circuitry.
LP	8	2	-	Tuning inductor connection. The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between LP and adjacent LM pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.
LM	9	3	-	
GNDBUF	10	4	P	GND connection for output buffer circuitry.
Q	11	5	O	PECL or LVDS output.
VDDBUF	12	6	P	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
QBAR	13	7	O	Complementary PECL, LVDS output; Or single ended CMOS output.
GNDBUF	14	8	P	GND connection for output buffer circuitry.
SEL1	15	9	I	Output frequency Selector pin.
SEL0	16	10	I	Output frequency Selector pin.

**FREQUENCY SELECTION TABLE**

SEL2	SEL1	SEL0	Selected Multiplier/Output Frequency
0	0	0	VCO Max*
0	0	1	VCO Min*
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Fin x 2
1	0	1	Fin x 8
1	1	0	Fin x 16
1	1	1	Fin x 4

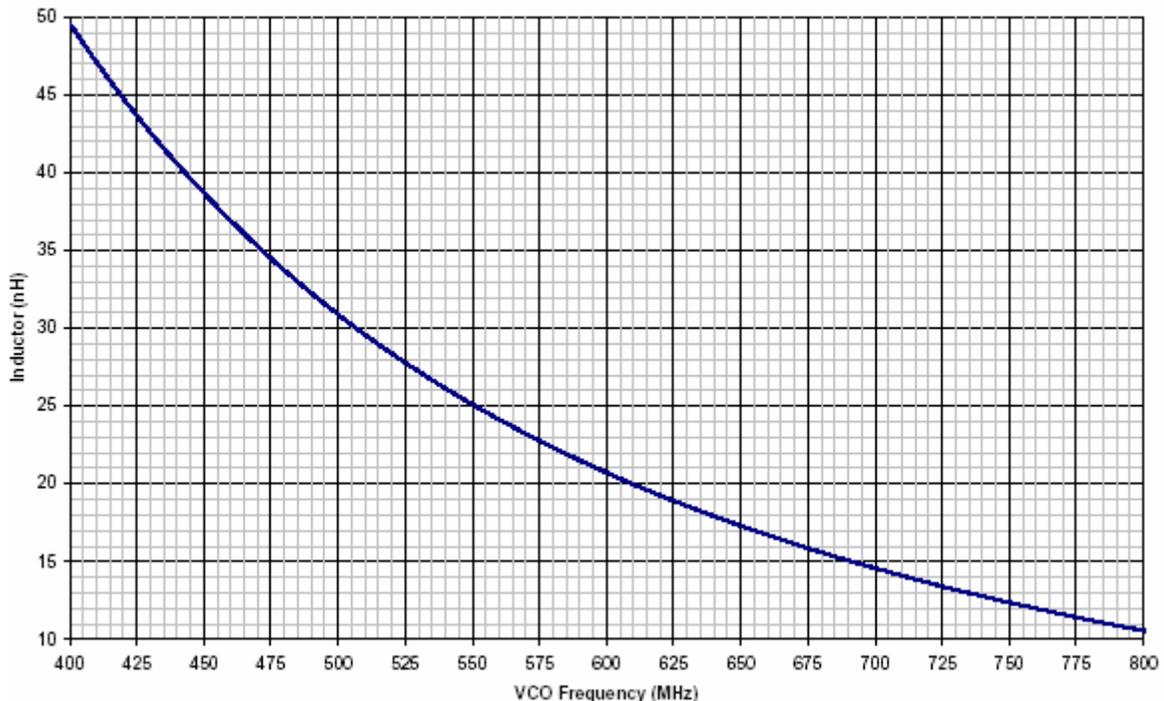
All SEL pads have internal pull-ups (default value is '1'). Bond to GND to set to 0.

\* Special Test Modes to help selecting the inductor value for the target output frequency.

**PERFORMANCE TUNING & INDUCTOR VALUE SELECTION**

Please refer to PhaseLink's 'PhasorV Tuning Assistance' software to automatically calculate the optimum inductor values. In addition, the chart below could be used as a reference for quick inductor value selection.

Use the special test modes "VCO Max" and "VCO Min" to determine the optimum inductor value. "VCO Max" represents the high end of the VCO range and "VCO Min" represents the low end of the VCO range. The output frequency in the "VCO Max" and "VCO Min" test modes is VCO/16. This means that the output frequencies are around the crystal frequency that will be used. The optimum inductor value is where the target crystal frequency is closest to the middle between the "VCO Max" and "VCO Min" output frequencies. In this case the VCO will lock in the middle of its tuning range with maximum margin on either side.



**38-640MHz Low Phase Noise XO**

**ELECTRICAL SPECIFICATIONS**

**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_i$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_o$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_s$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

**2. Crystal Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	19		40	MHz
Crystal Loading Rating	$C_L (xtal)$			17.7		pF
Crystal Shunt Capacitance	$C_0 (xtal)$				5	pF
Recommended ESR	$R_E$	AT cut			30	$\Omega$

**Note:** Crystal Loading rating: 17.7pF is the loading the crystal sees from the XO chip. It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires less load to be at nominal frequency, then a capacitor can be placed in series with the crystal. If the crystal requires more load to be at nominal frequency, capacitors can be placed from XIN and XOUT to ground. This however may reduce the oscillator gain.

**3. General Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	$I_{DD}$	PECL/LVDS/CMOS	38MHz< $F_{out}$ <320MHz			65/45/30	mA
		PECL/LVDS	320MHz< $F_{out}$ <640MHz			90/70	
Operating Voltage	$V_{DD}$			2.25		3.63	V
Output Clock Duty Cycle		@ 50% $V_{DD}$ (CMOS)		45	50	55	%
		@ 1.25V (LVDS)		45	50	55	
		@ $V_{DD} - 1.3V$ (PECL)		45	50	55	
Short Circuit Current					±50		mA

**Note:** CMOS operation is not advised above 200MHz with 15pF load; and 320MHz with 10pF load.

**38-640MHz Low Phase Noise XO**

**4. Jitter Specifications**

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Integrated jitter RMS	Integrated 12 kHz to 20 MHz	106.25MHz		0.4	0.5	ps
		156.25MHz		0.4	0.5	
		212.5MHz		0.4	0.5	
		312.5MHz		0.4	0.5	
		622.08MHz		0.4	0.5	
Period jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	106.25MHz		3	5	ps
		156.25MHz		3	5	
		212.5MHz		3	5	
		312.5MHz		3	5	
		622.08MHz		6	8	
Period jitter Peak-to-Peak	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	106.25MHz		20	30	ps
		156.25MHz		20	30	
		212.5MHz		20	30	
		312.5MHz		20	30	
		622.08MHz		40	50	

**5. Phase Noise Specifications**

PARAMETERS	FREQ.	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1M	@10M	UNITS
Phase Noise relative to carrier (typical)	106.25MHz	-66	-96	-122	-132	-126	-144	-150	dBc/Hz
	156.25MHz	-62	-92	-120	-132	-128	-140	-150	
	212.5MHz	-62	-92	-118	-126	-120	-140	-150	
	312.5MHz	-59	-85	-117	-128	-125	-139	-148	
	622.08MHz	-49	-84	-111	-120	-118	-128	-138	

**6. CMOS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V	30			mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V	30			mA
Output Clock Rise/Fall Time		0.3V ~ 3.0V with 15 pF load		0.7		ns
Output Clock Rise/Fall Time		20%-80% with 50Ω Load		0.3		ns

**38-640MHz Low Phase Noise XO**

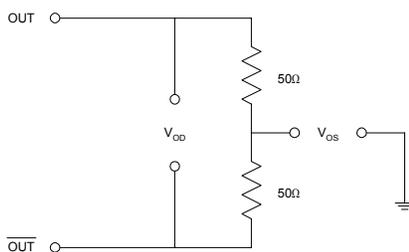
**8. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

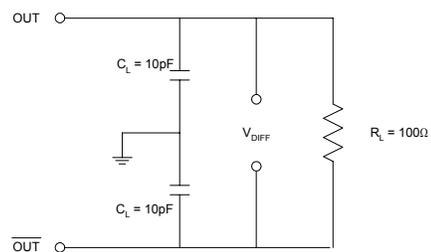
**9. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

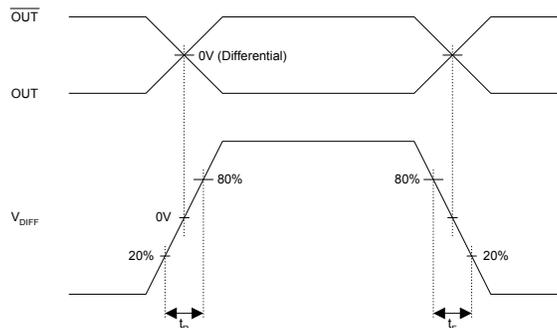
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



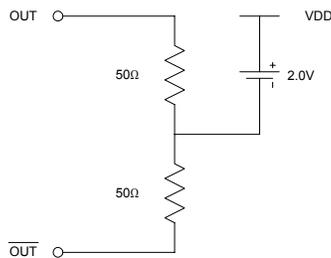
**10. PECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

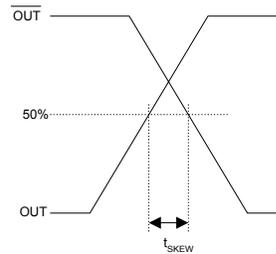
**11. PECL Switching Characteristics**

PARAMETERS	SYMBOL	FREQ.	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise & Fall Times	tr&tf	<150MHz		0.2	0.5	0.7	ns
Clock Rise & Fall Times		>150MHz <320MHz		0.2	0.4	0.55	
Clock Rise & Fall Times				0.2	0.3	0.45	

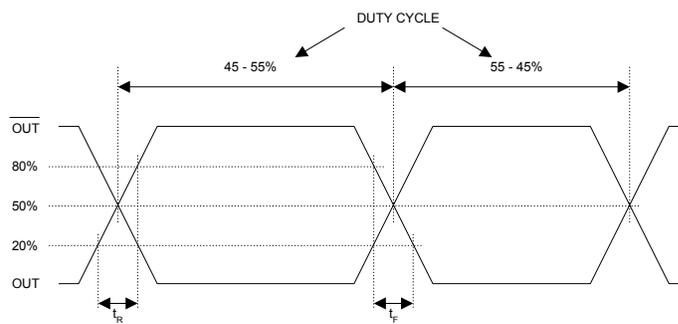
PECL Levels Test Circuit



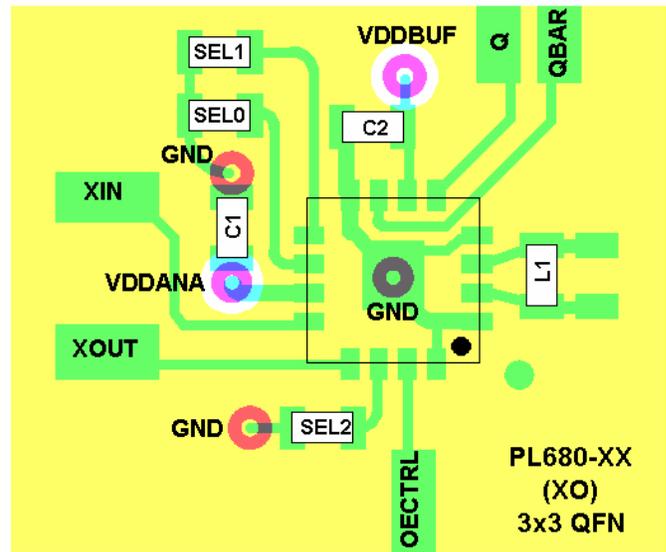
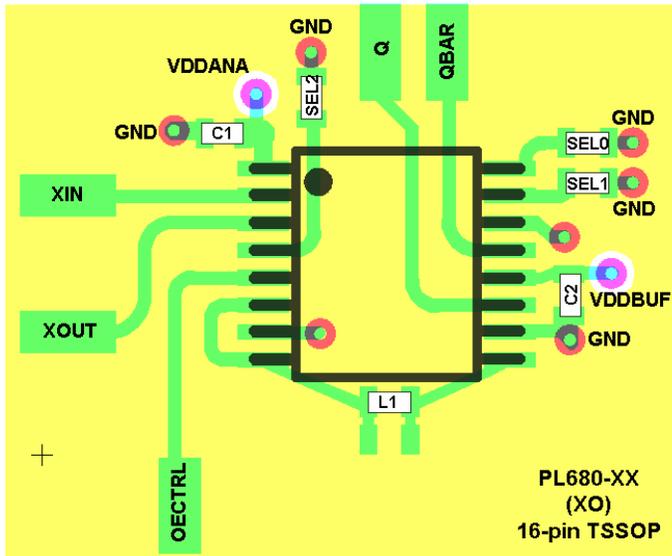
PECL Output Skew



PECL Transition Time Waveform



**LAYOUT RECOMMENDATIONS**



**PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION**

The following guidelines are to assist you with a performance optimized PCB design:

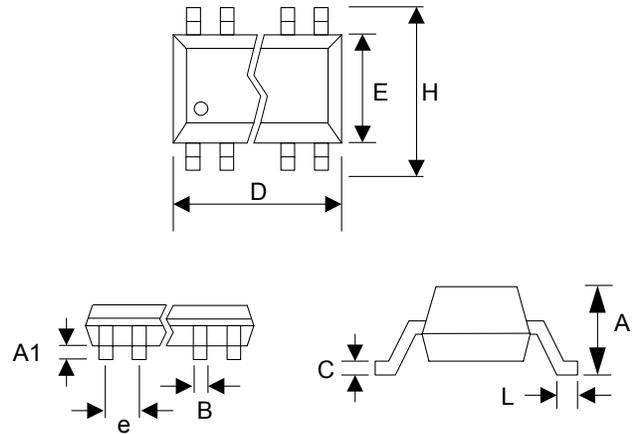
- Keep all the PCB traces to PL680 as short as possible, as well as keeping all other traces as far away from it as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.
- Please contact PhaseLink for the application note on how to design outputs driving long traces or the Gerber files for the PL680 layout.

**38-640MHz Low Phase Noise XO**

**PACKAGE INFORMATION**

**16-PIN SSOP**

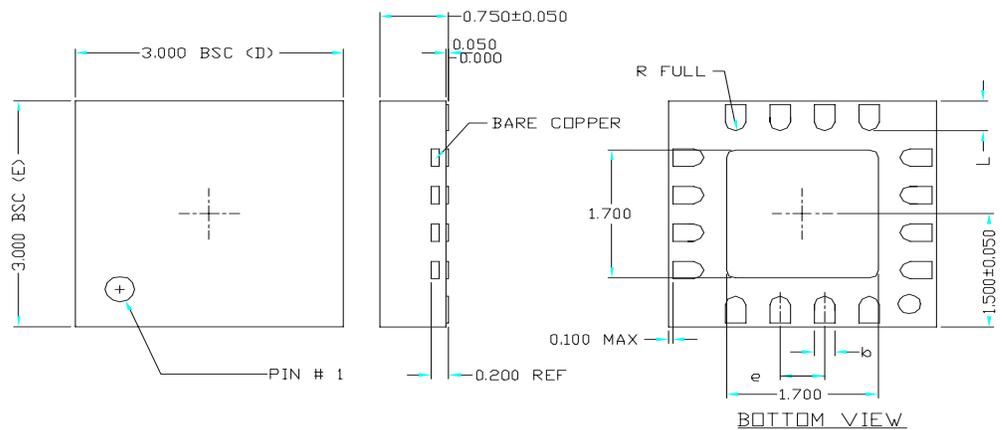
16 PIN TSSOP ( mm )		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



**16-PIN 3x3 QFN**

VARIATIONS:

SYMBOL	16 LD		
	MIN	NDM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		



**38-640MHz Low Phase Noise XO**

**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

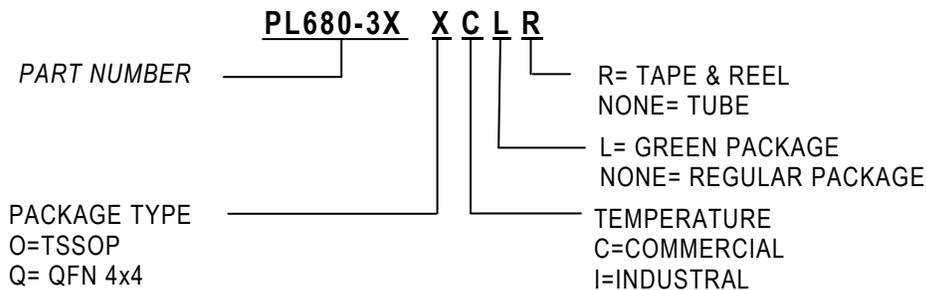
47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range



Order Number	Marking	Marking
PL680-37OC	P680-37OC	TSSOP - Tube
PL680-37OC-R	P680-37OC	TSSOP - Tape & Reel
PL680-37OCL	P680-37OCL	TSSOP - Tube (GREEN Package)
PL680-37OCL-R	P680-37OCL	TSSOP - Tape & Reel (GREEN Package)
PL680-37QC	P680-37QC	QFN - Tube
PL680-37QC-R	P680-37QC	QFN - Tape & Reel
PL680-37QCL	P680-37QCL	QFN - Tube (GREEN Package)
PL680-37QCL-R	P680-37QCL	QFN - Tape & Reel (GREEN Package)
PL680-38OC	P680-38OC	TSSOP - Tube
PL680-38OC-R	P680-38OC	TSSOP - Tape & Reel
PL680-38OCL	P680-38OCL	TSSOP - Tube (GREEN Package)
PL680-38OCL-R	P680-38OCL	TSSOP - Tape & Reel (GREEN Package)
PL680-38QC	P680-38QC	QFN - Tube
PL680-38QC-R	P680-38QC	QFN - Tape & Reel
PL680-38QCL	P680-38QCL	QFN - Tube (GREEN Package)
PL680-38QCL-R	P680-38QCL	QFN - Tape & Reel (GREEN Package)
PL680-39OC	P680-39OC	TSSOP - Tube
PL680-39OC-R	P680-39OC	TSSOP - Tape & Reel
PL680-39OCL	P680-39OCL	TSSOP - Tube (GREEN Package)
PL680-39OCL-R	P680-39OCL	TSSOP - Tape & Reel (GREEN Package)
PL680-39QC	P680-39QC	QFN - Tube
PL680-39QC-R	P680-39QC	QFN - Tape & Reel
PL680-39QCL	P680-39QCL	QFN - Tube (GREEN Package)
PL680-39QCL-R	P680-39QCL	QFN - Tape & Reel (GREEN Package)

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

**LIFE SUPPORT POLICY:** PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.