DALLAS SEMICONDUCTOR MAXIM

DS17485/DS17487
3V/5V Real-Time Clock

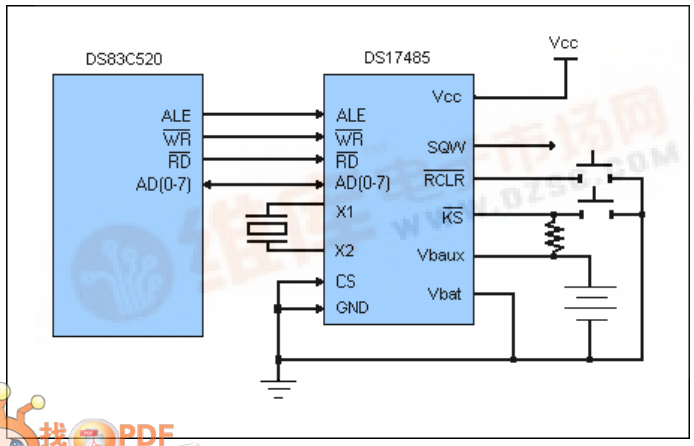
www.maxim-ic.com

FEATURES

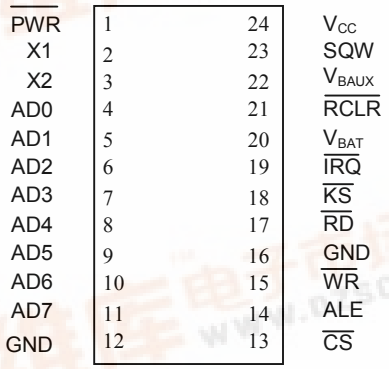
Incorporates industry standard DS1287 PC clock plus enhanced features:

- Y2K compliant
- +3V or +5V operation
- SMI recovery stack
- 64-bit silicon serial number
- Power-control circuitry supports system power-on from date/time alarm or key closure
- 32kHz output on power-up
- Crystal select bit allows RTC to operate with 6pF or 12.5pF crystal
- 114 bytes user NV RAM
- Auxiliary battery input
- 4kB additional NV RAM
- RAM clear input
- Century register
- Date alarm register
- Compatible with existing BIOS for original DS1287 functions
- Available as chip (DS17485) or standalone module with embedded battery and crystal (DS17487)
- Timekeeping algorithm includes leap-year compensation valid up to 2100
- Underwriters Laboratory (UL) recognized

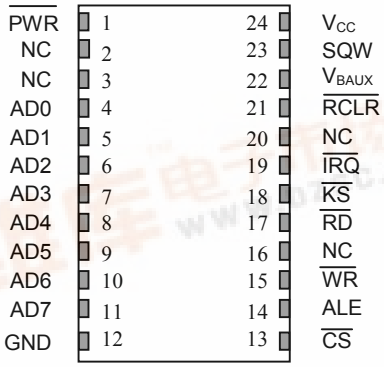
TYPICAL OPERATING CIRCUIT



PIN ASSIGNMENT



DS17485 24-Pin DIP
DS17485S 24-Pin SO



DS17487 24-Pin
Encapsulated Package

DS17485E 28-Pin TSOP

ORDERING INFORMATION

PART #	DESCRIPTION
DS17485XX-X	RTC Chip
3	+3V operating range
5	+5V operating range
blank	commercial temp range
N	industrial temp range
blank	24-pin DIP
E	28- pin TSOP
S	24- pin SO
DS17487X-X	RTC Module; 24-pin DIP
3	+3V operating rang
5	+5V operating range
blank	commercial temp range
N	industrial

PIN DESCRIPTION

X1	-	Crystal Input
X2	-	Crystal Output
$\overline{RCLR}$	-	RAM Clear Input
AD0–AD7	-	Multiplexed Address/Data Bus
$\overline{PWR}$	-	Power-On Interrupt Output (Open Drain)
$\overline{KS}$	-	Kickstart Input
$\overline{CS}$	-	RTC Chip-Select Input
ALE	-	RTC Address Strobe
$\overline{WR}$	-	RTC Write Data Strobe
$\overline{RD}$	-	RTC Read Data Strobe
$\overline{IRQ}$	-	Interrupt Request Output (Open Drain)
SQW	-	Square-Wave Output
VCC	-	+3V or +5V Main Supply
GND	-	Ground
VBAT	-	Battery + Supply
VBAUX	-	Auxiliary Battery Supply
NC	-	No Connect

DESCRIPTION

The DS17485/DS17487 are real-time clocks (RTC) designed as successors to the industry standard DS1285, DS1385, DS1485, DS1585, and DS1685 PC real-time clocks. These devices provide the industry standard DS1285 clock function with either +3V or +5V operation. The DS17485 also incorporates a number of enhanced features including a silicon serial number, power-on/off control circuitry, 114 bytes of user NV SRAM plus 4kB of additional NV RAM, and 32.768kHz output for sustaining power management activities.

The DS17485/DS17487 power-control circuitry allows the system to be powered on by an external stimulus such as a keyboard or by a time-and-date (wake-up) alarm. The $\overline{PWR}$ output pin is triggered by one or either of these events, and is used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS17485 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS17487 incorporates the DS17485 chip, a 32.768kHz crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas Semiconductor such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS17485/DS17487. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} – DC power is provided to the device on these pins. V_{CC} is the +3V or +5V input.

SQW – Square-Wave Output. The SQW pin provides a 32kHz square-wave output, t_{REC}, after a power-up condition has been detected. This condition sets the following bits, enabling the 32kHz output; DV1 = 1, and E32k = 1. A square wave is output on this pin if either SQWE = 1 or E32k = 1. If E32k = 1, then 32kHz is output regardless of the other control bits. If E32k = 0, then the output frequency is dependent on the control bits in register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A, as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in register B or the E32k bit in extended register 4Bh. A 32kHz SQW signal is output when the enable 32kHz (E32k) bit in extended register 4Bh is a logic 1 and V_{CC} is above V_{PF}. A 32kHz square wave is also available when V_{CC} is less than V_{PF} if E32k = 1, ABE = 1, and voltage is applied to the V_{BAUX} pin.

AD0 to AD7 – Multiplexed Bidirectional Address/Data Bus. Multiplexed buses save pins because address information time and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS17485 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, at which time the DS17485/DS17487 latches the address. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ pulse. In a read cycle the DS17485/DS17487 outputs 8 bits of data during the latter portion of the $\overline{RD}$ pulse. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high. The address/data bus also serves as a bidirectional data path for the external extended RAM.

ALE – RTC Address Strobe Input; Active High. A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS17485/DS17487.

$\overline{RD}$ –RTC Read Input; Active Low. $\overline{RD}$ identifies the time period when the DS17485/DS17487 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ – RTC Write Input; Active Low. The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed register.

$\overline{CS}$ – RTC Chip-Select Input; Active Low. The chip select signal must be asserted low during a bus cycle for DS17485/DS17487 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles that take place with ALE asserted but without asserting $\overline{CS}$ latches addresses. However, no data transfer occurs.

$\overline{IRQ}$ – Interrupt Request Output; Open Drain, Active Low. The $\overline{IRQ}$ pin is an active low output of the DS17485/DS17487 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to $\overline{IRQ}$'s active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open-drain output and requires an external pullup resistor. The voltage on the pullup supply should be no greater than V_{CC} + 0.2V.

$\overline{PWR}$ – Power-On Output; Open-Drain, Active Low. The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS17485/DS17487, $\overline{PWR}$ can be automatically activated from a kickstart input by the $\overline{KS}$ pin or from a wake-up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled by bits in the Dallas registers. The $\overline{PWR}$ pin can be connected through a pullup resistor to a positive supply. For 5V operation, the voltage of the pullup supply should be no greater than 5.7V. For 3V operation, the voltage on the pullup supply should be no greater than 3.9V.

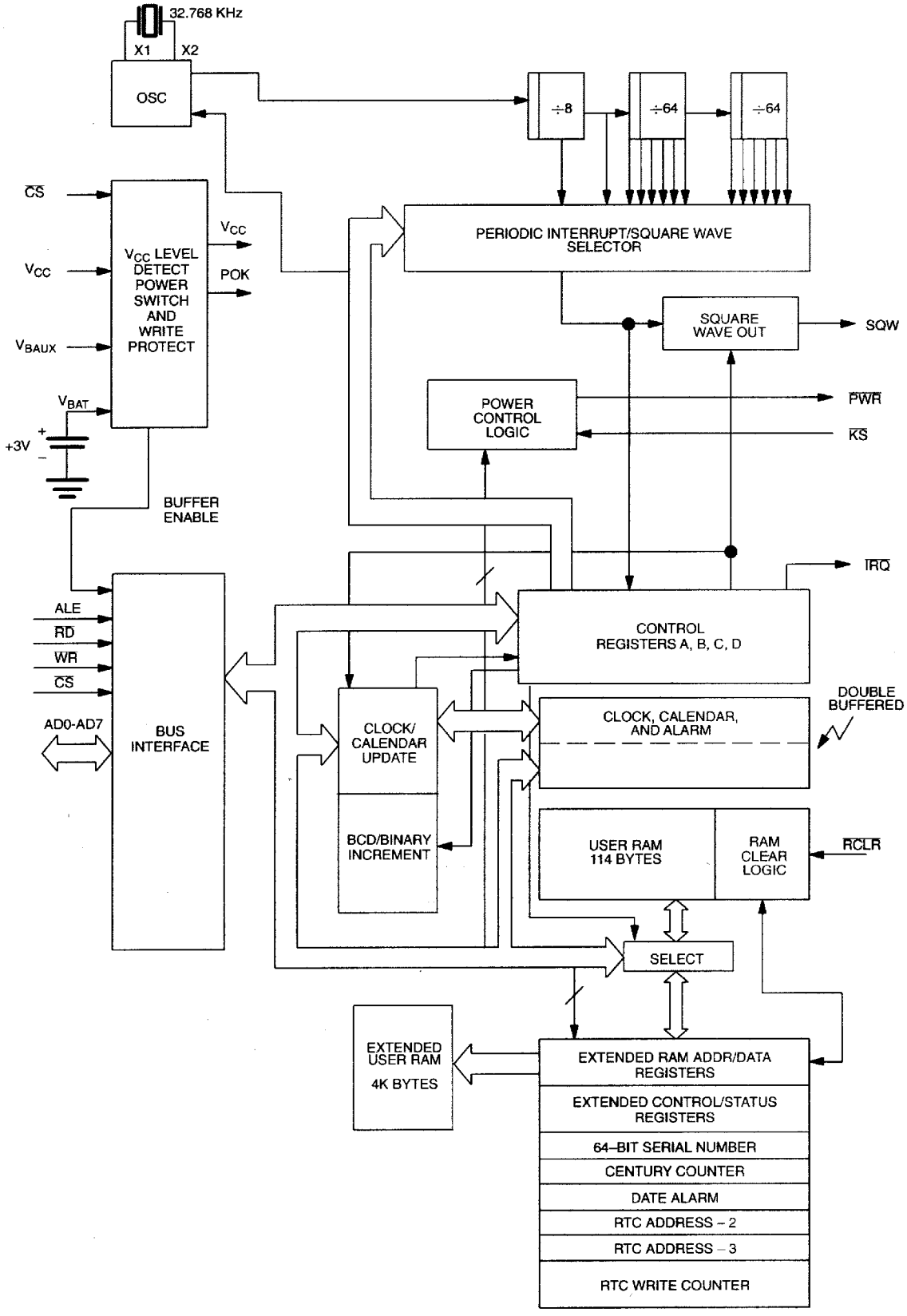
$\overline{KS}$ – Kickstart Input; Active Low. When V_{CC} is removed from the DS17485/DS17487, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and auxiliary-battery-enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ – RAM Clear Input; Active Low. If enabled by software, taking $\overline{RCLR}$ low results in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present. $\overline{RCLR}$ has an internal pullup and should not be connected to an external pullup resistor.

V_{BAUX} – Auxiliary battery input required for kickstart and wake-up features. This input also supports clock/calendar and user RAM if V_{BAT} is at lower voltage or is not present. A standard +3V lithium cell or other energy source can be used. For 3V operation, V_{BAUX} must be held between +2.5V and +3.7V. For 5V operation, V_{BAUX} must be held between +2.5V and +5.2V. If V_{BAUX} is not going to be used it should be grounded and the auxiliary-battery-enable bit bank 1, register 4BH, should = 0.

UL recognized to ensure against reverse charging current when used with a lithium battery. See "Conditions of Acceptability" at www.maxim-ic.com/TechSupport/QA/ntrl.htm.

Figure 1. BLOCK DIAGRAM



DS17485 ONLY

X1, X2 – Connections for a standard 32.768kHz quartz crystal. For greatest accuracy, the DS17485 must be used with a crystal that has a specified load capacitance of either 6pF or 12.5pF. The crystal select (CS) bit in extended-control register 4B is used to select operation with a 6pF or 12.5pF crystal. The crystal is attached directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high-impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.

For more information about crystal selection and crystal layout considerations, refer to *Application Note 58*, "Crystal Considerations with Dallas Real-Time Clocks." The DS17485 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

V_{BAT} – Battery input for any standard 3V lithium cell or other energy source. Battery voltage must be held between 2.5V and 3.7V for proper operation. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery. See "Conditions of Acceptability" at www.maxim-ic.com/TechSupport/AQ/ntrl.htm.

POWER-DOWN/POWER-UP CONSIDERATIONS

The RTC function continues to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS17485/DS17487 and reaches a level of greater than V_{PF} (power-fail trip point), the device becomes accessible after t_{REC}, provided that the oscillator is running and the oscillator countdown chain is not in reset (Register A). This time period allows the system to stabilize after power is applied.

The DS17485/DS17487 is available in either a 3V or a 5V device.

The 5V device is fully accessible and data can be written and read only when V_{CC} is greater than 4.5V. When V_{CC} is below 4.5V, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below the greater of V_{BAT} and V_{BAUX}, the RAM and timekeeper are switched over to a lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin.

The 3V device is fully accessible and data can be written or read only when V_{CC} is greater than 2.7V. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply (the greater of $_{VBAT}$ and V_{BAUX}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT} and V_{BAUX}, the power supply is switched from V_{CC} to the backup supply when V_{CC} drops below the larger of V_{BAT} and V_{BAUX}.

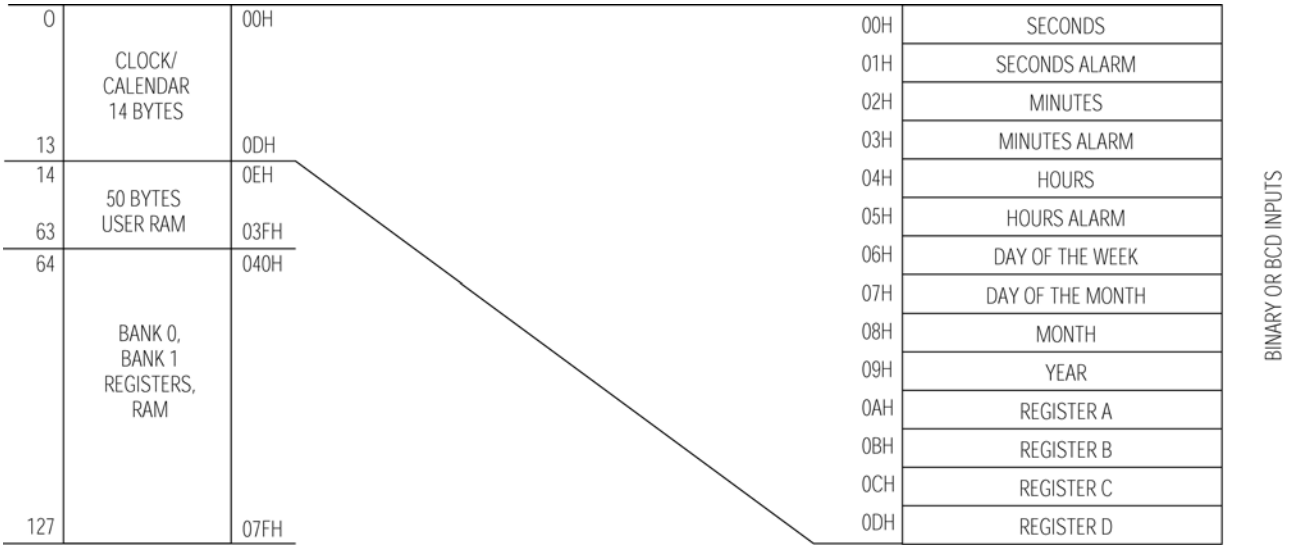
When V_{CC} falls below V_{PF}, the chip is write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, $\overline{RCLR}$, and SQW pins, all inputs are ignored and all outputs are in a high-impedance state.

RTC ADDRESS MAP

The address map for the RTC registers of the DS17485/DS17487 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and 4 bytes are used for control and status. All registers can be directly written or read except for the following:

1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.
3) The high order bit of the second byte is read-only.

Figure 2. DS17485 REAL-TIME CLOCK ADDRESS MAP



TIME, CALENDAR, AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either binary or binary-coded decimal (BCD) format. Table 1 shows the binary and BCD formats of the 10 time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching is explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic 1 to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD) should be set by the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic 1. The time, calendar, and alarm bytes are always accessible because they are double-buffered. Once per second the 10 bytes are advanced by 1 second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three time alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a “don’t care” state in one or more of the three time alarm bytes. The “don’t care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don’t care” condition when at logic 1. An alarm is generated each hour when the “don’t care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don’t care” codes in the hours and minute alarm bytes. The “don’t care” codes in all three time alarm bytes create an interrupt every second. The three time-alarm bytes can be used with the date alarm as described in *Wake-Up/Kickstart*. The century counter is discussed later in this text.

Table 1. TIME, CALENDAR, AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
OOH	Seconds	0 to 59	00 to B	00 to 59
01H	Seconds Alarm	0 to 59	00 to 3B	00 to 59
02H	Minutes	0 to 59	00 to 3B	00 to 59
03H	Minutes Alarm	0 to 59	00 to 3B	00 to 59
04H	Hours 12-hour Mode	1 to 12	01 to 0C AM, 81 to 8C PM	01 to 12 AM, 81 to 92 PM
	Hours 24-hour Mode	0 to 23	00 to 17	00 to 23
05H	Hours Alarm 12-hour Mode	1 to 12	01 to 0C AM, 81 to 8C PM	01 to 12 AM, 81 to 92 PM
	Hours Alarm 24-hour Mode	0 to 23	00 to 17	00 to 23
06H	Days of the Week Sunday = 1	1 to 7	01 to 07	01 to 07
07H	Date of Month	1 to 31	01 to 1F	01 to 31
08H	Month	1 to 12	01 to 0C	01 to 12
09H	Year	0 to 99	00 to 63	00 to 99
BANK 1, 48H	Century	0 to 99	00 to 63	00 to 99
BANK 1, 49H	Date Alarm	1 to 31	01 to 1F	01 to 31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

REGISTER A

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP – Update-in-Progress. The UIP bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer occurs soon. When UIP is a 0, the update transfer does not occur for at least 244µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 – These bits are defined as follows:

DV2 = Countdown Chain
1 – Resets countdown chain only if DV1 = 1
0 – Countdown chain enabled

DV1 = Oscillator Enable
0 – Oscillator off
1 – Oscillator on, V_{CC} power-up state

DV0 = Bank Select
0 – Original bank
1 – Extended registers

A pattern of 01x is the only combination of bits that turns the oscillator on and allows the RTC to keep time. A pattern of 11x enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 01x is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 – These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

- Enable the interrupt with the PIE bit;
- Enable the SQW output pin with the SQWE or E32k bits;
- Enable both at the same time and the same rate; or
- Enable neither.

Table 2 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET – When the SET bit is a 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS17485/DS17487.

PIE – Periodic Interrupt Enable. The PIE bit is a read/write bit, which allows the periodic interrupt flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal DS17485/DS17487 functions.

AIE – Alarm Interrupt Enable. The AIE bit is a read/write bit which, when set to a 1, permits the alarm flag (AF) bit in Register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS17485/DS17487 do not affect the AIE bit.

UIE – Update-Ended Interrupt Enable. The UIE bit is a read/write bit that enables the update-end flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE – Square-Wave Enable. When the SQWE bit is set to a 1 and E32k = 0, a square-wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to 0and E32k = 0, the SQW pin is held low. SQWE is a read/write bit. SQWE is set to a 1 when V_{CC} is powered up.

DM – Data Mode. The DM bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A 1 in DM signifies binary data while a 0 in DM specifies BCD data.

24/12 – 24/12-Control Bit. This bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write.

DSE – Daylight Savings Enable. The DSE bit is a read/write bit that enables two special updates when DSE is set to 1. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October, when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF – Interrupt Request Flag. This bit is set to a 1 when one or more of the following are true:

PF = PIE = 1 WF = WIE= 1
AF = AIE = 1 KF = KSE= 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF x PIE) + (AF x AIE) + (UF x UIE) + (WF x WIE) + (KF x KSE) + (RF x RIE)

Any time the IRQF bit is a 1, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF – Periodic Interrupt Flag. This is a read-only bit that is set to a 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{IRQ}$ signal is active and sets the IRQF bit. The PF bit is cleared by a software read of Register C.

AF – Alarm Interrupt Flag. A 1 in the AF bit indicates that the current time has matched the alarm time. If the AIE bit is also a 1, the $\overline{IRQ}$ pin goes low and a 1 appears in the IRQF bit. A read of Register C clears AF.

UF – Update Ended Interrupt Flag. This bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be a 1, which asserts the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 3 to BIT 0 – These are unused bits of the status Register C. These bits always read 0 and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – Valid RAM and Time. This bit is a read-only status bit. When VRT = 0, the RTC and RAM data are questionable and indicates that the lithium energy source has been exhausted and should be replaced. This bit indicates that status of the V_{BAT} and V_{BAUX} inputs.

BIT 6 to BIT 0 – The remaining bits of Register D are not usable. They cannot be written and, when read, they always read 0.

NV RAM–RTC

The general-purpose NV RAM bytes are not dedicated to any special function within the DS17485/DS17487. They can be used by the application program as nonvolatile memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real-time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 4kB of user RAM are accessible through the extended RAM address and data registers.

INTERRUPT CONTROL

The DS17485/DS17487 includes six separate, fully automatic sources of interrupt for a processor:

1) Alarm Interrupt
2) Periodic Interrupt
3) Update-Ended Interrupt
4) Wake-Up Interrupt
5) Kickstart Interrupt
6) RAM Clear Interrupt

The conditions that generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, should be used. There are 6 bits including 3 bits in Register B and 3 bits in Extended Register 4B that enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register 4A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register 4B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C because they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits that are set remain stable throughout the read cycle. All bits that were set are cleared when read and new interrupts that are pending during the read cycle are held until after the cycle is completed. 1 bit, 2 bits, or 3 bits can be set when reading Register C. Each used flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register 4A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line is driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ is held low as long as at least one of the six

possible interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS17485/DS17487 initiated an interrupt is accomplished by reading Register C and finding IRQF = 1. IRQF remains set until all enabled interrupt flag bits are cleared to 0.

OSCILLATOR CONTROL BITS

When the DS17487 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 01X in bits 4 through 6 of Register A turns the oscillator on and enable the countdown chain. Not that this is different than the dS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1. A pattern of 11X turns the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE-WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768kHz crystal tied to X1 and X2. The square-wave output is enabled and disabled through the SQWE bit in Register B or the E32k bit in extended register 4Bh. If the square wave is enabled (SQWE = 1 or E32k = 1), then the output frequency is determined by the settings of the E32k bit in Extended Register 4Bh and by the RS3–0 bits in Register A. If E32k = 1, then a 32.768kHz square wave is output on the SQW pin regardless of the settings of RS3–0 and SQWE.

If E32k = 0, then the square-wave output frequency is determined by the RS3–0 bits. These bits control a 1-of-15 decoder that selects one of 13 taps that divide the 32.768kHz frequency. The RS3–0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3–0 bits control the periodic interrupt selection as described below.

If E32k = 1, and the auxiliary-battery-enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX}, then the 32kHz square-wave output signal is output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power-management circuitry. If any of the above requirements are not met, no square-wave output signal is generated on the SQW pin in the absence of V_{CC}.

PERIODIC INTERRUPT SELECTION

The periodic interrupt causes the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3–0 bits in Register A, which select the square-wave frequency (Table 2). Changing the bits affects both the square-wave frequency and the periodic-interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32k bits control the square-wave output. Similarly, the PIE bit in Register B enables the periodic interrupt. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 2. PERIODIC INTERRUPT RATE AND SQUARE-WAVE OUTPUT FREQUENCY

EXTENDED REGISTER B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32k	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625ms	256Hz
0	0	0	1	0	7.8125ms	128Hz
0	0	0	1	1	122.070µs	8.192kHz
0	0	1	0	0	244.141µs	4.096kHz
0	0	1	0	1	488.281µs	2.048kHz
0	0	1	1	0	976.5625µs	1.024kHz
0	0	1	1	1	1.953125ms	512Hz
0	1	0	0	0	3.90625ms	256Hz
0	1	0	0	1	7.8125ms	128Hz
0	1	0	1	0	15.625ms	64Hz
0	1	0	1	1	31.25ms	32Hz
0	1	1	0	0	62.5ms	16Hz
0	1	1	0	1	125ms	8Hz
0	1	1	1	0	250ms	4Hz
0	1	1	1	1	500ms	2Hz
1	X	X	X	X	*	32.768kHz

**RS3 to RS0 determine periodic interrupt rates as listed for E32k = 0.*

UPDATE CYCLE

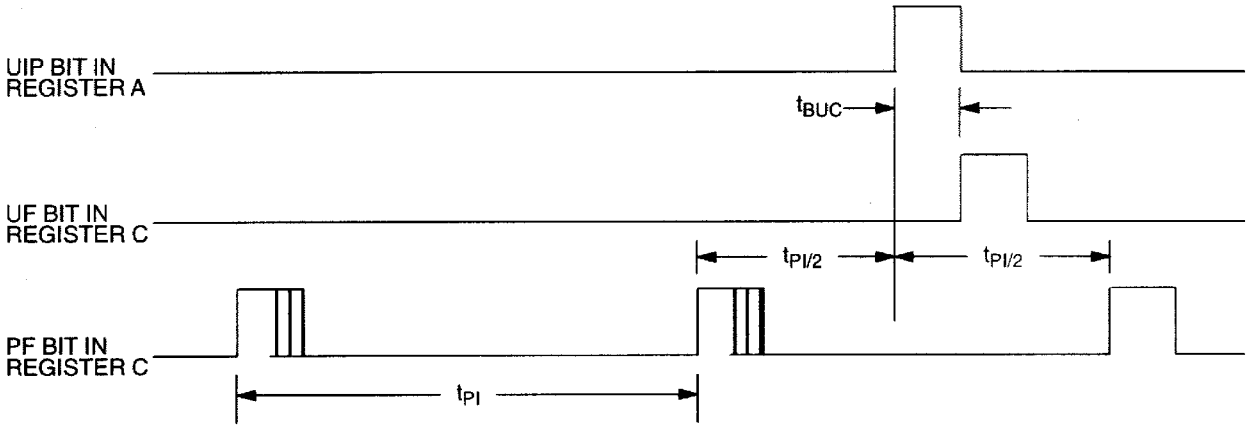
The serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, alarm, and elapsed time byte is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows the time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all alarm locations.

There are three methods that can handle access of the RTC that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999ms is available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data is changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2 + t_{BUC}) to ensure that data is not read during the update cycle.

Figure 3. UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

EXTENDED FUNCTIONS

The extended functions provided by the DS17485/DS17487 that are new to the RAMified RTC family are accessed by a software-controlled bank-switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS17485/DS17487 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers that provide control and status for the extended functions are accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

- 64-bit Silicon Serial Number
- Century Counter
- RTC Write Counter
- Date Alarm
- Auxiliary Battery Control/Status
- Wake-Up
- Kickstart
- RAM Clear Control/Status
- 4kB Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and return a 0 if read.

Silicon Serial Number

A unique 64-bit lasered serial number is located in bank 1, registers 40h–47h. This serial number is divided into three parts. The first byte in register 40h contains a model number to identify the device type of the DS17485/DS17487. Registers 41h–46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h–46h. All 8 bytes of the serial number are read-only registers.

The DS17485/DS17487 is manufactured such that no two devices contain an identical number in locations 41h–47h.

Century Counter

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

RTC Write Counter

An 8-bit counter located in extended register bank 1, 5Eh, counts the number of times the RTC is written to. This counter is incremented on the rising edge of the $\overline{WR}$ signal every time that the $\overline{CS}$ signal qualifies it. This counter is a read-only register and rolls over after 256 RTC write pulses. This counter

can be used to determine if and how many RTC writes have occurred since the last time this register was read.

Auxiliary Battery

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS17485/DS17487 kickstart, wake-up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The auxiliary-battery-enable (ABE; bank 1, register 04BH) bit in extended control register 4B is used to turn the auxiliary battery on and off for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled; when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS17485/DS17487, this auxiliary battery can be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS17485 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and V_{BAT} should be grounded. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

Wake-Up/Kickstart

The DS17485/DS17487 incorporates a wake-up feature that powers on the system at a predetermined date and time through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature allows the system to be powered up in response to a low-going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power can be applied upon such events as a key closure or modem-ring-detect signal. In order to use either the wake-up or the kickstart features, the DS17485/DS17487 must have an auxiliary battery connected to the V_{BAUX} pin, the oscillator must be running, and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin is not driven low in response to a kickstart or wake-up condition, while in battery-backed mode.

The wake-up feature is controlled through the wake-up-interrupt-enable bit in extended control register 4B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake-up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled by the kickstart-interrupt-enable bit in extended control register 4B (KSE, bank 1, 04BH).

A wake-up sequence occurs as follows: When wake-up is enabled through WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar monitors the current date for a match condition with the date alarm register (bank 1, register 049H). With the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake-up occurs at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm occurs regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin is automatically driven low. This output can be used to turn on the main system power supply that provides V_{CC} voltage to the DS17485/DS17487 as well as the other major components in the system. Also at this time, the wake-up flag (WF, bank 1, register 04AH) is set, indicating that a wake-up condition has occurred.

A kickstart sequence occurs when kickstarting is enabled through KSE = 1. While the system is powered down, the $\overline{KS}$ input pin is monitored for a low-going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line is pulled low, as it is for a wake-up condition. Also at this time, the kickstart Flag (KF, bank 1, register 04AH) is set, indicating that a kickstart condition has occurred.

The timing associated with both the wake-up and kickstarting sequences is illustrated in the *Wake-Up/Kickstart Timing Diagram* in the *Electrical Specifications* section of this data sheet. The timing associated with these functions is divided into five intervals, labeled 1 to 5 on the diagram.

The occurrence of either a kickstart or wake-up condition causes the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS17485/DS17487 V_{CC} pin rises above the greater of V_{BAT} or V_{PF} before the power-on timeout period (t_{POTO}) expires, then PWR remains at the active low level. If V_{CC} does not rise above the greater of V_{BAT} or V_{PF} in this time, then the $\overline{PWR}$ output pin is turned off and returns to its high-impedance level. In this event, the $\overline{IRQ}$ pin also remains tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power-on sequence remains set until cleared by software during a subsequent system power-on.

If V_{CC} is applied within the timeout period, then the system power-on sequence continue as shown in intervals 2 to 5 in the timing diagram. During interval 2, $\overline{PWR}$ remains active and $\overline{IRQ}$ is driven to its active low level, indicating that either WF or KF was set in initiating the power-on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit is automatically cleared to 0 in response to a successful power-on. The $\overline{PWR}$ line remains active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing 0's to both of these control bits. As long as no other interrupt within the DS17485/DS17487 is pending, the $\overline{IRQ}$ line is taken inactive once these bits are reset. Execution of the application software can proceed. During this time, both the wake-up and kickstart functions can be used to generate status and interrupts. WF is set in response to a date, hours, minutes, and seconds match condition. KF is set in response to a low-going transition on $\overline{KS}$. If the associated interrupt-enable bit is set (WIE and/or KSE), then the $\overline{IRQ}$ line is driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS17485/DS17487 can cause $\overline{IRQ}$ to be driven low. While system power is applied, the on-chip logic always attempts to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake-up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake-up or kickstart.

The system can be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high-impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin is placed in a high-impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake-up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and NV RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake-up and kickstart takes place. If PRS = 1, $\overline{PWR}$ stays active; otherwise, if PRS = 0 $\overline{PWR}$ is tri-stated.

RAM Clear

The DS17485/DS17487 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled through the RAM clear-enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM is cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action has no affect on either the clock/calendar settings or upon the contents of the extended RAM. The RAM clear flag (RF, bank 1, register 04AH) is set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE = 1, the $\overline{IRQ}$ line is also be driven low upon completion. The interrupt condition can be cleared by writing a 0 to the RF bit. The $\overline{IRQ}$ line then returns to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in *Electrical Characteristics*.

When RCE is cleared to 0, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin has no affect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no affect on RF.

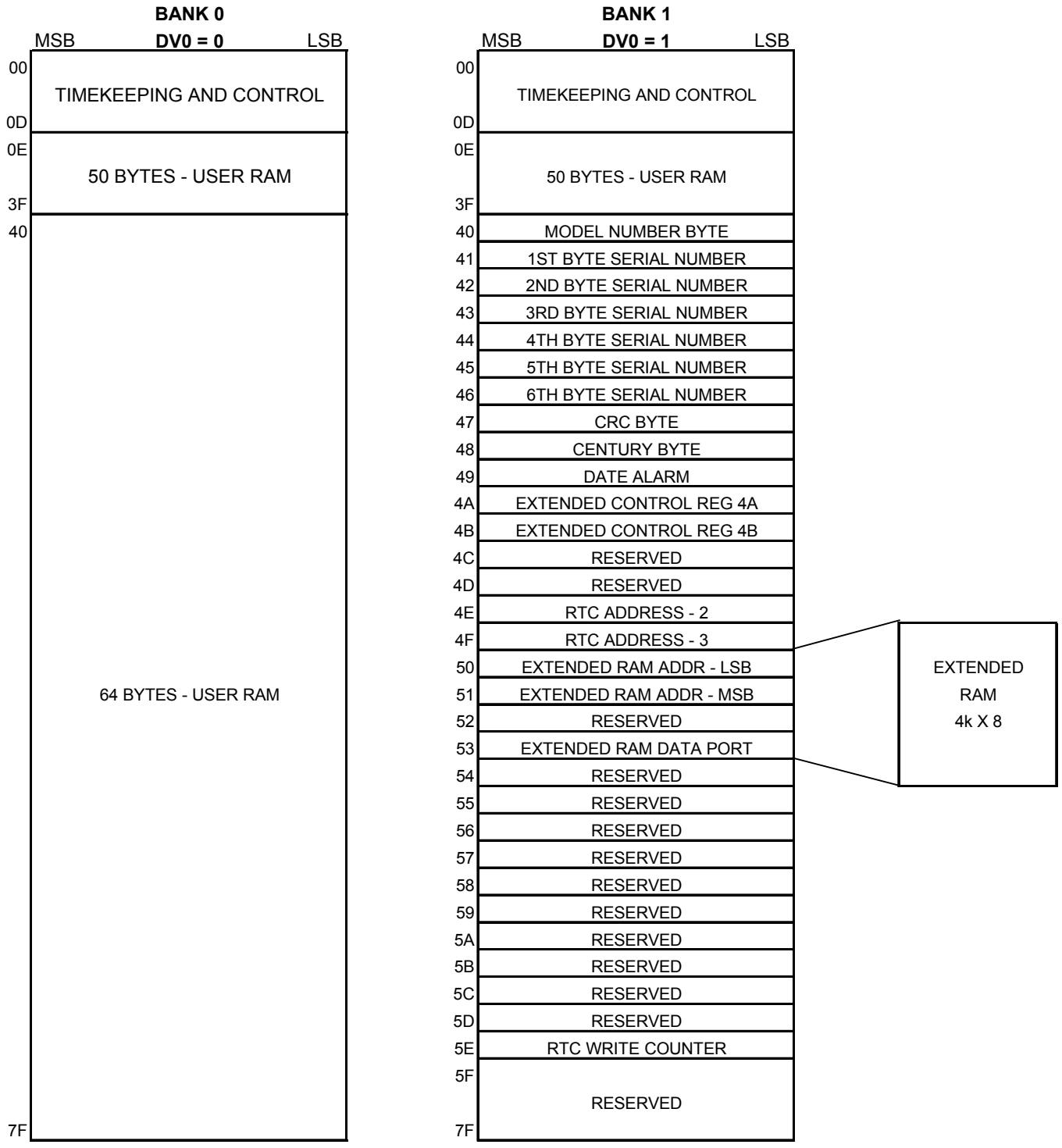
4k x 8 Extended RAM

The DS17485/DS17487 provides 4k x 8 of on-chip SRAM that is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power-OK signal (POK) generated from the write-protect circuitry. The on-chip 4k x 8 NV SRAM is accessed through the eight multiplexed address/data lines AD7 to AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the other register is used to hold read/write data. The SRAM address space is from 00h to 0FFFh.

Access to the extended 4k x 8 RAM is controlled by three of the Dallas registers shown in Figure 4. The Dallas registers in bank 1 must first be selected by setting the DV0 bit in register A to a logic 1. The 12-bit address of the RAM location to be accessed must be loaded into the extended RAM address registers located at 50h and 51h. The least significant address byte should be written to location 50h, and the most significant 4-bits (right-justified) should be loaded in location 51h. Data in the addressed location can be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location can be read or written repeatedly without changing the address in location 50h and 51h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit in the extended control register 4Ah, to a logic 1. With burst mode enabled, write the extended RAM starting address location to registers 50h and 51h. Then read or write the extended RAM data from/to register 53h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{RD}$ or $\overline{WR}$ only when register 53h is being accessed. Refer to the *Burst Mode Timing Waveform.*

Figure 4. DS17485/DS17487 EXTENDED REGISTER BANK DEFINITION



EXTENDED CONTROL REGISTERS

Two extended control registers are provided to supply controls and status information for the extended features offered by the DS17485/DS17487. These are designated as extended control registers 4A and 4B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

EXTENDED CONTROL REGISTER 4A

MSB							**LSB**
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	BME	*	PAB	RF	WF	KF

VRT2 – Valid RAM and Time 2. A read-only status bit. When VRT2 = 0, the RTC and RAM data are questionable and indicates that the lithium energy source connected to the V_{BAUX} input has been exhausted and should be replaced. This bit indicates the status of the V_{BAUX} input.

INCR – Increment in Progress Status. This bit is set to a 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR is set to a 1 at 122µs before the update cycle starts and is cleared to 0 at the end of each update cycle.

BME – Burst Mode Enable. The burst mode enable bit allows the extended user RAM address registers to automatically increment for consecutive reads and writes. When BME is set to a logic 1, the automatic incrementing is enabled and when BME is set to a logic 0, the automatic incrementing is disabled.

PAB – Power-Active Bar-Control. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. When this bit is 1, the $\overline{PWR}$ pin is in the high-impedance state. This bit can be written to a logic 1 or 0 by the user. If either WF and WIE = 1 or KF and KSE = 1, the PAB bit is cleared to 0.

RF – Ram Clear Flag. This bit is set to a logic 1 when a high-to-low transition occurs on the $\overline{RCLR}$ input if RCE = 1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF – Wake-Up Alarm Flag. This bit is set to 1 when a wake-up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF – Kickstart Flag. This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

*Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no affect on operation.

EXTENDED CONTROL REGISTER 4B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32k	CS	RCE	PRS	RIE	WIE	KSE

ABE – Auxiliary Battery Enable. This bit when written to a logic 1 enables the V_{BAUX} pin for extended functions.

E32k – Enable 32.768kHz Output. This bit when written to a logic 1 enables the 32.768kHz oscillator frequency to be output on the SQW pin. E32k is set to a 1 when V_{CC} is powered up.

CS – Crystal Select. When CS is set to a 0, the oscillator is configured for operation with a crystal that has a 6pF specified load capacitance. When CS = 1, the oscillator is configured for a 12.5pF crystal. CS is disabled in the DS17487 module and should be set to CS = 0.

RCE – RAM Clear Enable. When set to a 1, this bit enables a low level on $\overline{RCLR}$ to clear all 114 bytes of user RAM. When RCE = 0, $\overline{RCLR}$ and the RAM clear function are disabled.

PRS – PAB Reset Select. When set to a 0, the $\overline{PWR}$ pin is set high-z when the DS17485 goes into power fail. When set to a 1, the $\overline{PWR}$ pin remains active upon entering power fail.

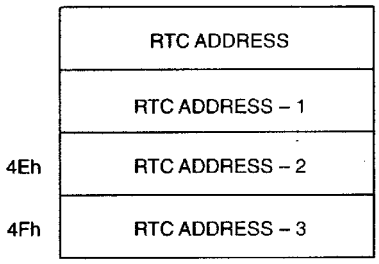
RIE – RAM Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin is driven low when a RAM clear function is completed.

WIE – Wake-up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin is driven active low when a wake-up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit has no affect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE – Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin is driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit has no affect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

SYSTEM MAINTENANCE INTERRUPT (SMI) RECOVERY STACK

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

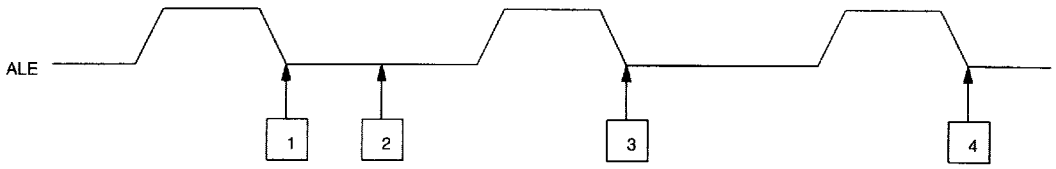


SMI RECOVERY STACK

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. The following waveform illustrates how the BIOS could recover the RTC address when an SMI occurs.



1) The RTC address is latched.
2) An SMI is generated before an RTC read or write occurs.
3) RTC address 0Ah is latched and the address from 1 is pushed to the "RTC Address–1" stack location. This step is necessary to change the bank select bit, DV0 = 1.
4) RTC address 4Eh is latched and the address from 1 is pushed to location 4Eh, "RTC Address–2" while 0Ah is pushed to the "RTC Address–1" location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-0.3V to +7.0V
Storage Temperature Range	-40°C to +85°C
Soldering Temperature Range	+260°C for 10 seconds (DIP) (Note 13) See IPC/JEDEC Standard J-STD-020A for Surface Mount Devices

* This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

OPERATING RANGE

RANGE	TEMP RANGE (°C)	V_{CC}
Commercial	0 to +70	3V ±10% or 5V ±10%
Industrial	-40 to +85	3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

Over the operating range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage 5V Operation	V_{CC}	4.5	5.0	5.5	V	
Power Supply Voltage 3V Operation	V_{CC}	2.7	3.0	3.7	V	
Input Logic 1 5V ±10% 3V ±10%	V_{IH}	 2.2 2.0		V_{CC} + 0.3	V	
Input Logic 0	V_{IL}	-0.3		0.6	V	
Battery Voltage	V_{BAT}	2.5		3.7	V	
Auxiliary Battery Voltage; V_{CC} = 5.0V	V_{BAUX}	2.5		5.2	V	
Auxiliary Battery Voltage; V_{CC} = 3.0V	V_{BAUX}	2.5		3.7	V	

DC ELECTRICAL CHARACTERISTICS

Over the operating range (5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		25	50	mA	1, 2
CMOS Standby Current ($\overline{CS}$ = V_{CC} - 0.2V)	I_{CC2}		1	3	mA	1, 2
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	5
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4	V	
Power-Fail Trip Point	V_{PF}	4.25	4.37	4.5	V	3
Battery-Switch Voltage	V_{SW}		V_{BAT}, V_{BAUX}		V	8
Battery Leakage OSC ON	I_{BAT1}		0.50	0.7	µA	11
Battery Leakage OSC OFF	I_{BAT2}		0.050	0.4	µA	11
I/O Leakage	I_{LO}	-1		+1	µA	4
$\overline{PWR}$ Output at 0.4V	I_{OLPWR}			10.0	mA	
$\overline{IRQ}$ Output at 0.4V	I_{OLIRQ}			2.1	mA	

DC ELECTRICAL CHARACTERISTICS

Over the operating range (3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power-Supply Current	I_{CC1}		15	30	mA	1, 2
CMOS Standby Current ($\overline{CS}$ = V_{CC} - 0.2V)	I_{CC2}		0.5	2	mA	1, 2
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	5
Output Logic 1 Voltage at -0.4mA	V_{OH}	2.4			V	
Output Logic 0 Voltage at +0.8mA	V_{OL}			0.4	V	
Power-Fail Trip Point	V_{PF}	2.5	2.6	2.7	V	3
Battery Leakage OSC ON	I_{BAT1}		0.50	0.7	µA	11
Battery Leakage OSC OFF	I_{BAT2}		0.050	0.4	µA	11
I/O Leakage	I_{LO}	-1		+1	µA	4
$\overline{PWR}$ Output at 0.4V	I_{OLPWR}			4	mA	
$\overline{IRQ}$ Output at 0.4V	I_{OLIRQ}			0.8	mA	

CRYSTAL SPECIFICATIONS*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Frequency	F_O		32.768		kHz	
Series Resistance	ESR			45	kΩ	
Load Capacitance	C_L		6 or 12.5		pF	

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58*, "Crystal Considerations for Dallas Real-Time Clocks" for additional specification.*

RTC AC TIMING CHARACTERISTICS

Over the operating range (3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	360		DC	ns	
Pulse-Width, $\overline{RD}$ / $\overline{WR}$ Low	PW_{RWL}	200			ns	
Pulse-Width, $\overline{RD}$ / $\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall	t_R, t_F			30	ns	
Chip-Select Setup Time Before $\overline{WR}$ or $\overline{RD}$	t_{CS}	20			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		90	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	40			ns	
Muxed Address Hold Time to ALE Fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	30			ns	
Pulse-Width ALE High	PW_{ASH}	40			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	30			ns	
Output Data-Delay Time from $\overline{RD}$	t_{DDR}	20		200	ns	6
Data Setup Time	t_{DSW}	70			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

AC TEST CONDITIONS

Output Load: 50pF
Input Pulse Levels: 0V to 3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

RTC AC TIMING CHARACTERISTICS

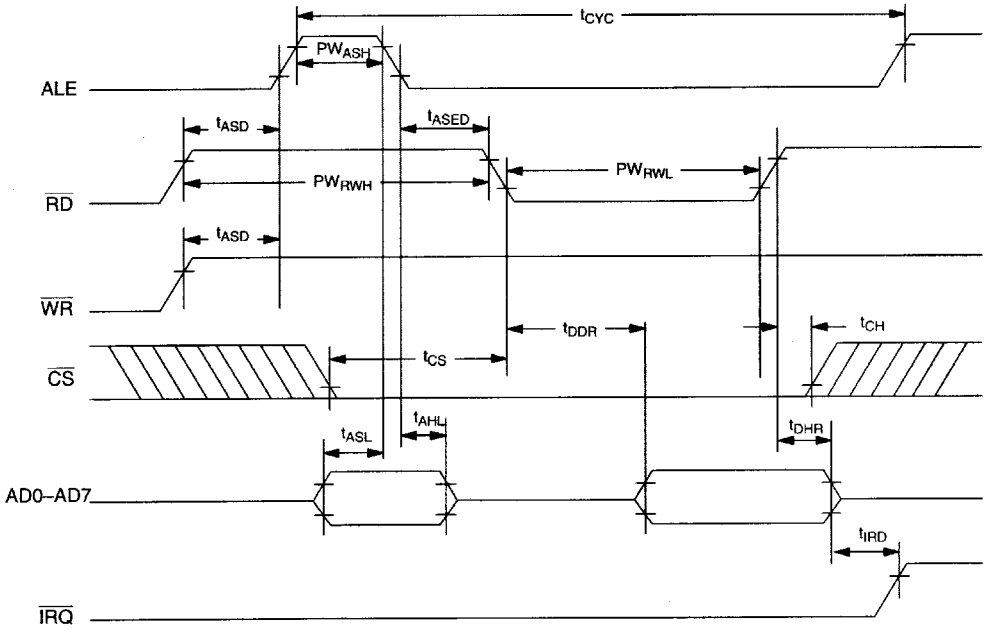
Over the operating range (5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	240		DC	ns	
Pulse-Width, $\overline{RD}$ / $\overline{WR}$ Low	PW_{RWL}	120			ns	
Pulse-Width, $\overline{RD}$ / $\overline{WR}$ High	PW_{RWH}	80			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip-Select Setup Time before $\overline{WR}$ or $\overline{RD}$	t_{CS}	20			ns	
Chip-Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	20			ns	
Muxed Address Hold Time to ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse-Width ALE High	PW_{ASH}	40			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	30			ns	
Output Data-Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	30			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

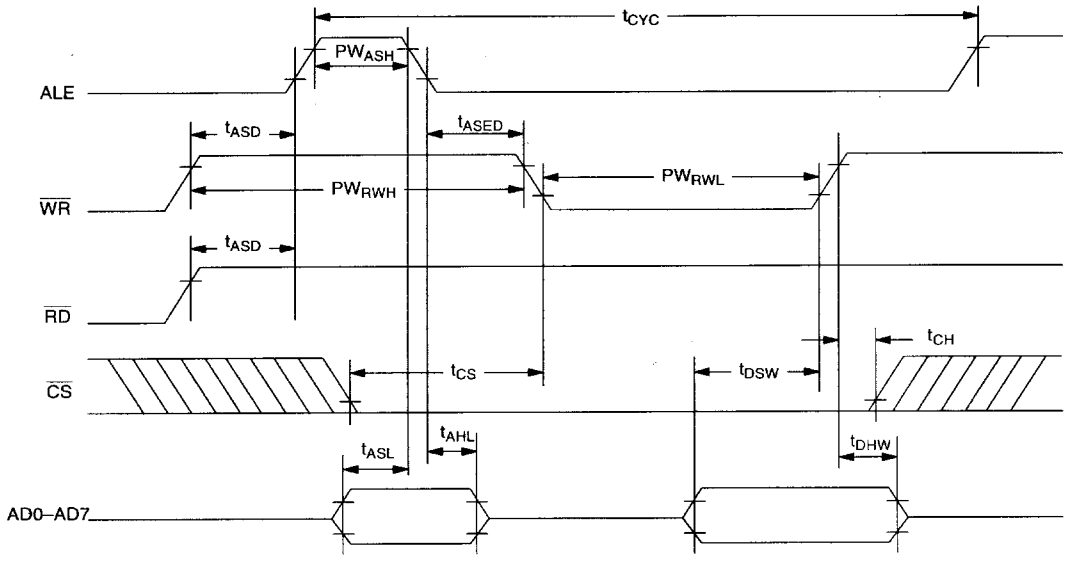
AC TEST CONDITIONS

Output Load: 50pF
Input Pulse Levels: 0V to 3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

BUS TIMING FOR READ CYCLE TO RTC AND RTC REGISTERS



BUS TIMING FOR WRITE CYCLE TO RTC AND RTC REGISTERS



POWER-UP/POWER-DOWN TIMING, 5V

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power-Fail	t_{PF}			0	ns	
Recovery at Power-Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power-Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power-Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power-Up	t_R $4.5 \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	9, 10

POWER-UP/POWER-DOWN TIMING, 3V

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ High to Power-Fail	t_{PF}			0	ns	
Recovery at Power-Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power-Down	t_F $2.5 \le V_{CC} \le 3.0V$	300			µs	
V_{CC} Slew Rate Power-Up	t_R $3.0 \ge V_{CC} \ge 2.5V$	0			µs	
Expected Data Retention	t_{DR}	10			years	9, 10

Warning: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

(T_A = +25°C)

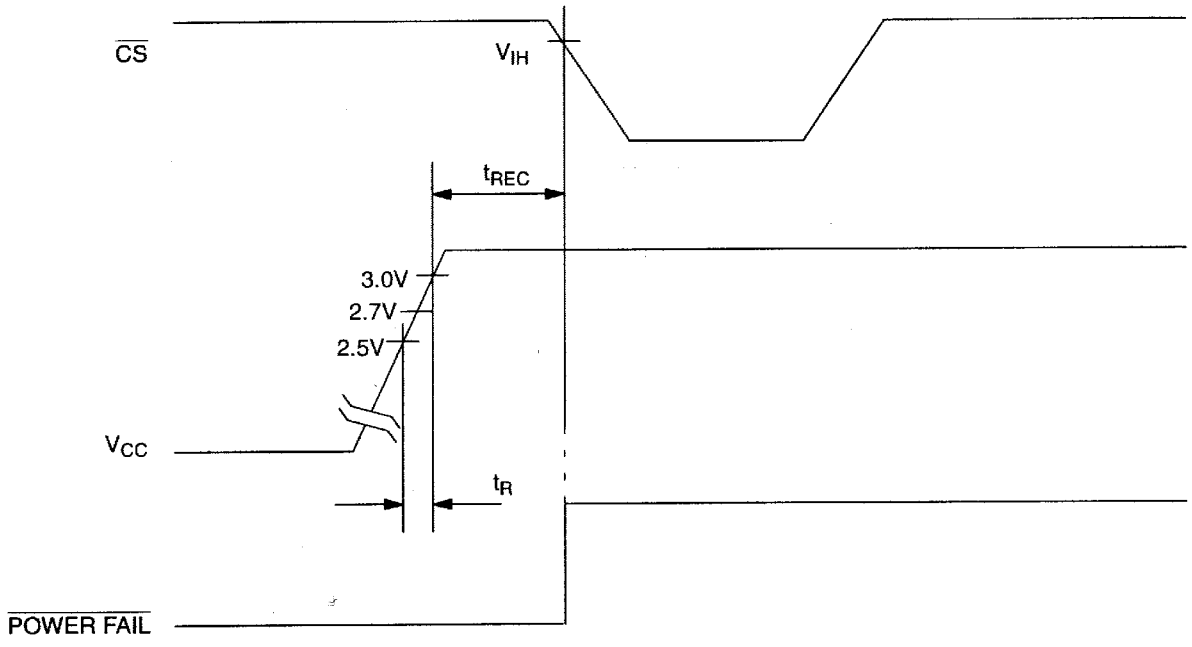
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE-UP/KICKSTART TIMING

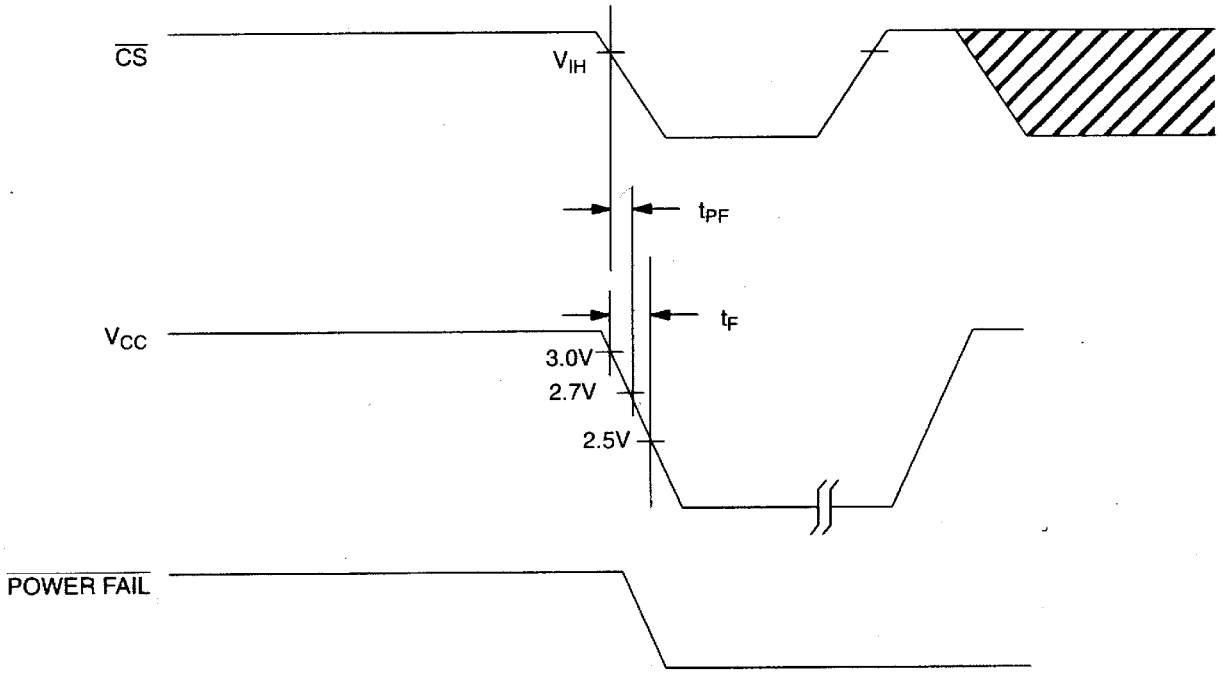
(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart-Input Pulse-Width	t_{KSPW}	2			µs	
Wake-up/Kickstart Power-On Timeout	t_{POTO}	2			s	7

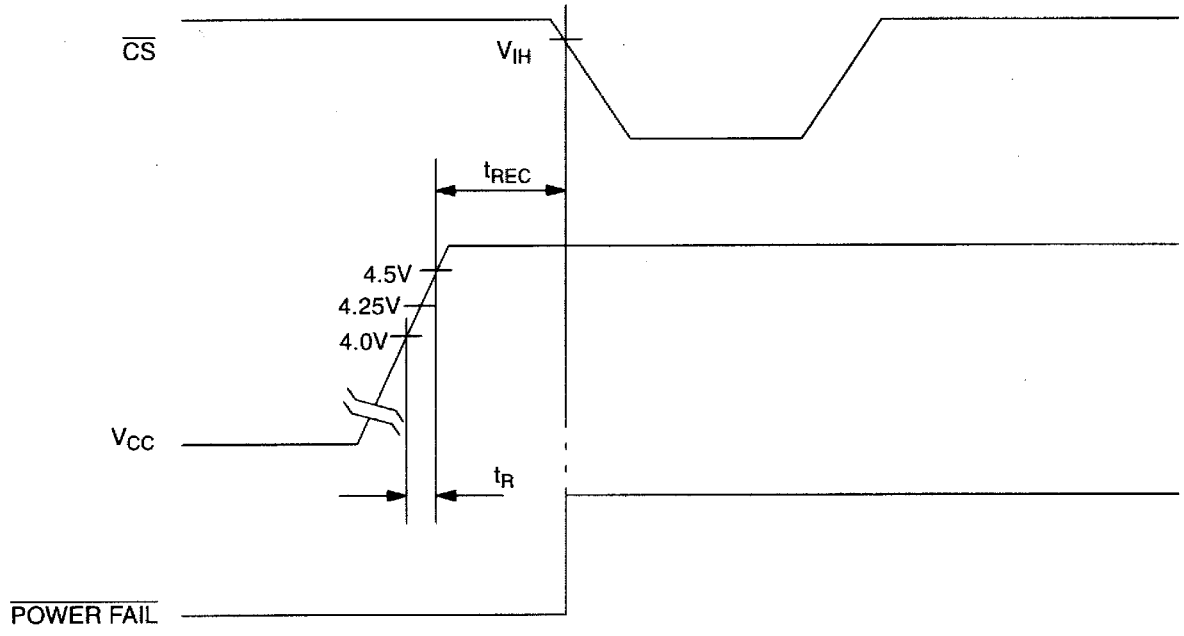
POWER-UP CONDITION, 3V



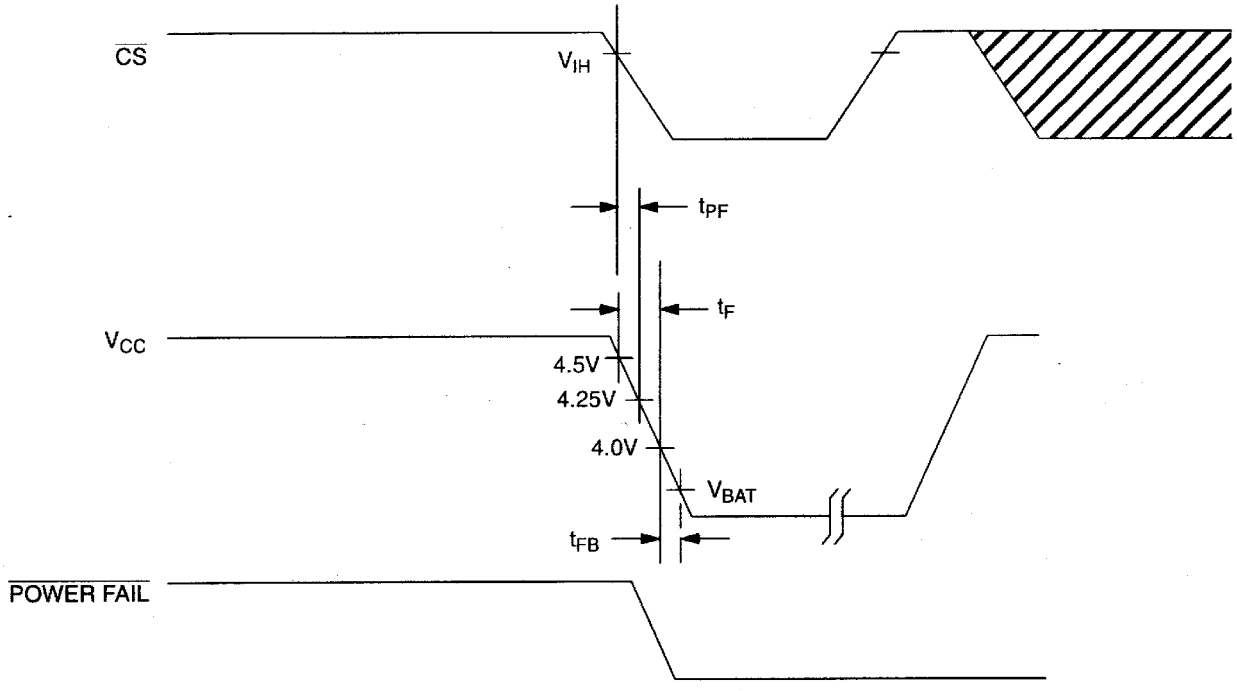
POWER-DOWN CONDITION, 3V



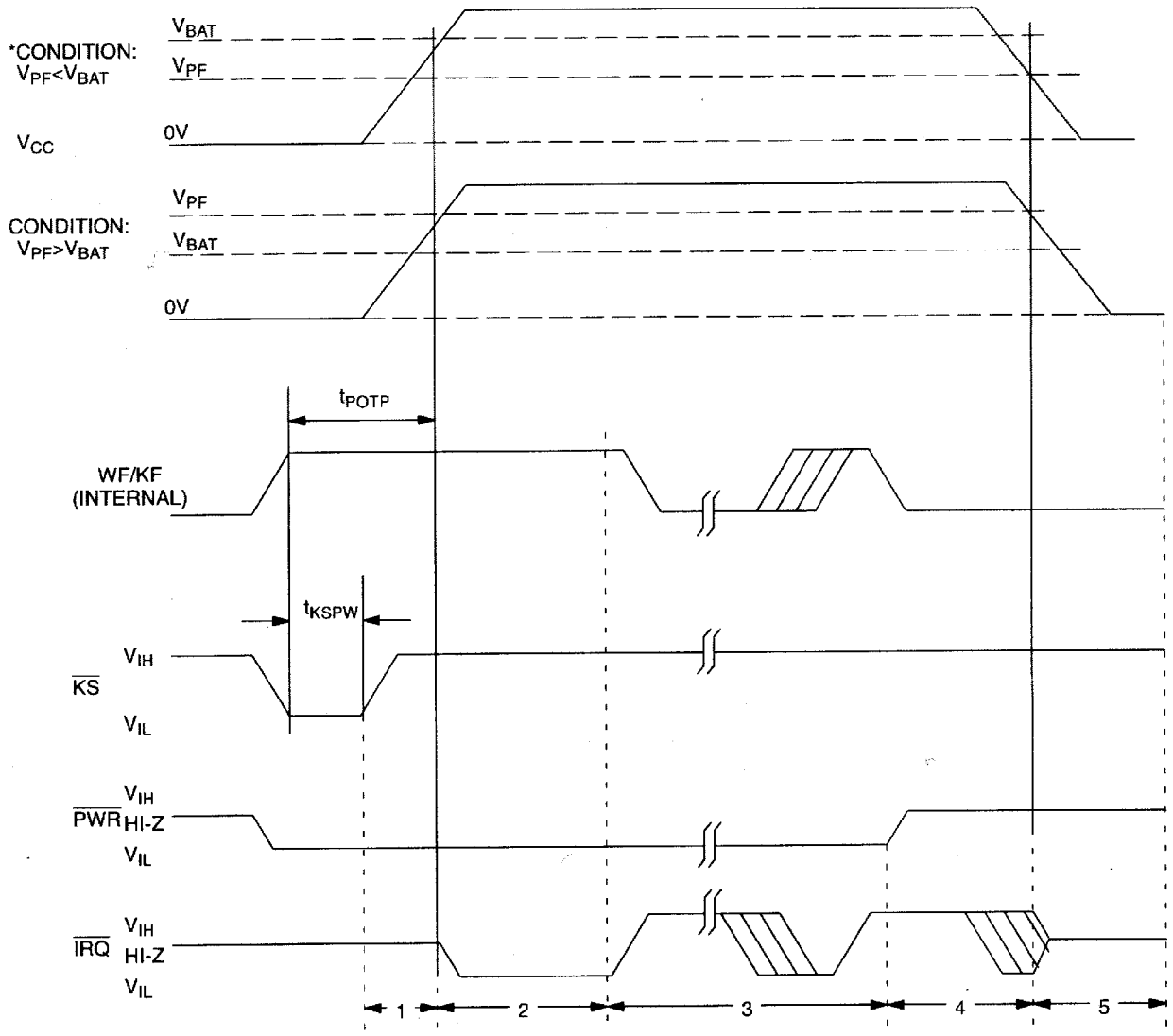
POWER-UP CONDITION, 5V



POWER-DOWN CONDITION, 5V

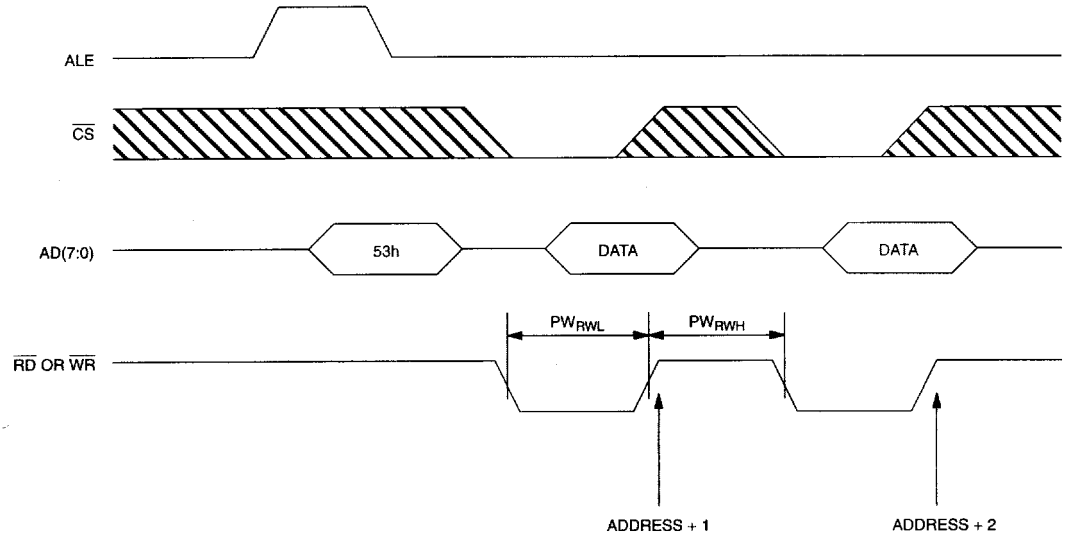


WAKE-UP/KICKSTART TIMING



Note: Time intervals shown above are referenced in *Wake-Up/Kickstart* section.
*This condition can occur with the 3V device.

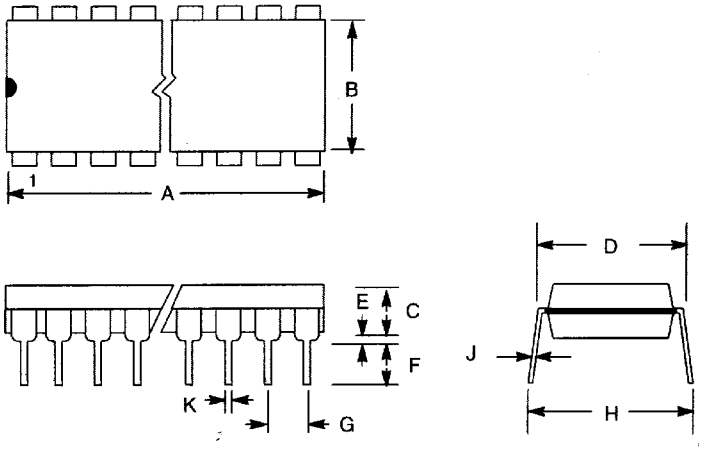
BURST MODE TIMING WAVEFORM



NOTES:

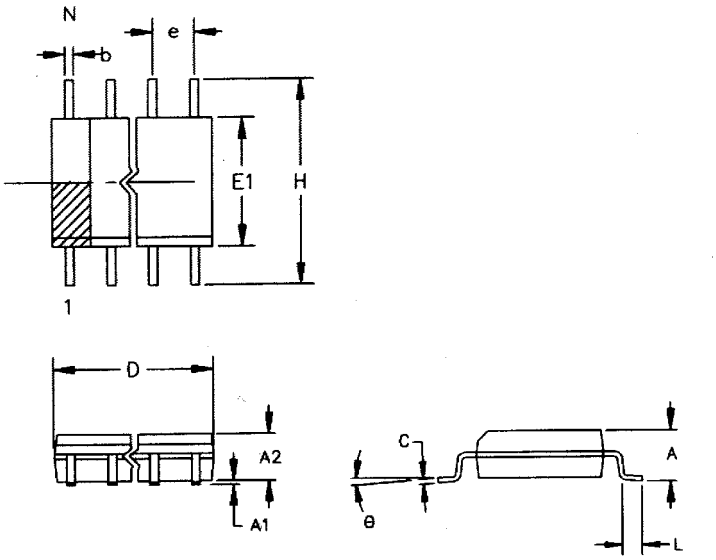
1) Typical values are at +25°C and nominal supplies.
2) Outputs are open.
3) Write-protection trip point occurs during power-fail prior to switchover from V_{CC} to V_{BAT}.
4) Applies to the AD0 to AD7 pins, and the SQW pin when each is in a high-impedance state.
5) The IRQ and PWR pins are open-drain.
6) Measured with a load of 50pF + 1 TTL gate.
7) Wake-up kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
8) V_{SW} is determined by the larger of V_{BAT} and V_{BAUX}.
9) The DS17487 keeps time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
10) t_{DR} is the amount of time that the internal battery can power the internal oscillator and internal registers of the DS17487.
11) I_{BAT1} and I_{BAT2} are measured at V_{BAT} = 3.5V.
12) RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used.

DS17485 24-PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN	1.245	1.270
MM	31.62	32.25
B IN	0.530	0.550
MM	13.46	13.97
C IN	0.140	0.160
MM	3.56	4.06
D IN	0.600	0.625
MM	15.24	15.88
E IN	0.015	0.050
MM	0.380	1.27
F IN	0.120	0.145
MM	3.05	3.68
G IN	0.090	0.110
MM	2.29	2.79
H IN	0.625	0.675
MM	15.88	17.15
J IN	0.008	0.012
MM	0.20	0.30
K IN	0.015	0.022
MM	0.38	0.56

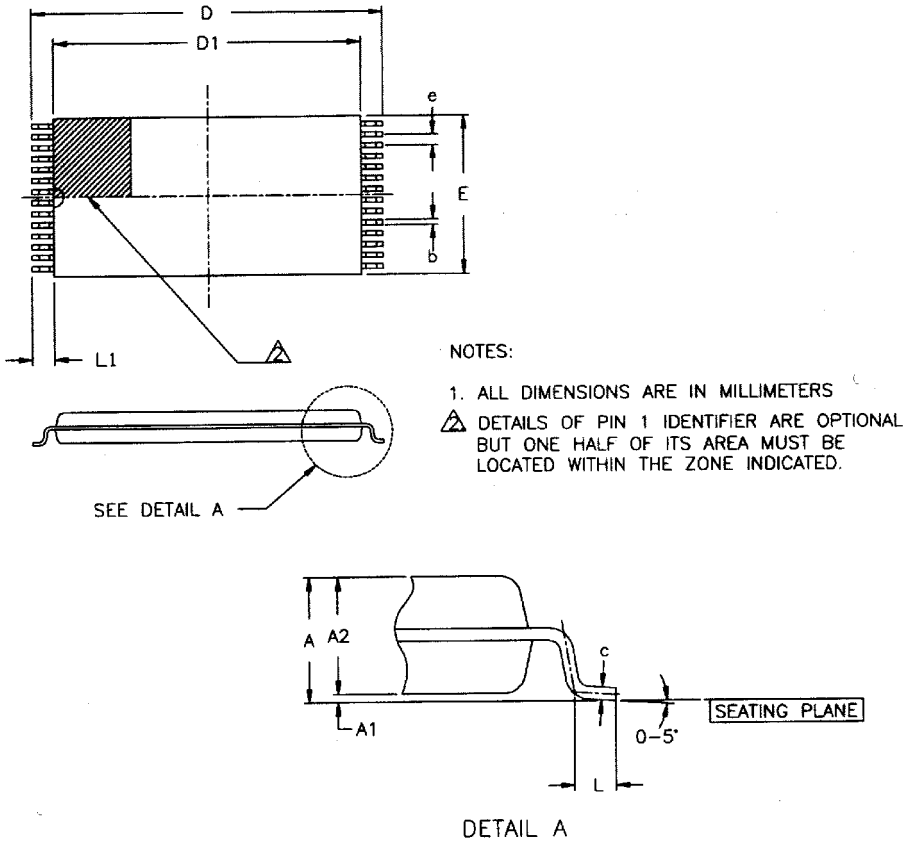
DS17485 24-PIN SO



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that one-half or more of its area is contained in the hatched zone.

PKG	24-PIN	
DIM	MIN	MAX
A IN	0.094	0.105
MM	2.38	2.68
A1 IN	0.004	0.012
MM	0.102	0.30
A2 IN	0.089	0.095
MM	2.26	2.41
b IN	0.013	0.020
MM	0.33	0.51
C IN	0.009	0.013
MM	0.229	0.33
D IN	0.598	0.612
MM	15.19	15.54
e IN	0.050 BSC	
MM	1.27 BSC	
E1 IN	0.290	0.300
MM	7.37	7.62
H IN	0.398	0.416
MM	10.11	10.57
L IN	0.016	0.040
MM	0.40	1.02
Θ	0°	8°

DS17485 28-PIN TSOP



PKG	28-PIN	
DIM	MIN	MAX
A	—	1.20
A1	0.05	—
A2	0.91	1.02
b	0.18	0.27
c	0.15	0.20
D	13.20	13.60
D1	11.70	11.90
E	7.90	8.10
e	0.55 BSC	
L	0.30	0.70
L1	0.80 BSC	

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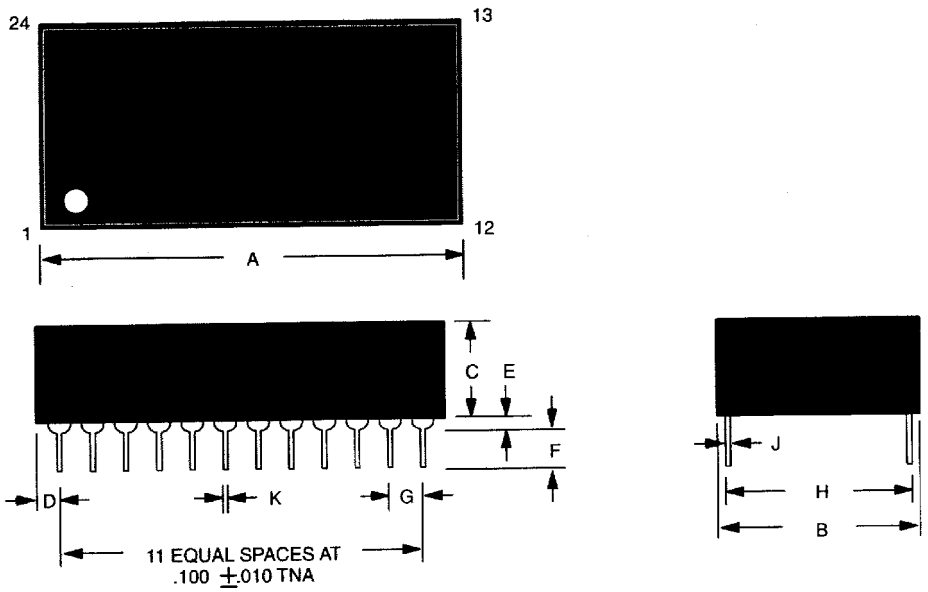
DS17487 RTC PLUS RAM



Note: Pins 2, 3, 16, and 20 are missing by design.

PKG	24-PIN	
DIM	MIN	MAX
A IN	1.320	1.335
MM	33.53	33.91
B IN	0.720	0.740
MM	18.29	18.80
C IN	0.345	0.370
MM	8.76	9.40
D IN	0.100	0.130
MM	2.54	3.30
E IN	0.015	0.030
MM	0.38	0.76
F IN	0.100	0.140
MM	2.79	3.56
G IN	0.090	0.110
MM	2.29	2.79
H IN	0.590	0.630
MM	14.99	16.00
J IN	0.008	0.012
MM	0.20	0.30
K IN	0.015	0.021
MM	0.38	0.53