150-mA Low Noise, Low Dropout Regulator

APPLICATIONS

- Cellular Phones, Wireless Handsets
- PDAs
- MP3 Players
- Digital Cameras
- Pagers
- Wireless Modem
- Noise-Sensitive Electronic Systems

DESCRIPTION

The SiP21106 BiCMOS 150 mA low noise LDO voltage regulators are the perfect choice for low battery operated low powered applications. An Ultra low ground current and low dropout voltage of 135 mV at 150 mA load helps to extend battery life for portable electronics. Systems requiring a quiet voltage source, such as RF applications, will benefit from the SiP21106 low output noise.

The SiP21107 do not require a noise bypass cpacitor and provides an error flag pin (POK or Power OK). POK output requires an external pull-up resistor and goes low when the supply has not come up to voltage.

The SiP21108 output is adjusted with an external resistor network.

The SiP21106/7/8 regulators allow stable operation with very small ceramic output capacitors, reducing board space and component cost. They are designed to maintain regulation while delivering 330 mA peak current upon turn-on. During start-up, an active pull-down circuit improves the output transient response and regulation. In shutdown mode, the output automatically discharges to ground through a 100 Ω NMOS.

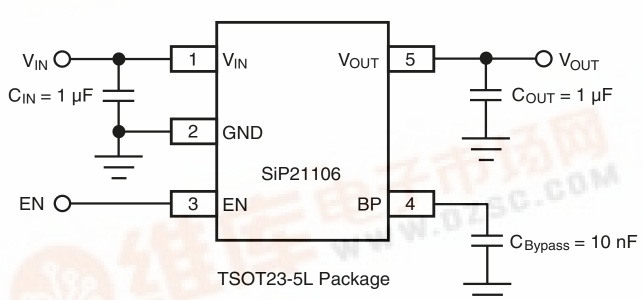
The SiP21106/7/8 are available in TSOT23-5L and a super thin lead (Pb)-free TSC75-6L packages for operation over the industrial operation range (- 40 °C to 85 °C).

FEATURES

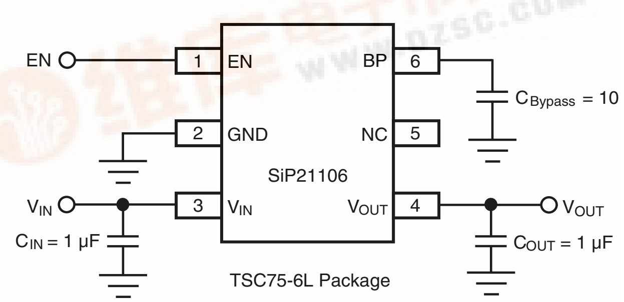
- TSC75-6L Package (1.6 x 1.6 x 0.6 mm), and TSOT23-5L Package Options
- 1.0 % Output Voltage Accuracy at 25 °C
- Low Dropout Voltage: 135 mV at 150 mA
- SiP21106 Low Noise: 60 µV$_{(rms)}$ (10 Hz to 100 kHz Bandwidth) With 10 nF Over Full Load Range
- 35 µA (typical) Ground Current at 1 mA Load
- 1 µA Maximum Shutdown Current at 85 °C
- Output Auto Discharge at Shutdown Mode
- Built-in Short Circuit (330 mA typical) and Thermal Protection (160 °C typical)
- SiP21108 Adjustable Output Voltage
- SiP21107 POK Error Flag
- - 40 °C to + 125 °C Junction Temperature Range for Operation
- Uses Low ESR Ceramic Capacitors
- Fixed Voltage Output 1.3 V to 5 V in 50 mV Steps

Pb-free
RoHS COMPLIANT

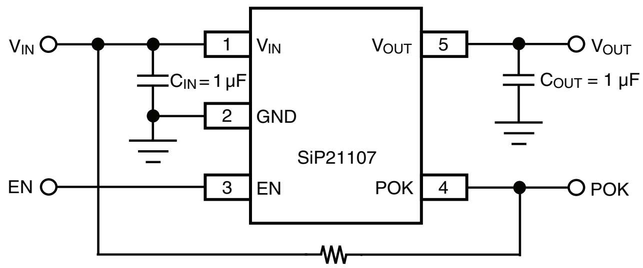
TYPICAL APPLICATION CIRCUIT



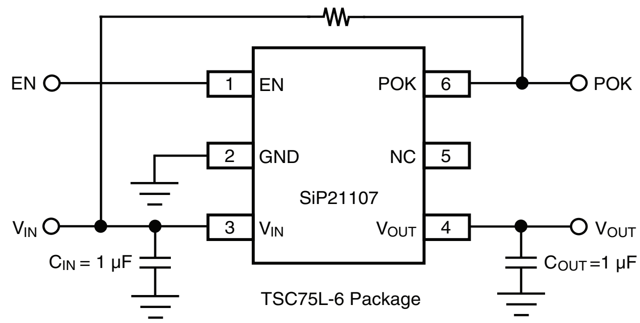
TSOT23-5L Package



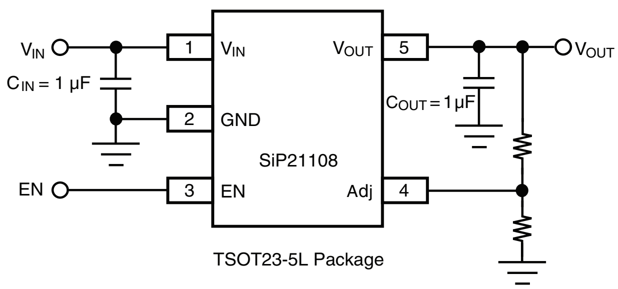
TSC75-6L Package



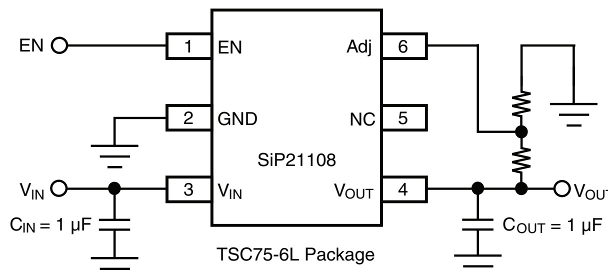
TSOT23-5L Package



TSC75L-6 Package



TSOT23-5L Package



TSC75-6L Package

ABSOLUTE MAXIMUM RATINGS			
Parameter	**Limit**		**Unit**
Input Voltage, V_{IN} to GND	- 0.3 to 6		V
V_{EN} (See Detailed Description)	- 0.3 to 6		
Output Current (I_{OUT})	Short Circuit Protected		
Output Voltage (V_{OUT})	- 0.3 to V_{IN} + 0.3		V
	TSC75-6L	TSOT23-5L	
Package Power Dissipation (P_D)[a]	420	440	mW
Package Thermal Resistance (θ_{JA})[b]	131	180	°C/W
Maximum Junction Temperature, $T_{J(max)}$	125		°C
Storage Temperature, T_{STG}	- 65 to 150		
Lead Temperature, T_L[c]	260		

Notes:
a. Derate 7.6 mW/°C for TSC75-6L package and 5.5 mW/°C for TSOT23-5L package above T_A = 70 °C.
b. Device mounted with all leads soldered or welded to PC board.
c. Soldering for 5 sec.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE		
Parameter	**Limit**	**Unit**
Input Voltage, V_{IN}	2.2 to 5.5	V
Operating Ambient Temperature T_A	- 40 to 85	°C

SPECIFICATIONS							
Parameter	**Symbol**	**Test Conditions Unless Specified** $V_{IN} = V_{OUT(nom)} + 1.0\ V = V_{EN}$ $I_{OUT} = 1$ mA, $C_{IN} = 1\ \mu F$, $C_{OUT} = 1\ \mu F$ - 40 °C < T_A < 85 °C for full	**Temp**[a]	**Min**[b]	**Typ**[c]	**Max**[b]	**Unit**
Input Voltage Range	V_{IN}		Full	2.2		5.5	V
Output Voltage Accuracy	V_{OUT}	$I_{OUT} = 1$ mA	Room	- 1.0		1.0	%
			Full	- 2.5		2.5	
Line Regulation		All others	Full	- 0.2	0.006	0.2	%/V
		For 4.6 V to 5.0 V		- 0.4		0.4	
Dropout Voltage[d] (2.2 V ≤ $V_{OUT(nom)}$ < 2.6 V)	V_{DO}	$I_{OUT} = 50$ mA	Room		45		mV
			Full		55		
		$I_{OUT} = 100$ mA	Room		90		
			Full		106		
		$I_{OUT} = 150$ mA	Room		135	250	
			Full		160	300	
Dropout Voltage ($V_{OUT(nom)}$ ≥ 2.6 V)	V_{DO}	$I_{OUT} = 50$ mA	Room		45		mV
			Full		55		
		$I_{OUT} = 100$ mA	Room		90		
			Full		106		
		$I_{OUT} = 150$ mA	Room		135	180	
			Full		160	220	
Ground Pin Current[e]	I_{GND}	$I_{OUT} = 1$ mA	Room		35	75	µA
			Full			85	
		$I_{OUT} = 150$ mA	Room		39	75	
			Full			85	
Output Noise Voltage[f] (RMS)	e_N	SiP21106 $V_{OUT(nom)} = 2.8$ V, BW = 10 Hz to 100 kHz, 1 mA < I_{OUT} < 150 mA, $C_{BP} = 0.01\ \mu F$	Room		60		µV
		SiP21107/8 $V_{OUT(nom)} = 2.8$ V, BW = 10 Hz to 100 kHz, 1 mA < I_{OUT} < 150 mA	Room		350		µV
Ripple Rejection	PSRR	$I_{OUT} = 150$ mA, f = 1 kHz	Room		70		dB
		$I_{OUT} = 150$ mA, f = 10 kHz	Room		55		
		$I_{OUT} = 150$ mA, f = 100 kHz	Room		25		
Load Regulation	LDR	V_{OUT} ≥ 2.6 V, I_{OUT} : 1 mA to 150 mA	Room		0.003	0.006	%/mA
		V_{OUT} < 2.6 V, I_{OUT} : 1 mA to 150 mA	Room		0.005	0.009	
Auto Discharge Resistance	R_{DIS}	$V_{OUT} = 2$ V	Room		100		Ω
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$		Room		160		°C
Thermal Hysteresis	T_{HYST}		Room		20		
Output Current Limit	I_{O_LIMIT}	$V_{OUT} = 0$ V	Room	170	330	600	mA
Shutdown Supply Current	$I_{CC(off)}$	$V_{EN} = 0$ V	Full		0.02	1	µA
EN Pin Input Voltage	V_{ENH}	High = Regulator ON (Rising)	Full	1.2		5.5	V
	V_{ENL}	Low = Regulator OFF (Falling)	Full			0.4	
EN Pin Input Current	I_{EN}		Room		0.009		µA
Output Voltage Turn-On Time	t_{on}	EN to V_{OUT} delay; I_{OUT} = 1 mA			70		µs

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified $V_{IN} = V_{OUT(nom)} + 1.0$ V $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF - 40 °C < T_A < 85 °C for full	Temp[a]	Min[b]	Typ[c]	Max[b]	Unit
Adjustable Voltage Section (SiP21108 Version only)							
Feedback Voltage	V_{Adj}		Room	1.188	1.2	1.212	V
			Full	1.170		1.230	
Error Flag Section (SiP21107 Version only)							
POK(OFF) Leakage	I_{OFF}	R_{PU} to V_{OUT} or V_{IN}	Full			1	µA
POK(ON) Voltage	V_{POKL}	$I_{SINK} = 0.5$ mA	Full			0.4	V
POK Threshold[g]	V_{POKLH}	V_{IN} rising, $I_{OUT} = 1$ mA, POK goes high	Full	90		96	%
POK Hysteresis	V_{HYST}	V_{IN} falling, $I_{OUT} = 1$ mA, POK goes low	Room		1.5		

Notes:
a. Room = 25 °C, Full = - 40 to 85 °C. Derate 7.6 mW/°C for TSC75 and 5.5 mW/°C for SOT23 above $T_A = 70$ °C
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Dropout voltage is defined as the input-to-output differential voltage at which the output voltage drops 2 % below its nominal value with constant load. For outputs = 2.2 V, dropout voltage is not applicable due to 2.2 V minimum input voltage requirement.
e. Ground current is specified for normal operation as well as “drop-out” operation.
f. Output noise is proportional to output voltage. Use formula $e_N = 60$ µV(rms)*V_{OUT}/2.8 V.
g. POK threshold percentage is calculated by V_{IN}/V_{OUT} x 100 %.

TIMING WAVEFORMS

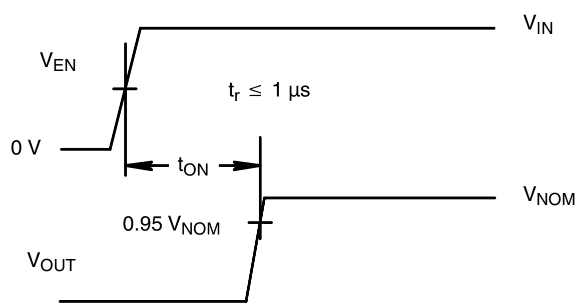
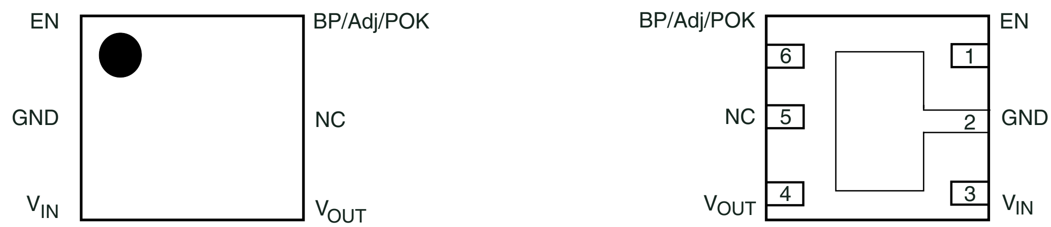
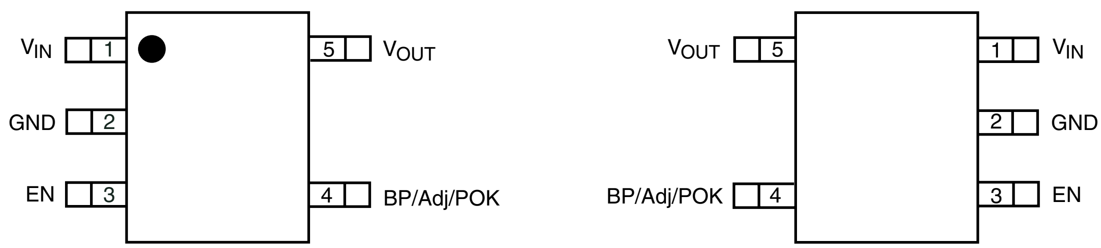


Figure 1.

PIN CONFIGURATION



TOP VIEW TSC75-6L PACKAGE (1.6 x 1.6 x 0.6 mm) BOTTOM VIEW



TOP VIEW BOTTOM VIEW

TSOT23-5L Package

Figure 2.

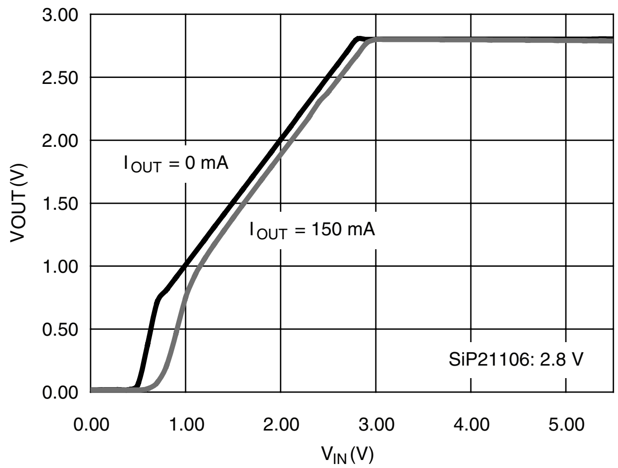
PIN DESCRIPTION			
Pin Number TSC75-6L	**Pin Number TSOT23-5L**	**Name**	**Function**
1	3	EN	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused. Do not leave floating.
2	2	GND	Ground pin. For better thermal capability, directly connected to large ground plane.
3	1	V_{IN}	Input supply pin. Bypass this pin with a 1 µF ceramic or tantalum capacitor to ground.
4	5	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.
5	-	NC	No Connection.
6	4	BP/Adj/POK	- BP (SiP21106): Noise bypass pin. For low noise applications, a 10 nF ceramic capacitor should be connected from this pin to ground. - Adj (SiP21108): Adjust input pin. Connect feedback resistors to program the output voltage for trim value of 1.2005 V. - POK (SiP21107): Power OK (Error Flag) pin. Open-drain output, which requires connecting a pull-up resistor to V_{IN} or V_{OUT}. POK pin is actively high to indicate an output normal operation condition on regulator and goes low to indicate under-voltage fault condition.

ORDERING INFORMATION

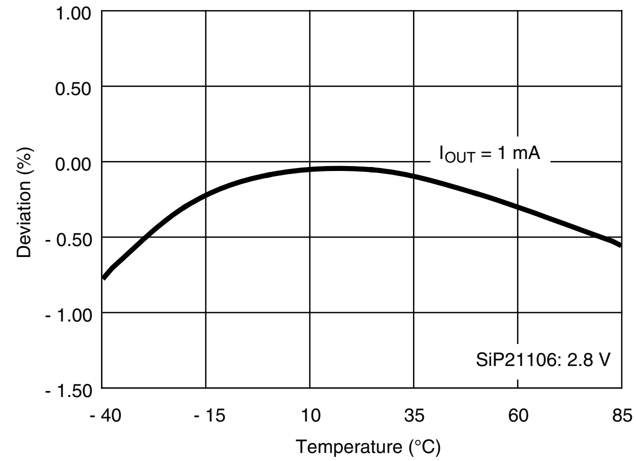
Part Number	Marking	Voltage	Temperature Range	Package
SiP21108DVP-T1-E3	AA	Adjustable	- 40 °C to 85 °C	TSC75-6L
SiP21106DVP-18-E3	BG	1.8		
SiP21106DVP-25-E3	BP	2.5		
SiP21106DVP-26-E3	BR	2.6		
SiP21106DVP-28-E3	BT	2.8		
SiP21106DVP-30-E3	BV	3.0		
SiP21106DVP-33-E3	BY	3.3		
SiP21106DVP-46-E3	CM	4.6		
SiP21106DVP-285-E3	CT	2.85		
SiP21107DVP-18-E3	DG	1.8		
SiP21107DVP-25-E3	DP	2.5		
SiP21107DVP-26-E3	DR	2.6		
SiP21107DVP-28-E3	DT	2.8		
SiP21107DVP-30-E3	DV	3.0		
SiP21107DVP-33-E3	DY	3.3		
SiP21107DVP-46-E3	EM	4.6		
SiP21107DVP-285-E3	ET	2.85		
SiP21108DT-T1-E3	N9	Adjustable	- 40 °C to 85 °C	TSOT23-5L
SiP21106DT-18-E3	N1	1.8		
SiP21106DT-25-E3	NA	2.5		
SiP21106DT-26-E3	NC	2.6		
SiP21106DT-28-E3	N2	2.8		
SiP21106DT-285-E3	NE	2.85		
SiP21106DT-30-E3	NG	3.0		
SiP21106DT-33-E3	N3	3.3		
SiP21106DT-46-E3	N4	4.6		
SiP21107DT-18-E3	N5	1.8		
SiP21107DT-25-E3	NB	2.5		
SiP21107DT-26-E3	ND	2.6		
SiP21107DT-28-E3	N6	2.8		
SiP21107DT-285-E3	NF	2.85		
SiP21107DT-30-E3	NH	3.0		
SiP21107DT-33-E3	N7	3.3		
SiP21107DT-46-E3	N8	4.6		

Note:
Other fixed output voltage options are available. Please contact your Vishay sales representative or distributor for details.

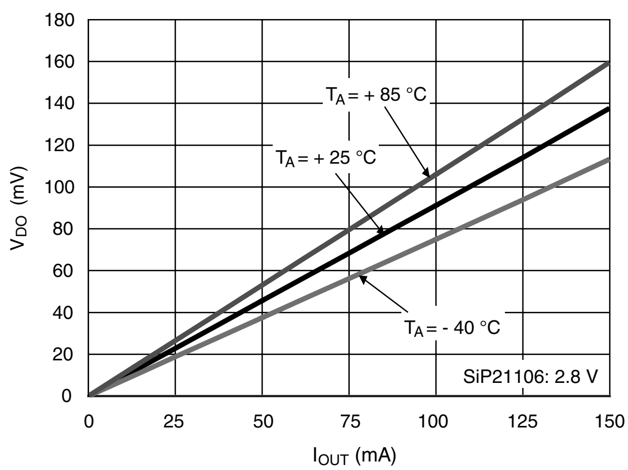
TYPICAL CHARACTERISTICS



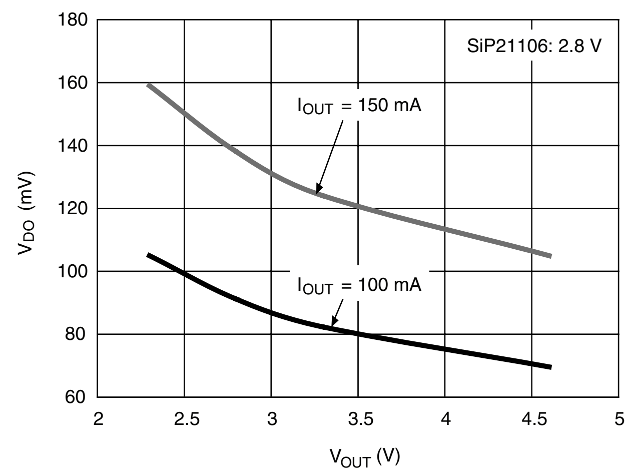
Output Voltage vs. Input Voltage



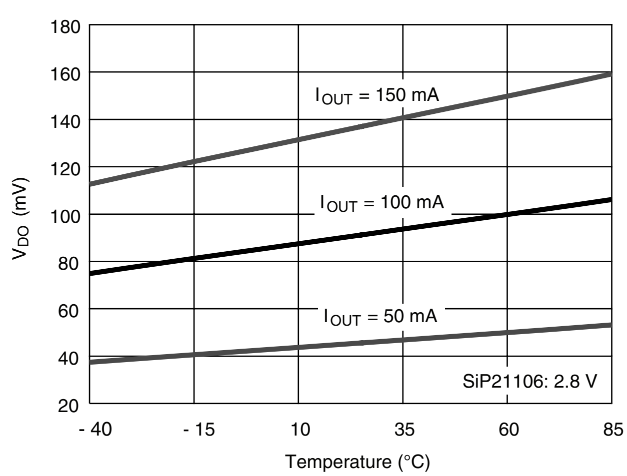
Output Voltage Accuracy vs. Temperature



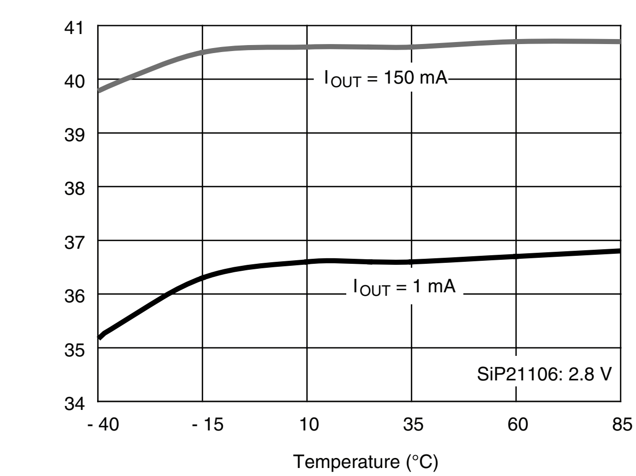
Dropout Voltage vs. Load Current



Dropout Voltage vs. Output Voltage

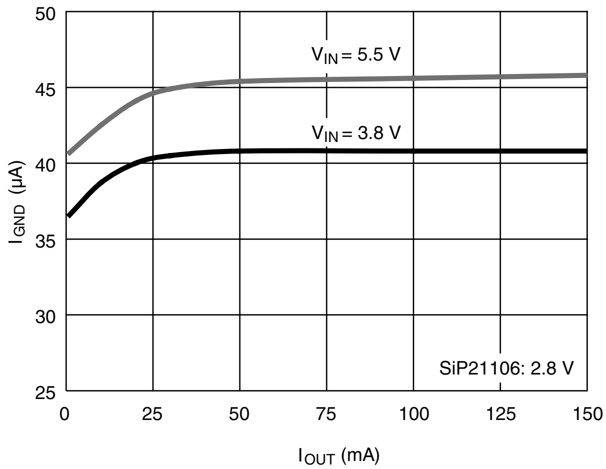


Dropout Voltage vs. Temperature

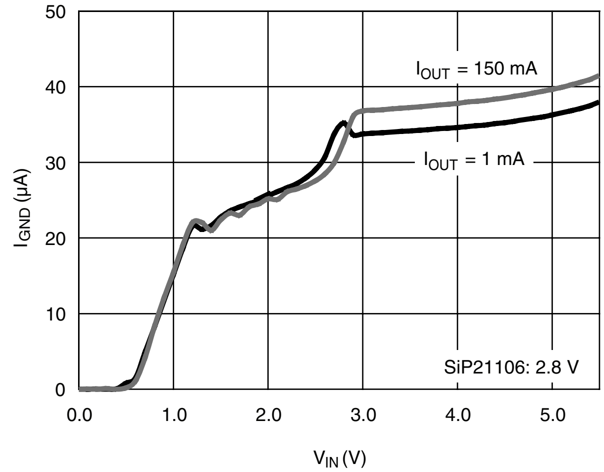


Ground Current vs. Temperature

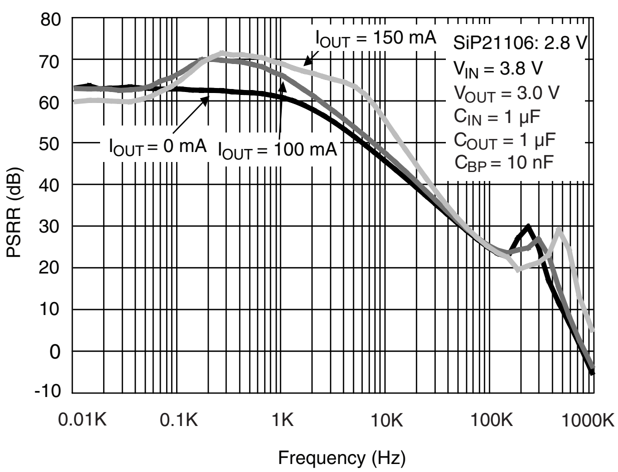
TYPICAL CHARACTERISTICS



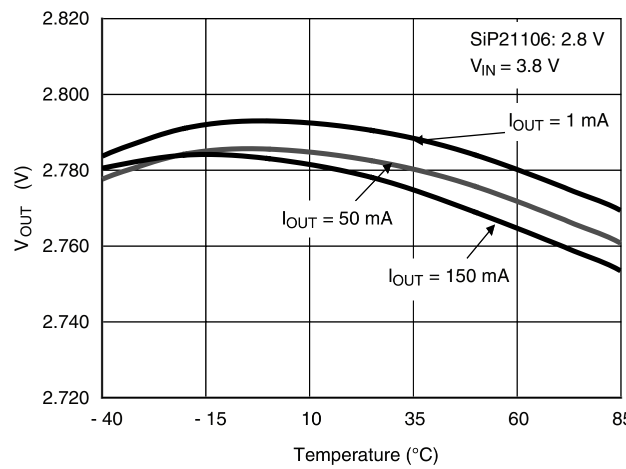
Ground Current vs. Output Current



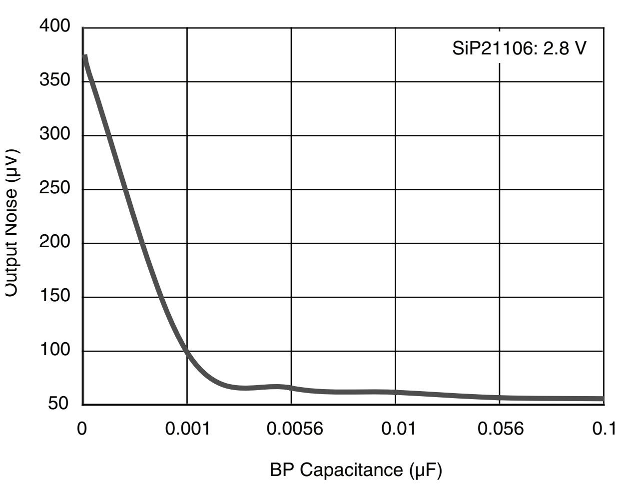
Ground Current vs. Input Voltage at 25 °C



PSRR

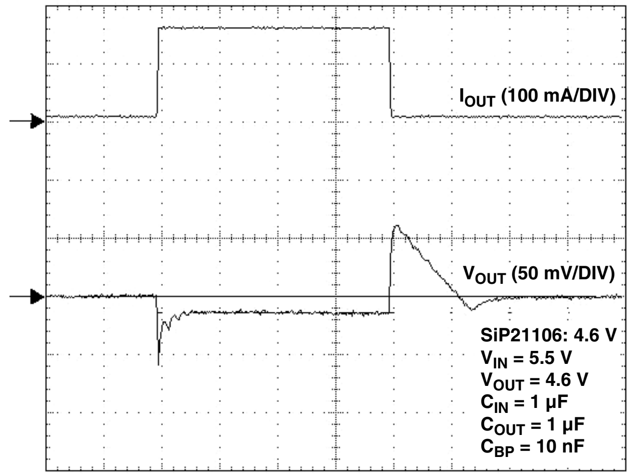


Output Voltage Accuracy vs. Load Current

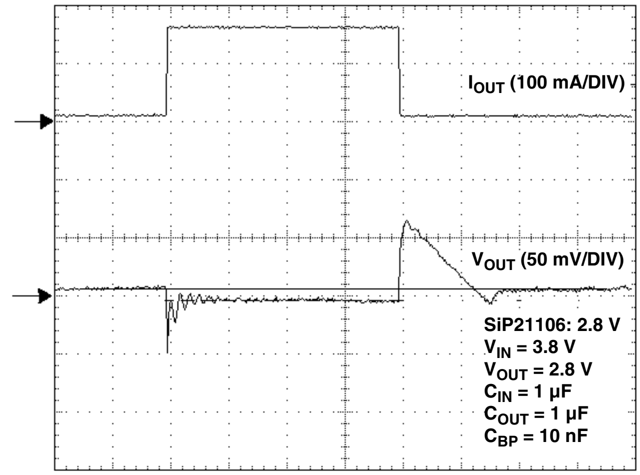


Output Noise vs. BP Capacitance

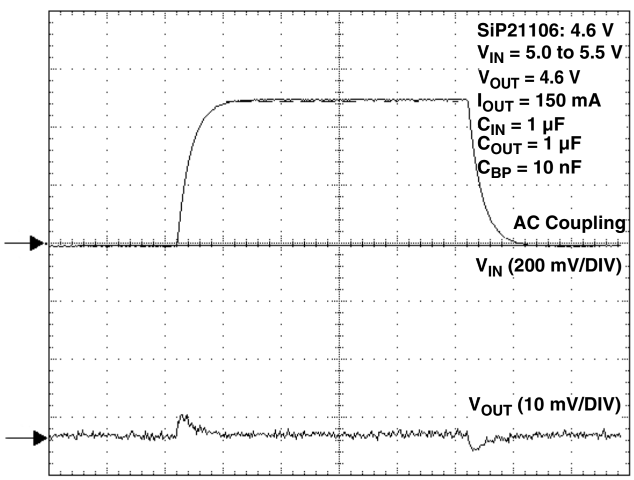
TYPICAL OPERATING WAVEFORMS



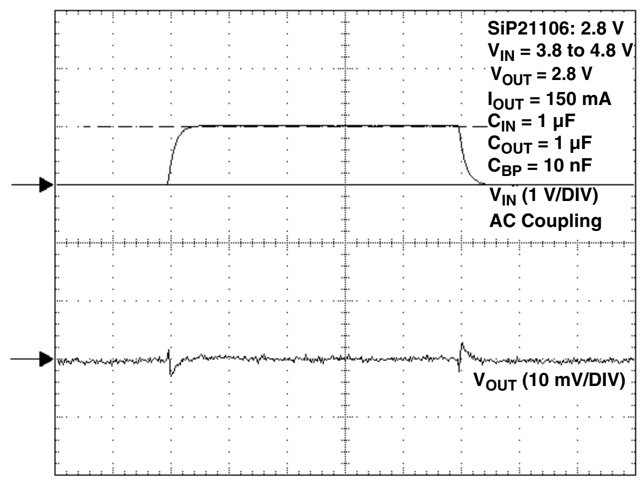
50 µS/DIV
Load Transient Response



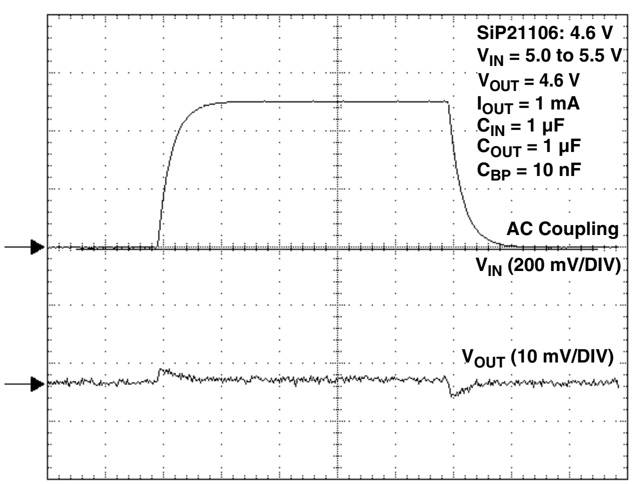
50 µS/DIV
Load Transient Response



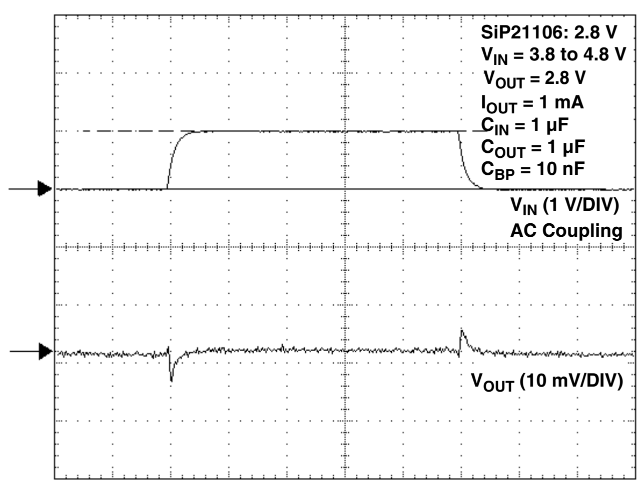
200 µS/DIV
Line Transient Response



200 µS/DIV
Line Transient Response

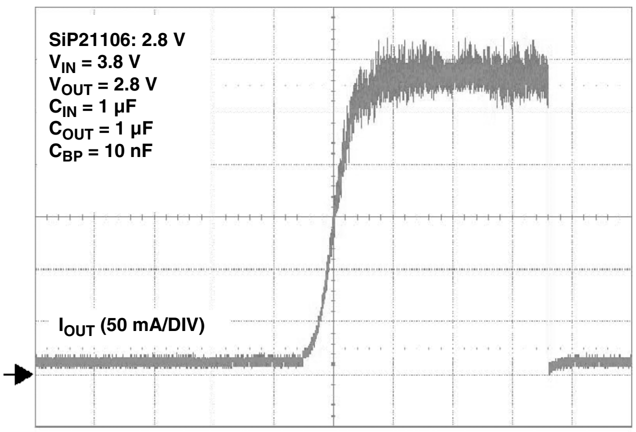


200 µS/DIV
Line Transient Response

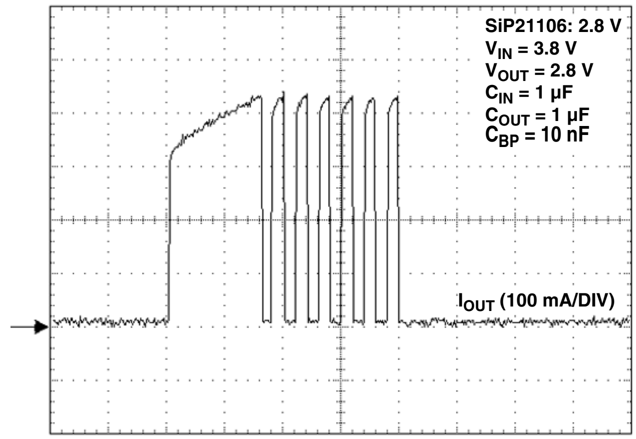


200 µS/DIV
Line Transient Response

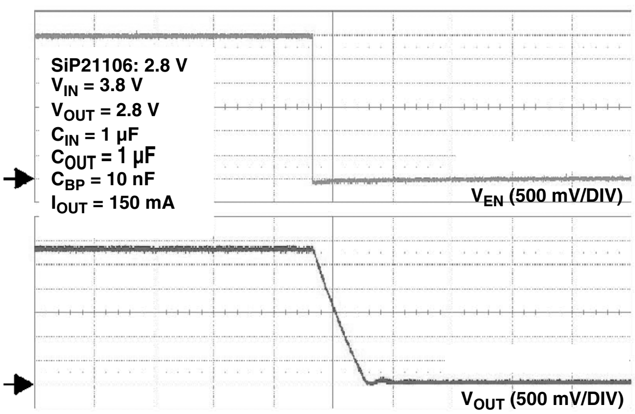
TYPICAL OPERATING WAVEFORMS



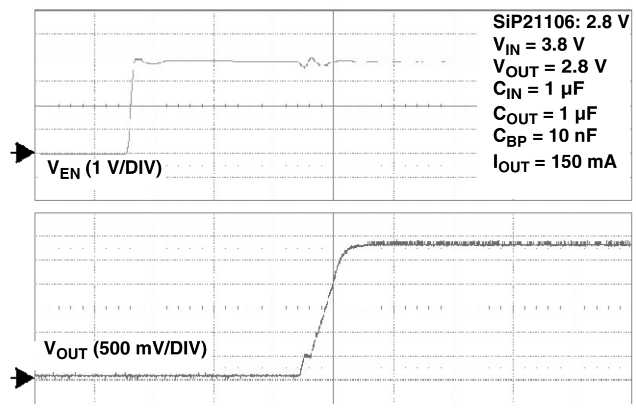
50 mS/DIV
Output Short Circuit Current



50 mS/DIV
Output Short Thermal Cycling

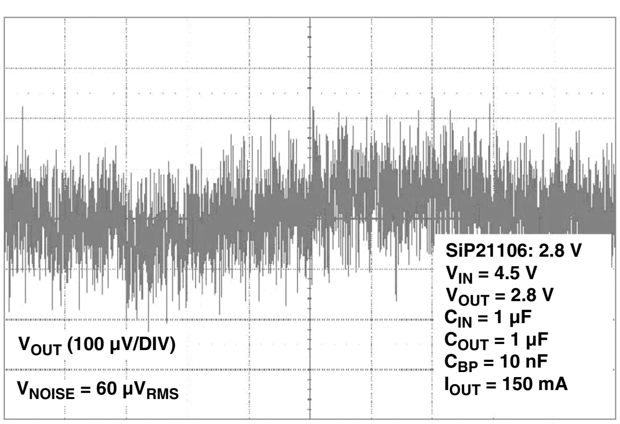


20 µS/DIV
Output Voltage Power-Down

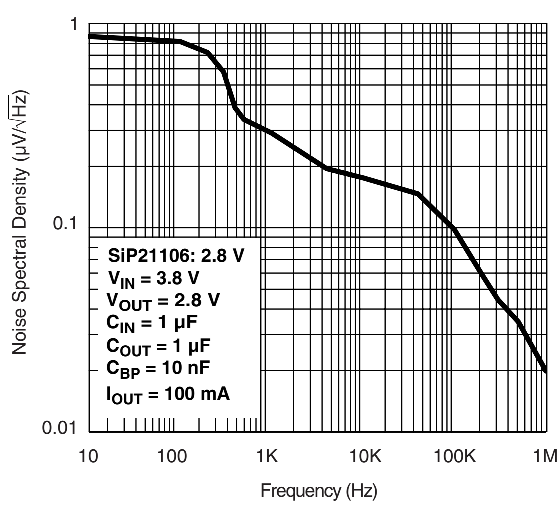


20 µS/DIV
Output Voltage Start-Up

TYPICAL WAVEFORMS



2 ms/DIV
Output Noise



Output Noise Spectral Density

FUNCTIONAL BLOCK DIAGRAM

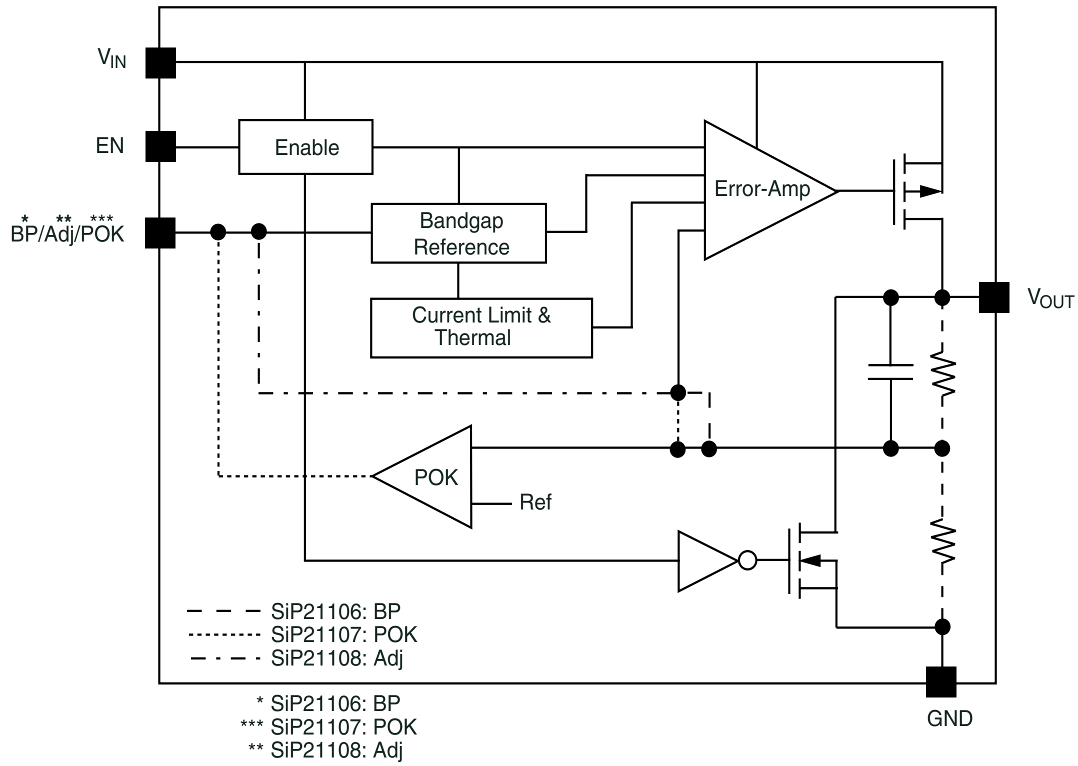


Figure 3.

DETAILED DESCRIPTION

As shown in the block diagram, the circuit consists of a bandgap reference, error amplifier, P-Channel pass transistor and an internal feedback resistor voltage divider, which is used to monitor and control the output voltage.

A constant 1.2 V bandgap reference voltage is applied to the non-inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage on its inverting input and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This increases the PMOS's gate to source voltage and allows more current to pass through the transistor to the output which increases the output voltage. Conversely, if the feedback voltage is higher than the reference voltage, the pass transistor gate is pulled high, decreasing the gate-to-source voltage, thereby allowing less current to pass to the output and causing it to drop.

Internal P-Channel Pass Transistor

A 0.9 Ω (typical) P-Channel MOSFET is used as the pass transistor for the SiP21106/7/8 part series. The MOSFET transistor offers many advantages over the more, formerly, common PNP pass transistor designs, which ultimately result in longer battery lifetime. The main disadvantage of PNP pass transistors is that they require a certain base current to stay on, which significantly increases under heavy load conditions. In addition, during dropout, when the pass transistor saturates, the PNP regulators waste considerable current. In contrast, P-Channel MOSFETS require virtually zero-base drive and do not suffer from the stated problems. These savings in base drive current translate to lower quiescent current which is typical around 35 µA as shown in the *Typical Characteristics.*

Shutdown and Auto-Dischage/No-Discharge

Bringing the EN voltage low will place the part in shutdown mode where the device output enters a high-impedance state and the quiescent current is reduced to below 1 µA, reducing the drain on the battery in standby mode and increasing standby time. Connect EN pin to input for normal operation. The output has an internal pull down to discharge the output to ground when the EN pin is low. The internal pull down is a 100 Ω typical resistor, which can discharge a 1 µF in less than 1 ms. Refer to *Typical Operating Waveforms* for turn-off waveforms.

Output Voltage Selection

The SiP21106 has fixed voltage outputs that are preset to voltages from 1.8 V to 4.6 V (see Ordering Information).

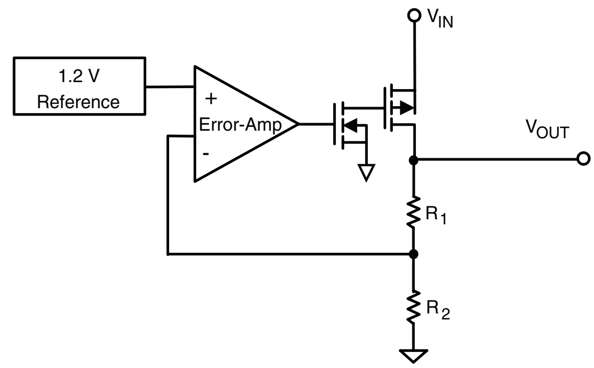


Figure 4.

The SiP21108 has a user-adjustable output that can be set through the resistor feedback network consisting of R_1 and R_2. R_2 range of 100K to 400K is recommended to be consistent with ground current specification. R_1 can then be determined by the following equation:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{ref}} - 1\right)$$

Where V_{ref} is typically 1.2005 V. Use 1 % or better resistors for better output voltage accuracy (see Figure 4).

Current Limit

The SiP21106/7/8 include a current limit block which monitors the current passing through the pass transistor through a current mirror and controls the gate voltage of the MOSFET, limiting the output current to 330 mA (typical). This current limit feature allows for the output to be shorted to ground for an indefinite amount of time without damaging the device.

Thermal-Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds T_J = 150 °C, the device turns the P-Channel pass transistor off allowing the device to cool down. Once the temperature drops by about 20 °C, the thermal sensor turns the pass transistor on again and resumes normal operation. Consequently, a continuous thermal overload condition will result in a pulsed output. It is generally recommended to not exceed the junction temperature rating of 125 °C for continuous operation.

Noise Reduction in SiP21106

For the SiP21106, an external 10 nF bypass capacitor at BP pin is used to create a low pass filter for noise reduction. The startup time is fast, since a power-on circuit pre-charges the bypass capacitor. After the power-up sequence the pre-charge circuit is switched to standby mode in order to save current. It is therefore not recommended to use larger bypass capacitor values than 50 nF. When the circuit is used without a capacitor, stable operation is guaranteed.

POK Status in SiP21107

The POK comparator monitors the output until the supply comes up to specified percentage of V_{IN}. This open drain NMOS output requires an external pull-up resistor to either V_{OUT} or V_{IN}. The internal NMOS can drive up to 0.5 mA loads. POK pin is actively high to indicate an output normal operation condition on regulator and goes low to indicate under-voltage on regulator.

APPLICATION INFORMATION

Input/Output Capacitor Selection and Regulator Stability

It is recommended that a low ESR 1 µF capacitor be used on the SiP21106/7/8 input. A larger input capacitance with lower ESR would improve noise rejection and line-transient response. A larger input bypass capacitor may be required in applications involving long inductive traces between the source and LDO. The circuit is stable with only a small output capacitor equal to 6 nF/mA (≈ 1 µF at 150 mA) of load. Since the bandwidth of the error amplifier is around 1 - 3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150 mA load current, an ESR < 0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated. Applying a larger output capacitor would increase power supply rejection and improve load-transient response. Some ceramic dielectrics such as the Z5U and Y5V exhibit large capacitance and ESR variation over temperature. If such capacitors are used, a 2.2 µF or larger value may be needed to ensure stability over the industrial temperature range. If using higher quality ceramic capacitors, such as those with X7R and Y7R dielectrics, a 1 µF capacitor will be sufficient at all operating temperatures.

Operating Region and Power Dissipation

An important consideration when designing power supplies is the maximum allowable power dissipation of a part. The maximum power dissipation in any application is dependant on the maximum junction temperature, $TJ_{(max)}$ = 125 °C, the ambient temperature, T_A, and the junction-to-ambient thermal resistance for the package, which is the summation of $\theta_{J\text{-}C}$, the thermal resistance of the package, and $\theta_{C\text{-}A}$, the thermal resistance through the PC board and copper traces. Power dissipation may be formulaically expressed as:

$$P_{(max)} = \frac{T_J(max) - T_A}{\theta_{J\text{-}C} + \theta_{C\text{-}A}}$$

The GND pin of the SiP21106/7/8 acts as both the electrical connection to GND as well as a path for channeling away heat. Connect this pin to a GND plane to maximize heat dissipation.Once maximum powChanneler dissipation is calculated using the equation above, the maximum allowable output current for any input/output potential can be calculated as

$$I_{OUT(max)} = \frac{P_{(max)}}{V_{IN} - V_{OUT}}$$

PCB Layout

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitor should be kept close to the LDO. The rise in junction temperature depends on how efficiently the heat is carried away from junction-to-ambient. The junction-to-lead thermal impedance is a characteristic of the package and is fixed. The thermal impedance between lead-to-ambient can be reduced by increasing the copper area on PCB. Increase the input, output and ground trace area to reduce the junction-to-ambient thermal impedance.

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