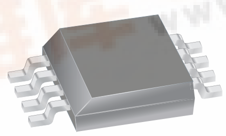
A6850

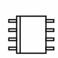
Dual Channel Switch Interface IC

Features and Benefits

- 4.75 to 26.5 V operation
- Low V_{IN}-to-V_{OUT} voltage drop
- $^{1}/_{10}$ current sense feedback
- Survive short-to-battery and short-to-ground faults
- Survive 40 V load dump
- >4 kV ESD rating on the output pins, >2 kV on all other pins
- Output current limiting
- Low operating and Sleep mode currents
- Integrates with Allegro A114x and A118x Hall effect two-wire sensors

Package: 8 pin SOIC (suffix L)



Approximate Scale 1:1 

Description

The Allegro® A6850 is designed to interface between a microprocessor and a pair of 2-wire Hall effect sensors. The A6850 uses protected high-side low resistance DMOS MOSFETs to switch the supply voltage to the two Hall effect devices. Each switch can be controlled independently via individual ENABLE pins and both switches are protected with current-limiting circuitry. The output switches are rated to operate to 26.5 V and will source at least 25 mA per channel before current limiting.

Typical two-wire Hall sensor applications require the user to measure the supply current to determine whether the Hall sensor is switched on (magnetic field present) or switched off (no magnetic field present). This is usually accomplished by using an external series shunt resistor and protection circuits for the microprocessor. In many systems, the sensed voltage is used as the input to a microprocessor analog-to-digital (A-to-D) input. This provides the system with an indication of the status of the two-wire switch as well as provides the capability for diagnostic information if there is an open or shorted sensor.

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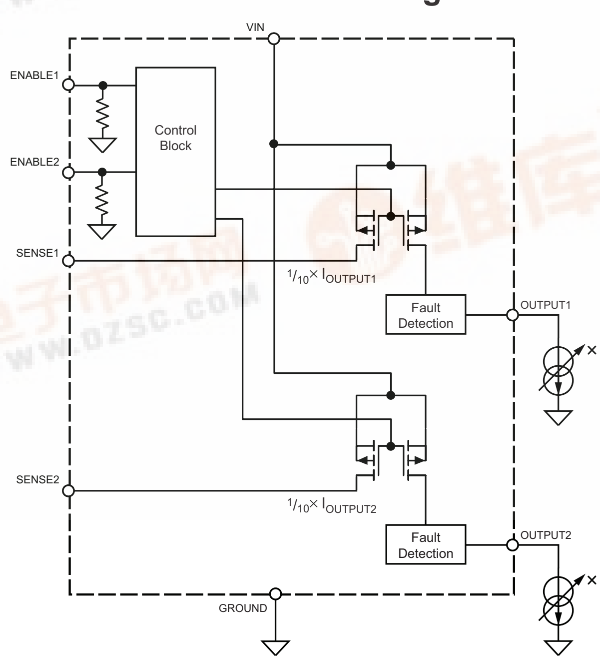
Functional Block Diagram



Description (continued)

The A6850 eliminates the need for the external series shunt resistor in Hall sensor applications by incorporating an integrated current mirror which reports the Hall sensor supply current as a $^1/_{10}$ value on the SENSE1 or SENSE2 output pin. A low current Sleep mode is available (<15 µA) by driving both ENABLE pins low. Also, the A6850 can be used to interface to mechanical switches.

The A6850 is supplied in an 8-pin Pb (lead) free SOIC package, with 100% matte tin leadframe plating.

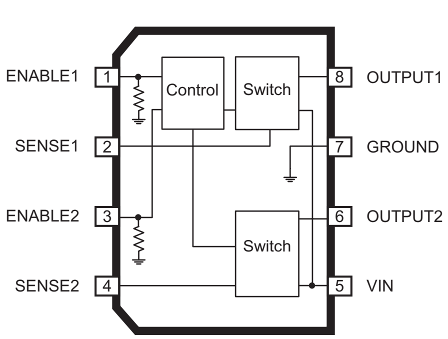
Selection Guide

Part Number	Packing
A6850KLTR-T	13-in. reel, 3000 pieces/reel
A6850KL-T	Tube, 98 pieces/tube

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{IN}		40	V
Output Voltage	$V_{OUTPUTx}$		–0.3 to 40	V
SENSE*x* Voltage Range	V_{SENSEx}		–0.3 to 7	V
ENABLE*x* Voltage Range	$V_{ENABLEx}$		–0.3 to 7	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	$T_J(max)$		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC
ESD Rating - Human Body Model	HBM	AEC-Q100-002; OUTPUT1 and OUTPUT2	4.5	kV
		AEC-Q100-002; all other pins	2.5	kV
ESD Rating - Charged Device Model	CDM	AEC-Q100-011; all pins	1050	V

Pin-out Diagram



Terminal List Table

Name	Number	Description
ENABLE1	1	Digital input pulled to ground
SENSE1	2	Sensed current output
ENABLE2	3	Digital input pulled to ground
SENSE2	4	Sensed current output
VIN	5	Chip power supply voltage
OUTPUT2	6	Switchable voltage supply to sensor
GROUND	7	Ground reference
OUTPUT1	8	Switchable voltage supply to sensor

ELECTRICAL CHARACTERISTICS at T_J = -40 to +150°C (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Input Voltage Range	V_{IN}		4.75	–	26.5	V
Supply Input Quiescent Current	I_{INQ}	Operating mode, $I_{OUTPUTx}$ = 0 mA	–	–	5.0	mA
		Sleep mode: ENABLE1 and ENABLE2 low $V_{OUTPUT1} = V_{OUTPUT2}$ = 0 V	–	–	15	µA
Power-Up Time[1]	t_{ON}		–	–	20	µs
OUTPUTx Source Resistance	$R_{DS(on)}$	$I_{OUTPUTx}$ = 20 mA	–	–	35	Ω
OUTPUTx Leakage Current	$I_{OUTPUTQ}$	$V_{OUTPUTx}$ = 0 V; disabled	–	–	20	µA
SENSE*x* Output Current Offset[2]	$I_{SENSE(ofs)}$	$I_{SENSEx} = (I_{OUTPUTx} / 10) + I_{SENSE(ofs)}$, I_{OUTPUT} = 2 mA to 20 mA	–100	–	100	µA
	I_{SENSEQ}	V_{SENSEx} = 0 V; disabled	–	–	10	µA
SENSE*x* Voltage[3]	V_{SENSEx}	V_{IN} > 7 V	0	–	6	V
		V_{IN} < 7 V	0	–	V_{IN} – 1	V
ENABLE*x* Input Voltage Range	$V_{ENABLEH}$		2.0	–	–	V
	$V_{ENABLEL}$		–	–	0.4	V
ENABLE*x* Input Hysteresis	$V_{ENABLEhys}$	At least one output enabled	150	–	350	mV
ENABLE*x* Current	I_{ENABLE}	ENABLE*x* = 2.0 V	–	40	100	µA
		ENABLE*x* = 0.4 V	–	8.0	20	µA
OUTPUT Current Limit	$I_{OUTPUTM}$		25.0	35.0	45.0	mA
OUTPUT Reverse Bias Current	$I_{OUTPUT(rvrs)}$	Reverse bias blocking: V_{IN} = 4.75 V, V_{OUTPUT} = 26.5 V	–	500	750	µA
Overvoltage Protection Threshold	V_{OVP}	Rising V_{IN}	27.0	–	33.0	V
Overvoltage Protection Hysteresis	V_{OVPhys}		–	2.0	–	V
Thermal Shutdown Threshold	T_{TSD}	Temperature Increasing	–	175	–	°C
Thermal Shutdown Hysteresis	T_{TSDhys}		–	15	–	°C

[1]Delay from end of Sleep mode to outputs enabled.
[2]For input and output current specifications, negative current is defined as coming out of (sourced from) the specified device pin.
[3]User to ensure that V_{SENSEx} remains within the specified range. If V_{SENSEx} exceeds the maximum value, the device is self-protected by an internal clamp, but not all parameters perform as specified.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	80	ºC/W
		1-layer PCB with copper limited to solder pads	140	ºC/W

*Additional thermal data available on the Allegro Web site.

Functional Description

Thermal Shutdown (TSD)

The A6850 protects itself from excessive heat damage by disabling both outputs when the junction temperature, T_J, rises above the TSD threshold (T_{TSD}). The outputs will remain off until the junction temperature falls below the T_{TSD} level minus the TSD hysteresis, T_{TSDhys}.

T_J can be estimated by calculating the power dissipation (P_D) of the A6850. To calculate P_D:

$$P_D = V_{IN} I_{INQ} - V_{OUTPUT1} I_{OUTPUT1} - V_{OUTPUT2} I_{OUTPUT2} - V_{SENSE1} I_{SENSE1} - V_{SENSE2} I_{SENSE2} \,. \tag{1}$$

$$P_D = V_{IN} I_{INQ} + (V_{IN} - V_{OUTPUT1}) I_{OUTPUT1} + (V_{IN} - V_{OUTPUT2}) I_{OUTPUT2} + (V_{IN} - V_{SENSE1}) I_{SENSE1} + (V_{IN} - V_{SENSE2}) I_{SENSE2} \,. \tag{2}$$

The temperature rise of the A6850 can be calculated by multiplying P_D and the thermal resistance from junction to ambient, $R_{\theta JA}$. The formula for temperature rise, ΔT, is:

$$\Delta T = P_D \times R_{\theta JA} \,. \tag{3}$$

The $R_{\theta JA}$ for an 8-pin SOIC (Allegro L package) on a one-layer board with minimum copper area is 140°C/W. (More thermal data is available on the Allegro MicroSystems Web site.)

The total junction temperature can be calculated by:

$$T_J = T_A + \Delta T \,, \tag{4}$$

where T_A is the ambient air temperature.

Example: Calculating the power dissipation and temperature rise, given:

$T_A = 25°C$,
$V_{IN} = 5$ V,
$I_{INQ} = 5$ mA,
$I_{OUTPUT1} = I_{OUTPUT2} = 15$ mA,
$V_{Dropx} = V_{IN} - V_{OUTPUTx} = 0.7$ V,
$I_{SENSEx} = I_{OUTPUTx} / 10 = 1.5$ mA, and
$R_{SENSE1} = R_{SENSE2} = 2$ kΩ.

Then:

$$P_D = 5\text{ V} \times 5\text{ mA} + 0.7\text{ V} \times 15\text{ mA} + [5\text{ V} - (1.5\text{ mA} \times 2\text{ k}\Omega)] \times 1.5\text{ mA} + 0.7\text{ V} \times 15\text{ mA} + [5\text{ V} - (1.5\text{ mA} \times 2\text{ k}\Omega)] \times 1.5\text{ mA} = 52\text{ mW} \,.$$

Substituting in equation 3:

$$\Delta T = 52\text{ mW} \times 140°\text{C/W} = 7.3°\text{C} \,.$$

Substituting in equation 4:

$$T_J = 25°\text{C} + 7.3°\text{C} = 32.3°\text{C} \,.$$

Output Current Limit

The A6850 limits the output current to a maximum current of $I_{OUTPUTM}$. The output current will remain at the current limit until the output load is reduced or the A6850 goes into thermal shutdown.

The high output current limit allows the bypass capacitor, C_{BYP}, on the Hall sensor to charge up quickly. This allows a high slew rate on the VCC pin of the Hall sensor, ensuring that the sensor Power-On State will be correct. See the Applications Information section for schematic diagrams and power calculations.

Output Faults

The A6850 withstands short-to-ground or short-to-battery of the OUTPUTx pins. In the case of short-to-ground, current is held to the current limit ($I_{OUTPUTM}$).

If $V_{OUTPUTx}$ > (V_{IN} + 0.7 V) during short-to-battery, the A6850 monitors $V_{OUTPUTx}$ and disables the outputs. Because the protection circuitry requires a finite amount of time to disable the outputs, a bypass capacitor of 1 μF is necessary on VIN. Although OUTPUTx sinks current into the A6850 in this state, the current is bled to ground and does not charge-up capacitors tied to VIN.

Overvoltage Protection

The A6850 has built-in overvoltage protection against a load dump on the supply bus. In the case of a load dump, or when V_{IN} is connected to the battery supply bus and V_{IN} rises above the overvoltage threshold, V_{OVP}, the A6850 will shut off the outputs.

SENSE Pin Outputs

The A6850 divides the OUTPUT*x* pin current by 10 and mirrors it onto the corresponding SENSE*x* pin. Putting sense resistors, RSENSE, from these pins to ground will create a voltage that can be read by an ADC (analog-to-digital converter). The value of R_{SENSE} should be chosen so that the voltage drop across the sense resistor (V_{RSENSE}) does not exceed the maximum voltage rating of the ADC. For further protection of the ADC, an external clamping circuit, such as a Zener diode, can be used to clamp any transient current spikes that may occur on the output that would be translated onto the SENSE pins.

The sense current is one tenth of the output current, plus an offset current. This offset current is consistent across the whole range of the output current. The sense current can be calculated by the following formula:

$$I_{SENSEx} = (I_{OUTPUTx} / 10) + I_{SENSE(ofs)} . \quad (5)$$

The sense resistor must also be chosen to meet the voltage limits on the sense pin (see Electrical Characteristics table).

Sleep Mode

Low-leakage or sleep modes are required in automotive applications to minimize battery drain when the vehicle is parked. The A6850 enters sleep mode when both ENABLE pins are low. In sleep mode, the internal regulators and all other internal circuitry are disabled.

When enabling an output, the part must first come out of sleep mode. Consequently, the wake-up time amounts to a propagation delay before the outputs turn on. Also, the ENABLE pins do not switch with hysteresis until the regulators stabilize.

After the internal regulators stabilize, internal circuitry is enabled and the outputs turn on, as shown in figure 1. As long as one ENABLE pin is held high, the A6850 operates with hysteresis.

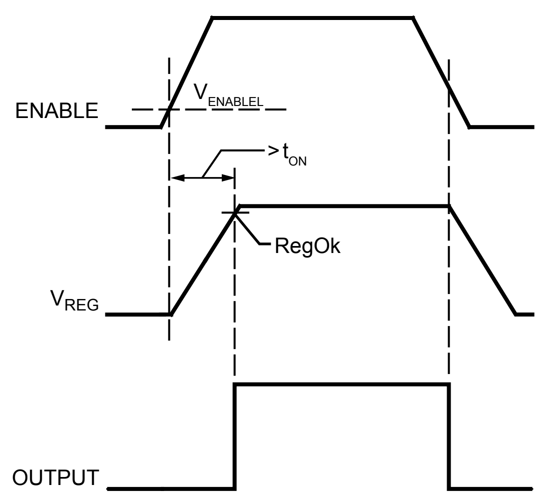


Figure 1. Activation Timing Diagram. Exiting Sleep mode via ENABLE signal to output waveform.

Applications Information

Two-Wire Sensor Interfacing

When voltage is applied to two-wire Hall effect sensors, current flows within one of two narrow ranges. Any current level not within these ranges indicates a fault condition.

The following table describes some of the possible output conditions that can be monitored through the SENSE pins. Figure 2 is a typical application using the A6850 with dual Hall effect sensors.

Signal and Fault Table

Condition	Output Pin Current (mA)	Sense Pin Current (mA)	Sense Pin Voltage, R_{sense}= 1.5 k (V)
OUTPUT Pin Short-to-Ground	25 to 45	2.5 to 4.5	3.75 to 6.75
Logic High from Hall Sensor	12 to 17	1.2 to 1.7	1.8 to 2.55
Short-to-Battery	0.0	0.0	0
Logic Low from Hall Sensor*	2 to 6.9	0.2 to 0.69	0.3 to 1.04
Thermal Shutdown	0.0	0.0	0
OUTPUT Pin Open	0.0	0.0	0

*This current range includes all A114x and A118x sensors.

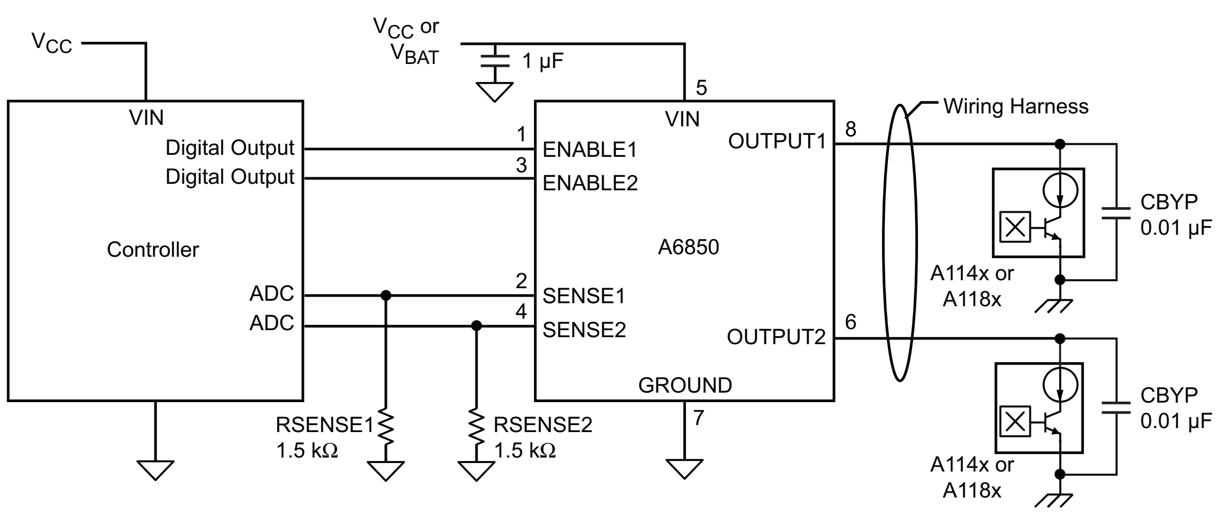


Figure 2. Typical Application with 2-Wire Hall Effect Sensors

Mechanical Switch Interfacing

The A6850 can be used as an interface between mechanical switches, set in a switch-to-ground configuration, and a low voltage microprocessor. A series resistor must be placed in the circuit to limit current when the mechanical switch is closed, in order to prevent excessive power dissipation in the A6850.

For example, to calculate the power dissipation in the A6850 driving two mechanical switches with 1 kΩ series resistors, with V_{IN} = 12 V, assume that the current limit for each of the outputs is set to the maximum value, $I_{OUTPUTM}$ (max) = 45 mA.

When the mechanical switch is closed without a series resistor, the A6850 will be at the current limit. The full 12 V of the power supply will drop across the A6850 at 45mA The power dissipation for one mechanical switch closed would be:

$$P_{D1} = V_{Drop1} \times I_{OUTPUT1} \quad (6)$$
$$= 12\text{ V} \times 45\text{ mA}$$
$$= 540\text{ mW} .$$

A series resistor included in the circuit reduces power dissipation in the A6850. The voltage drop across the resistor would be:

$$V_{RSERIES} = V_{IN} - V_{Drop1} \quad (7)$$
$$= 12\text{ V} - 0.7\text{ V}$$
$$= 11.3\text{ V} .$$

The current is then limited to:

$$I_{OUTPUT1} = V_{RSERIES} / R_{SERIES} \quad (8)$$
$$= 11.3\text{ V} / 1\text{ k}\Omega$$
$$= 11.3\text{ mA} .$$

Power dissipation in the A6850 from this switch is much lower:

$$P_{D1} = V_{Drop1} \times I_{OUTPUT1} \quad (9)$$
$$= 0.7\text{ V} \times 11.3\text{ mA}$$
$$= 7.91\text{ mW} .$$

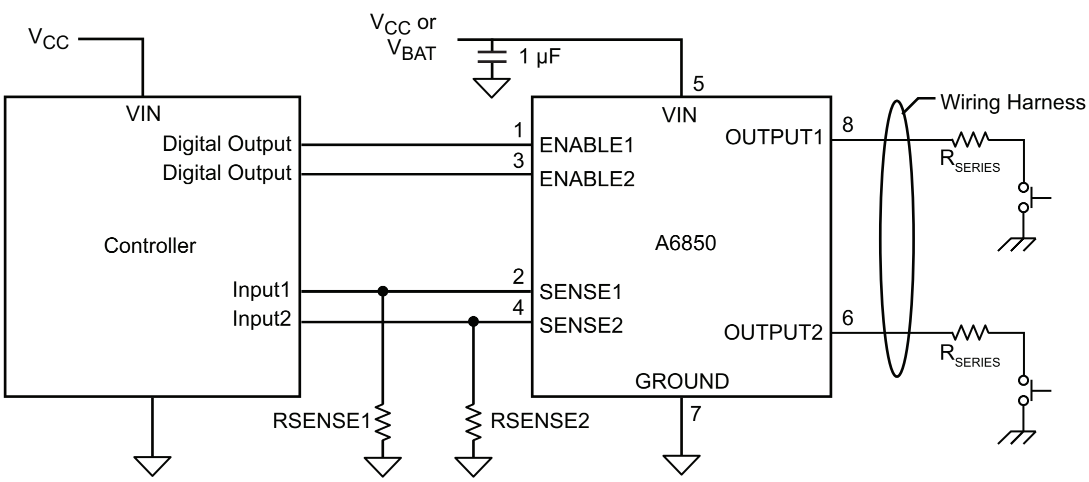
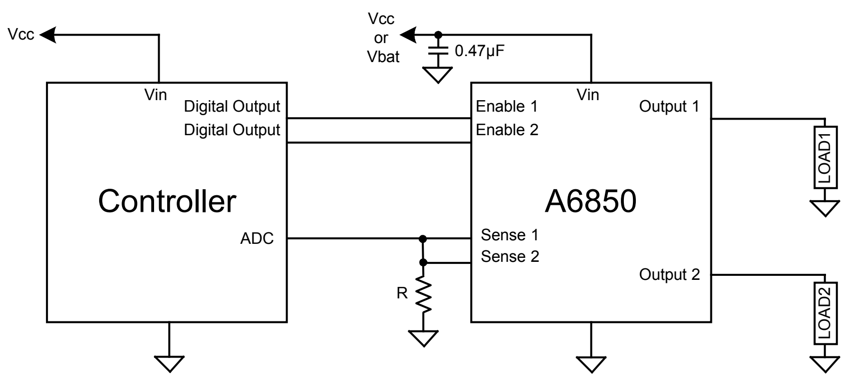
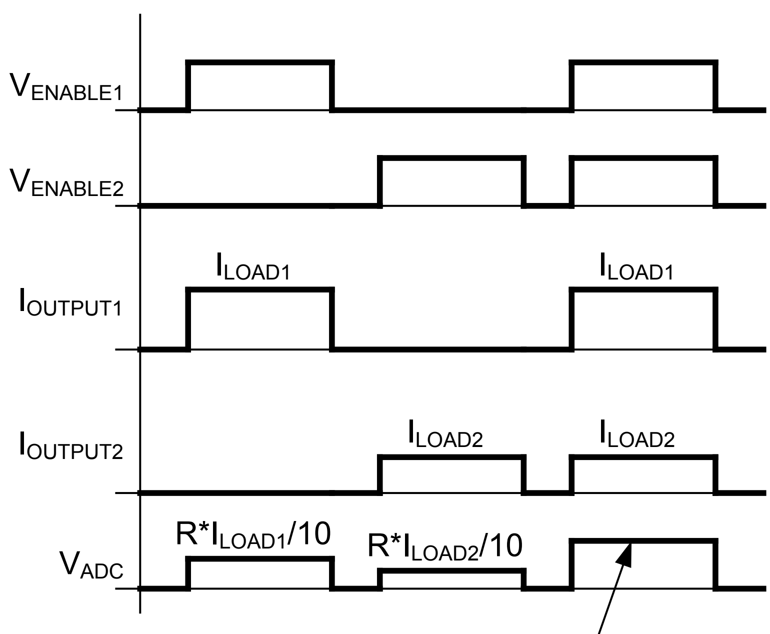


Figure 3. Typical Application with Mechanical Switches

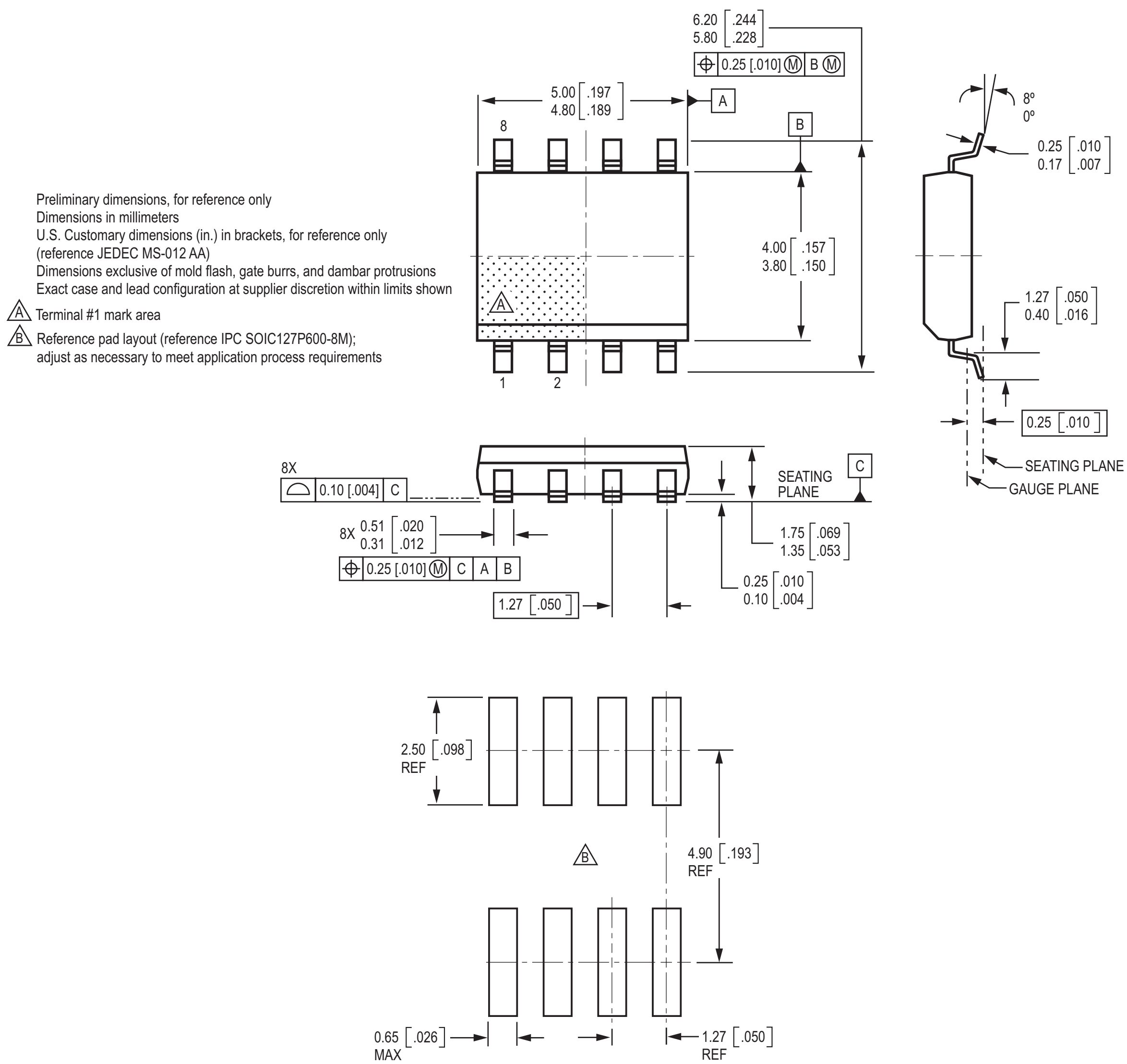
Ganging SENSE1 and SENSE2

In certain applications both outputs may be read with a single ADC channel. The OUTPUTx loads are enabled by alternatively activating ENABLEx. In fact, both ENABLE1 and ENABLE2 may be activated simultaneously, with the SENSE1 and SENSE2 currents added together. For valid measurements the load resistor need only be selected so that V_{SENSEx} remain within specification.





L Package, 8-Pin SOIC



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