Ultra-Low Distortion Differential ADC Driver

Preliminary Technical Data

ADA4938-1

FEATURES

- Extremely low harmonic distortion
  - −112 dBc HD2 @ 10 MHz
  - −79 dBc HD2 @ 50 MHz
  - −102 dBc HD3 @ 10 MHz
  - −81 dBc HD3 @ 50 MHz
- Low input voltage noise: 2.2 nV/√Hz
- High speed
  - −3 dB bandwidth of 1.5 GHz, G = 1
  - Slew rate: 4700 V/µs
  - 0.1 dB gain flatness to 125 MHz
  - Fast overdrive recovery of 4 ns
- 1 mV typical offset voltage
- Externally adjustable gain
- Differential to differential or single-ended to differential operation
- Adjustable output common-mode voltage
- Wide Supply Voltage Range: +5 V & ± 5 V
- Pb-free 3 mm x 3 mm LFCSP package

FUNCTIONAL BLOCK DIAGRAM

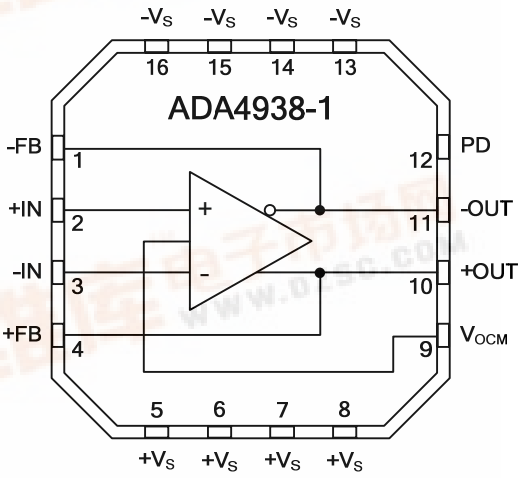

Figure 1.

APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

GENERAL DESCRIPTION

The ADA4938-1 is a low noise, ultra-low distortion, high speed differential amplifier. It is an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 70 MHz. The output common mode voltage is adjustable over a wide range, allowing the ADA4938-1 to match the input of the ADC. The internal common mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

Full differential and single-ended to differential gain configurations are easily realized with the ADA4938-1. A simple external feedback network of four resistors determines the amplifier's closed-loop gain.

The ADA4938-1 is fabricated using ADI's proprietary third generation high-voltage XFCB process, enabling it to achieve very low levels of distortion with input voltage noise of only 2.2 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4938-1 make it well suited for a wide variety of data acquisition and signal processing and applications.

The ADA4938-1 is available in a Pb-free, 3 mm x 3mm lead frame chip scale package (LFCSP). Pinout has been optimized to facilitate layout and minimize distortion. The part is specified to operate over the extended industrial temperature range of −40°C to +85°C.

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12/06—Revision PrA: Initial Version

SPECIFICATIONS

DUAL SUPPLY OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = -5 V, V_{OCM} = 0 V, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = 1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted.
All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} TO ±OUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.1 V p-p, Differential Input		1500		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, Differential Input		125		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, Differential Input		1300		MHz
	V_{OUT} = 4 V p-p, Differential Input		800		MHz
Slew Rate	V_{OUT} = 2 V p-p		4700		V/µs
Overdrive Recovery Time	V_{IN} = 5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−112		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−79		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−102		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−81		dBc
IMD	50 MHz				dBc
IP3	50 MHz				dBm
Voltage Noise (RTI)			2.2		nV/√Hz
Noise Figure	G = +2		21		dB
Input Current Noise			2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-}$ = 0 V		1		mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current			3.5		µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−4.7 to 3.4		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V		−77		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output	-3.9		3.9	V
Linear Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V; 10 MHz		−66		dB
V_{OCM} to ±OUT PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			400		MHz
Slew Rate			1700		V/µs
Input Voltage Noise (RTI)			7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		−3.8		3.8	V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-}$ = 0 V		1	3.5	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		1		V/V
POWER SUPPLY					
Operating Range		4.5		11	V

Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current			40		mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
	Powered down		< 1		mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−90		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤ 1		V
	Enabled		≥ 2		V
Turn-Off Time			1		µs
Turn-On Time			200		ns
$\overline{PD}$ Bias Current					
Enabled	$\overline{PD}$ = 5 V		40		µA
Disabled	$\overline{PD}$ = 0 V		200		µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

SINGLE SUPPLY OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, V_{OCM} = $+V_S$/2, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = 1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted.
All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} TO ±OUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.1 V p-p, Differential Input		1500		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, Differential Input		125		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, Differential Input		1100		MHz
Slew Rate	V_{OUT} = 2 V p-p		3900		V/µs
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−110		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−79		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−100		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−79		dBc
IMD	50 MHz				dBc
IP3	50 MHz				dBm
Voltage Noise (RTI)			2.2		nV/√Hz
Noise Figure	G = +2		21		dB
Input Current Noise			2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		1		mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current			3.5		µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			0.3 to 3.4		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V		−77		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output	1.1		3.9	V
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−66		dB
V_{OCM} TO ±OUT PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			400		MHz
Slew Rate	V = 0.5 V		1700		V/µs
Input Voltage Noise (RTI)			7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		1.2		3.8	V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS, cm}$ = $V_{OUT, cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		1		mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		1		V/V
POWER SUPPLY					
Operating Range		4.5		11	V
Quiescent Current			36		mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
	Powered down		< 1		mA

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−90		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤ 1		V
	Enabled		≥ 2		V
Turn-Off Time			1		µs
Turn-On Time			200		ns
PD Bias Current					
Enabled	$\overline{PD}$ = 5 V		20		µA
Disabled	$\overline{PD}$ = 0 V		−120		µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 2
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	95	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4938-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4938-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through-holes, ground, and power planes reduces the θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP (95 °C/W) on a JEDEC standard 4-layer board.

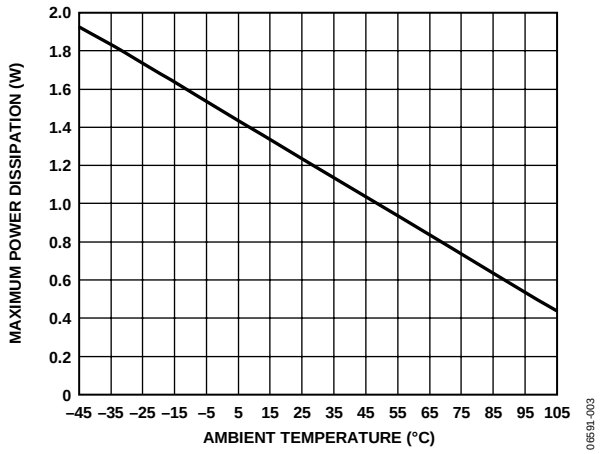

Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

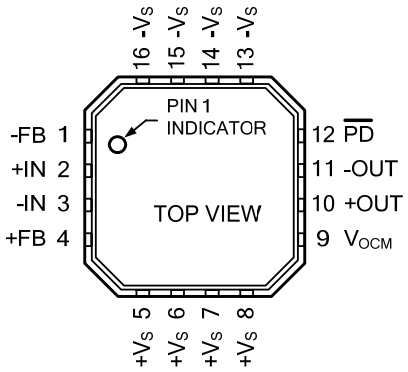

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−FB	Negative Output for Feedback Component Connection
2	+IN	Positive Input Summing Node
3	−IN	Negative Input Summing Node
4	+FB	Positive Output for Feedback Component Connection
5 to 8	$+V_S$	Positive Supply Voltage
9	V_{OCM}	Output Common-Mode Voltage
10	+OUT	Positive Output for Load Connection
11	−OUT	Negative Output for Load Connection
12	$\overline{PD}$	Power-Down Pin
13 to 16	$-V_S$	Negative Supply Voltage

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

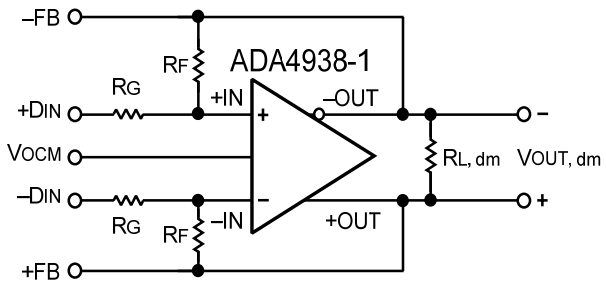

Figure 4. Circuit Definitions

Differential Voltage

This refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-Mode Voltage

This refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Balance is a measure of how well differential signals are matched in amplitude and are exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The ADA4938-1 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4938-1 behaves much like a standard voltage feedback op amp and makes it easier to perform single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Also like an op amp, the ADA4938-1 has high input impedance and low output impedance.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The ADA4938-1 architecture results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to zero. This results in nearly perfectly balanced differential outputs that are identical in amplitude and are exactly 180° apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The ADA4938-1 uses open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 4). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 4 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes the input resistors (R_G) and feedback resistors (R_F) on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4938-1 can be estimated using the noise model in Figure 5. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The noise currents are assumed to be equal and produce a voltage across the parallel combination of the gain and feedback resistances. v_{nCM} is the noise voltage density at the V_{OCM} pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 6 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

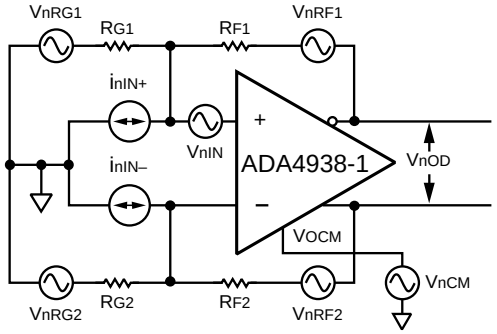

Figure 5. ADA4938-1 Noise Model

Table 6. Output Noise Voltage Density Calculations

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Output Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N(v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{G2} \| \| R_{F2})$	G_N	$v_{nO2} = G_N[i_{nIN-} \times (R_{G2} \| \| R_{F2})]$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{G1} \| \| R_{F1})$	G_N	$v_{nO3} = G_N[i_{nIN+} \times (R_{G1} \| \| R_{F1})]$
V_{OCM} Input	v_{nCM}	v_{nCM}	$G_N(\beta_1 - \beta_2)$	$v_{nO4} = G_N(\beta_1 - \beta_2)(v_{nCM})$
Gain Resistor R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	$G_N(1 - \beta_2)$	$v_{nO5} = G_N(1 - \beta_2)(4kTR_{G1})^{1/2}$
Gain Resistor R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	$G_N(1 - \beta_1)$	$v_{nO6} = G_N(1 - \beta_1)(4kTR_{G2})^{1/2}$
Feedback Resistor R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

THE IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from V_{OCM}, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. When G = 1, with a ground referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, a worst-case differential-mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 6, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

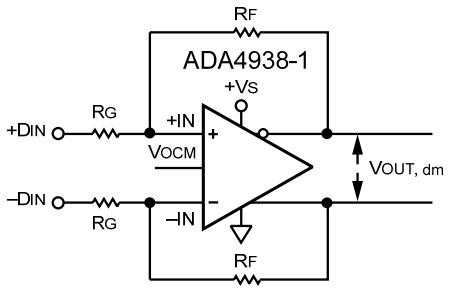

Figure 6. ADA4938-1 Configured for Balanced (Differential) Inputs

For an unbalanced, single-ended input signal (see Figure 7), the input impedance is

$$R_{IN,cm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

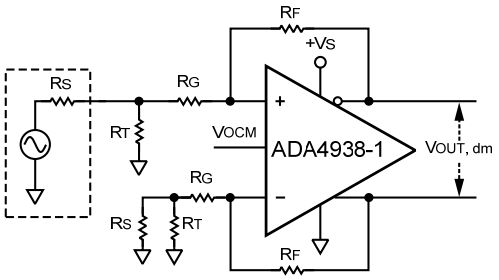

Figure 7. ADA4938-1 Configured for Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The ADA4938-1 is optimized for level-shifting, ground-referenced input signals. As such, the center of the input common-mode range is shifted approximately 1 V down from midsupply. For 5 V single-supply operation, the input common-mode range at the summing nodes of the amplifier is 0.3 V to 3.0 V. To avoid clipping at the outputs, the voltage swing at the +IN and –IN terminals must be confined to these ranges.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4938-1 is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC. However, care must be taken to

assure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ. If multiple ADA4938-1 devices share one reference output, it is recommended that a buffer be used.

Table 7 and Table 8 list several common gain settings, associated resistor values, input impedance, output noise density, and approximate large signal bandwidth for both balanced and unbalanced input configurations. Also shown are the input common-mode voltage swings under the given conditions for different V_{OCM} settings with both dual and single 5 V supplies.

Table 7. Differential Ground-Referenced Input, DC-Coupled; See Figure 6

Nominal Gain (dB)	R_F (Ω)	R_G (Ω)	$R_{IN,dm}$(Ω)	Differential Output Noise Density (nV/√Hz)	Approximate Large-Signal Bandwidth (MHz)	Common-Mode Swing at +IN, –IN (V)			
						$+V_S$ = 5 V, $-V_S$ = -5 V $V_{OUT,dm}$ = 2.0 V p-p		$+V_S$ =5 V $V_{OUT,dm}$ = 2.0 V p-p	
						V_{OCM} = 0 V	V_{OCM} = 3.5 V	V_{OCM} = 2.5 V	V_{OCM} = 3.2 V
0	200	200	400	5.8		-0.50 to 0.50	1.25 to 2.25	0.75 to 1.75	1.10 to 2.10
	348	348	696	6.7					
3	280	200	400	7.2		-0.35 to 0.35	1.10 to 1.82	0.69 to 1.40	0.98 to 1.69
	348	249	498	7.6					
6	200	100	200	8.0		-0.25 to 0.25	0.92 to 1.42	0.58 to 1.08	0.82 to 1.32
	348	174	348	9.0					
10	316	100	200	11		-0.16 to 0.16	0.68 to 1.00	0.44 to 0.76	0.61 to 0.92
	348	110	220	12					
12	402	100	200	14		-0.13 to 0.13	0.57 to 0.82	0.37 to 0.62	0.51 to 0.76
	348	86.6	173	13					
14	499	100	200	17		-0.10 to 0.10	0.48 to 0.68	0.32 to 0.52	0.43 to 0.63
	348	69.8	140	16					

Table 8. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω; See Figure 7

Nominal Gain (dB)	R_F (Ω)	R_{G1} (Ω)	R_T (Ω)	$R_{IN,cm}$ (Ω)	R_{G2} (Ω)[1]	Differential Output Noise Density (nV/√Hz)	Approximate Large-Signal Bandwidth (MHz)	Common-Mode Swing at +IN, -IN (V)			
								$+V_S$ = 5 V, $-V_S$ = -5 V $V_{OUT,dm}$ = 2.0 V p-p		$+V_S$ =5 V $V_{OUT,dm}$ = 2.0 V p-p	
								V_{OCM} = 0 V	V_{OCM} = 3.5 V	V_{OCM} = 2.5 V	V_{OCM} = 3.2 V
0	200	200	61.9	267	226	5.5		-0.56 to 0.56	1.29 to 2.42	0.75 to 1.75	1.13 to 2.26
	348	348	56.2	464	374	6.5					
3	280	200	60.4	282	226	6.8		-0.40 to 0.40	1.16 to 1.97	0.71 to 1.52	1.03 to 1.83
	348	249	59.0	351	274	7.3					
6	200	100	75.0	150	130	7.0		-0.33 to 0.33	1.05 to 1.70	0.66 to 1.31	0.94 to 1.59
	348	174	61.9	261	200	8.4					
10	316	100	73.2	161	130	9.7		-0.21 to 0.21	0.82 to 1.23	0.52 to 0.93	0.73 to 1.14
	348	110	69.8	177	140	10					
12	402	100	71.5	167	130	12		-0.16 to 0.16	0.70 to 1.02	0.45 to 0.77	0.62 to 0.94
	348	86.6	76.8	144	118	11					
14	499	100	71.5	171	130	14		-0.13 to 0.13	0.59 to 0.85	0.39 to 0.65	0.53 to 0.79
	348	69.8	86.6	120	100	12					

[1] $R_{G2} = R_{G1} + (R_S||R_T)$

LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4938-1 is sensitive to the PCB environment in which it operates. Realizing its superior performance requires attention to the details of high speed PCB design.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4938-1 as possible. However, the area near the feedback resistors (R_F), gain resistors (R_G), and the input summing nodes (Pin 2 and Pin 3) should be cleared of all ground and power planes (see Figure 8). This minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies.

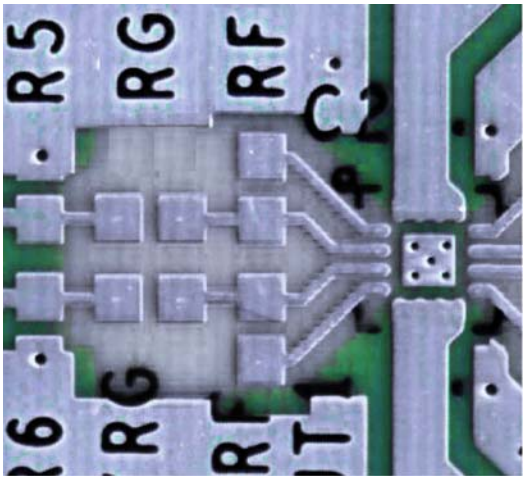

Figure 8. Ground and Power Plane Voiding in Vicinity of R_F and R_G

The power supply pins should be bypassed as close to the device as possible and directly to a nearby ground plane. High frequency ceramic chip capacitors should be used. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 µF) be used for each supply. The 1000 pF capacitor should be placed closer to the device. Further away, low frequency bypassing should be provided, using 10 µF tantalum capacitors from each supply to ground.

Signal routing should be short and direct to avoid parasitic effects. Wherever complementary signals exist, a symmetrical layout should be provided to maximize balanced performance. When routing differential signals over a long distance, PCB traces should be close together, and any differential wiring should be twisted such that loop area is minimized. This reduces radiated energy and makes the circuit less susceptible to interference.

OUTLINE DIMENSIONS

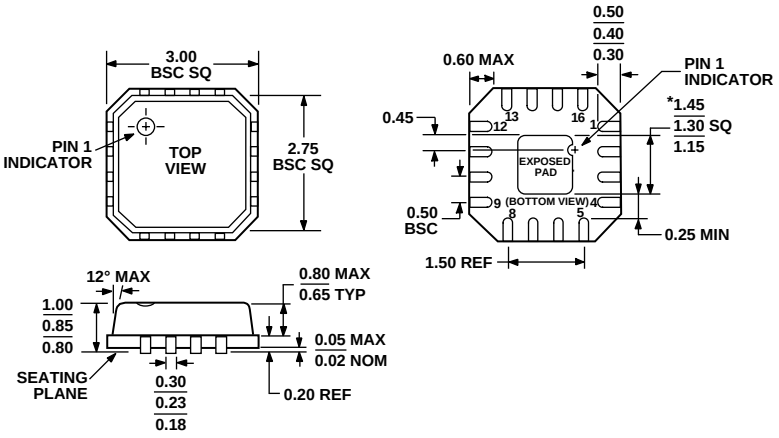

Figure 9. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body
(CP-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Ordering Quantity	Temperature Range	Package Description	Package Option	Branding
ADA4938-1ACPZ-R2	5,000	−40°C to +85°C	16-Lead 3 mm × 3 mm LFCSP	CP-16-2	TBD
ADA4938-1ACPZ-RL	1,500	−40°C to +85°C	16-Lead 3 mm × 3 mm LFCSP	CP-16-2	TBD
ADA4938-1ACPZ-R7	250	−40°C to +85°C	16-Lead 3 mm × 3 mm LFCSP	CP-16-2	TBD