ANALOG DEVICES

+3 V/+5 V/±5 V CMOS 4- and 8-Channel Analog Multiplexers

ADG658/ADG659

FEATURES

±2 V to ±6 V dual supply
2 V to 12 V single supply
Automotive temperature range −40°C to +125°C
<0.1 nA leakage currents
45 Ω on resistance over full signal range
Rail-to-rail switching operation
Single 8-to-1 multiplexer ADG658
Differential 4-to-1 multiplexer ADG659
16-lead LFCSP/TSSOP/QSOP packages
Typical power consumption <0.1 μW
TTL/CMOS compatible inputs
Package upgrades to 74HC4051/74HC4052 and MAX4051/MAX4052/MAX4581/MAX4582

APPLICATIONS

Automotive applications
Automatic test equipment
Data acquisition systems
Battery-powered systems
Communication systems
Audio and video signal routing
Relay replacement
Sample-and-hold systems
Industrial control systems

GENERAL DESCRIPTION

The ADG658 and ADG659 are low voltage, CMOS analog multiplexers comprised of eight single channels and four differential channels, respectively. The ADG658 switches one of eight inputs (S1–S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. The ADG659 switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines A0 and A1. An $\overline{\text{EN}}$ input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

These parts are designed on an enhanced process that provides lower power dissipation yet gives high switching speeds. These parts can operate equally well as either multiplexers or demultiplexers and have an input range that extends to the supplies. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. All digital inputs have 0.8 V to 2.4 V logic thresholds, ensuring TTL/CMOS logic compatibility when using single +5 V or dual ±5 V supplies.

The ADG658 and ADG659 are available in 16-lead TSSOP/QSOP packages and 16-lead 4 mm × 4 mm LFCSP packages.

PRODUCT HIGHLIGHTS

1. Single- and dual-supply operation.
   The ADG658 and ADG659 offer high performance and are fully specified and guaranteed with ±5 V, +5 V, and +3 V supply rails.
2. Automotive temperature range −40°C to +125°C.
3. Low power consumption, typically <0.1 μW.
4. 16-lead 4 mm × 4 mm LFCSP packages, 16-lead TSSOP package and 16-lead QSOP package.

FUNCTIONAL BLOCK DIAGRAM

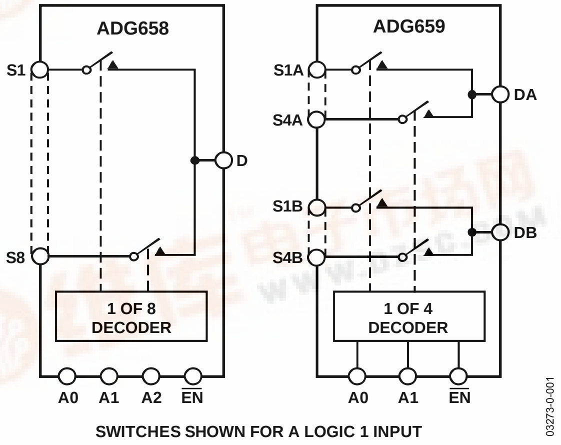

Figure 1.

Rev. A

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REVISION HISTORY

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Updated Format .... Universal
Added QSOP Package Outline 20
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3/03—Rev. 0: Initial Version

SPECIFICATIONS: DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to+125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance (R_{ON})	45			Ω typ	V_S = ±4.5 V, I_S = 1 mA;
	75	90	100	Ω max	Test Circuit 1
On Resistance Match between	1.3			Ω typ	
Channels (ΔR_{ON})	3	3.2	3.5	Ω max	V_S = 3.5 V, I_S = 1 mA
On Resistance Flatness ($R_{FLAT(ON)}$)	10			Ω typ	V_{DD} = +5 V, V_{SS} = −5 V;
	16	17	18	Ω max	V_S = ±3 V, I_S = 1 mA
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source OFF Leakage I_S (OFF)	±0.005			nA typ	V_D = ±4.5 V, V_S = ∓ 4.5 V;
	±0.2		±5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.005			nA typ	V_D = ±4.5 V, V_S = ∓ 4.5 V;
ADG658	±0.2		±5	nA max	Test Circuit 3
ADG659	±0.1		±2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.005			nA typ	V_D = V_S = ±4.5 V; Test Circuit 4
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{TRANS}	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	140	165	ns max	V_S = 3 V; Test Circuit 5
t_{ON} ($\overline{EN}$)	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	140	165	ns max	V_S = 3 V; Test Circuit 7
t_{OFF} ($\overline{EN}$)	30			ns typ	R_L = 300 Ω, C_L = 35 pF
	45	50	55	ns max	V_S = 3 V; Test Circuit 7
Break-Before-Make Time Delay, t_{BBM}	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; Test Circuit 6
Charge Injection	2			pC typ	V_S = 0 V, R_S = 0 Ω,
	4			pC max	C_L = 1 nF; Test Circuit 8
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
Total Harmonic Distortion, THD + N	0.025			% typ	R_L = 600 Ω, 2 V p-p, f = 20 Hz to 20 kHz
Channel-to-Channel Crosstalk (ADG659)	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 11
−3 dB Bandwidth					
ADG658	210			MHz typ	R_L = 50 Ω, C_L = 5 pF;
ADG659	400			MHz typ	Test Circuit 10
C_S (OFF)	4			pF typ	f = 1 MHz
C_D (OFF)					
ADG658	23			pF typ	f = 1 MHz
ADG659	12			pF typ	f = 1 MHz

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to+125°C	Unit	Test Conditions/Comments
C_D, C_S (ON)					
ADG658	28			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.01			μA typ	Digital Inputs = 0 V or 5.5 V
			1	μA max	
I_{SS}	0.01			μA typ	Digital Inputs = 0 V or 5.5 V
			1	μA max	

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[1] Temperature range is as follows: B Version: −40°C to +85°C. Y Version: −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

SPECIFICATIONS: SINGLE SUPPLY 5V

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance (R_{ON})	85			Ω typ	V_S = 0 V to 4.5 V, I_S = 1 mA;
	150	160	200	Ω max	Test Circuit 1
On Resistance Match between	4.5			Ω typ	V_S = 3.5 V, I_S = 1 mA
Channels (ΔR_{ON})	8	9	10	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	13	14	16	Ω typ	V_{DD} = 5 V, V_{SS} = 0 V
					V_S = 1.5 V to 4 V, I_S = 1 mA
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.005			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V;
	±0.2		±5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.005			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V;
ADG658	±0.2		±5	nA max	Test Circuit 3
ADG659	±0.1		±2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.005			nA typ	V_S = V_D = 1 V or 4.5 V, Test Circuit 4
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{TRANS}	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	270	300	ns max	V_S = 3 V; Test Circuit 5
t_{ON} ($\overline{EN}$)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	190	245	280	ns max	V_S = 3 V; Test Circuit 7
t_{OFF} ($\overline{EN}$)	35			ns typ	R_L = 300 Ω, C_L = 35 pF
	50	60	70	ns max	V_S = 3 V; Test Circuit 7
Break-Before-Make Time Delay, t_{BBM}	100			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; Test Circuit 6
Charge Injection	0.5			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF;
	1			pC max	Test Circuit 8
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz;
(ADG659)					Test Circuit 11
−3 dB Bandwidth					
ADG658	180			MHz typ	R_L = 50 Ω, C_L = 5 pF;
ADG659	330			MHz typ	Test Circuit 10
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)					
ADG658	29			pF typ	f = 1 MHz
ADG659	15			pF typ	f = 1 MHz

C_D, C_S (ON)			
ADG658	30	pF typ	f = 1 MHz
ADG659	16	pF typ	f = 1 MHz
POWER REQUIREMENTS			V_{DD} = 5.5 V
I_{DD}	0.01	μA typ	Digital Inputs = 0 V or 5.5 V
	1	μA max	

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[1] Temperature range is as follows: B Version: −40°C to +85°C. Y Version: −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

SPECIFICATIONS: SINGLE SUPPLY 2.7 TO 3.6 V

V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.[1]

Table 3.

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	V_{DD} = 2.7 V, V_{SS} = 0 V
On Resistance (R_{ON})	185			Ω typ	V_S = 0 V to 2.7 V, I_S = 0.1 mA;
	300	350	400	Ω max	Test Circuit 1
On Resistance Match between	2			Ω typ	V_S = 1.5 V, I_S = 0.1 mA
Channels (ΔR_{ON})	4.5	6	7	Ω max	
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.005			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
	±0.2		±5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.005			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
ADG658	±0.2		±5	nA max	Test Circuit 3
ADG659	±0.1		±2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.005			nA typ	V_S = V_D = 1 V or 3 V, Test Circuit 4
ADG658	±0.2		±5	nA max	
ADG659	±0.1		±2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.5	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{TRANS}	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	370	440	490	ns max	V_S = 1.5 V; Test Circuit 7
t_{ON} ($\overline{EN}$)	230			ns typ	R_L = 300 Ω, C_L = 35 pF
	370	440	490	ns max	V_S = 1.5 V; Test Circuit 7
t_{OFF} ($\overline{EN}$)	50			ns typ	R_L = 300 Ω, C_L = 35 pF
	80	90	110	ns max	V_S = 1.5 V; Test Circuit 7
Break-Before-Make Time Delay, t_{BBM}	200			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 1.5 V; Test Circuit 6
Charge Injection	1			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF;
	2			pC max	Test Circuit 8
Off Isolation	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
Channel-to-Channel Crosstalk (ADG659)	−90			dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; Test Circuit 11
−3 dB Bandwidth					
ADG658	160			MHz typ	R_L = 50 Ω, C_L = 5 pF;
ADG659	300			MHz typ	Test Circuit 10
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)					
ADG658	29			pF typ	f = 1 MHz
ADG659	15			pF typ	f = 1 MHz
C_D, C_S (ON)					
ADG658	30			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.01			μA typ	Digital Inputs = 0 V or 3.6 V
			1	μA max	

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[1] Temperature range is as follows: B Version: −40°C to +85°C. Y Version: −40°C to +125°C.

[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 4.

Parameters	Ratings
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +13 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs[1]	GND −0.3 V to V_{DD} +0.3 V or 10 mA, whichever occurs first
Peak Current, S or D	40 mA
(Pulsed at 1 ms, 10% duty cycle max)	
Continuous Current, S or D	20 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance, 16-Lead QSOP	104°C/W
θ_{JA} Thermal Impedance, 16-Lead TSSOP	150.4°C/W
θ_{JA} Thermal Impedance (4-Layer Board),	
16-Lead LFCSP	70°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	5.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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[1] Over voltages at A_X, $\overline{EN}$, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

Table 5. ADG658 Truth Table

A2	A1	A0	$\overline{\text{EN}}$	Switch Condition
X[1]	X	X	1	NONE
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8

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[1] X = Don't Care

Table 6. ADG659 Truth Table

A1	A0	$\overline{\text{EN}}$	On Switch Pair
X[1]	X	1	NONE
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

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[1] X = Don't Care

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

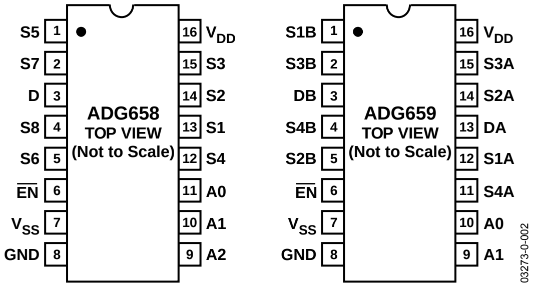
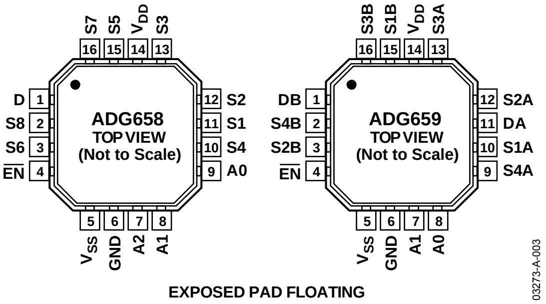


Figure 2. 16-Lead TSSOP/QSOP



EXPOSED PAD FLOATING

Figure 3. 4 mm x 4 mm LFCSP

Table 7. Functional Descriptions

Parameter	Description
V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
A_X	Logic Control Input.
$\overline{EN}$	Active Low Digital Input. When high, device is disabled and all switches are OFF. When low, $A_X$logic inputs determine ON switch.
V_D (V_S)	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match between Any Two Channels, i.e., R_{ON}max – R_{ON}min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of ON Resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch OFF.
I_D (OFF)	Drain Leakage Current with the Switch OFF.
I_D, I_S (ON)	Channel Leakage Current with the Switch ON.
V_{INL}	Maximum Input Voltage for Logic 0.
V_{INH}	Minimum Input Voltage for Logic 1.
I_{INL} (I_{INH})	Input Current of the Digital Input.
C_S (OFF)	OFF Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	OFF Switch Drain Capacitance. Measured with reference to ground.

Parameter	Description
C_D, C_S (ON)	ON Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
t_{ON}	Delay between Applying the Digital Control Input and the Output Switching ON. See Test Circuit 7.
t_{OFF}	Delay between Applying the Digital Control Input and the Output Switching OFF.
t_{BBM}	ON Time. Measured between 80% points of both switches when switching from one address state to another.
Charge Injection	Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output during Switching.
Off Isolation	Measure of Unwanted Signal Coupling through an OFF Switch.
Crosstalk	Measure of Unwanted Signal Coupled through from One Channel to Another as a Result of Parasitic Capacitance.
Bandwidth	The Frequency at which the Output is Attenuated by 3 dB.
On Response	The Frequency Response of the ON Switch.
Insertion Loss	The Loss Due to the ON Resistance of the Switch.

TYPICAL PERFORMANCE CHARACTERISTICS

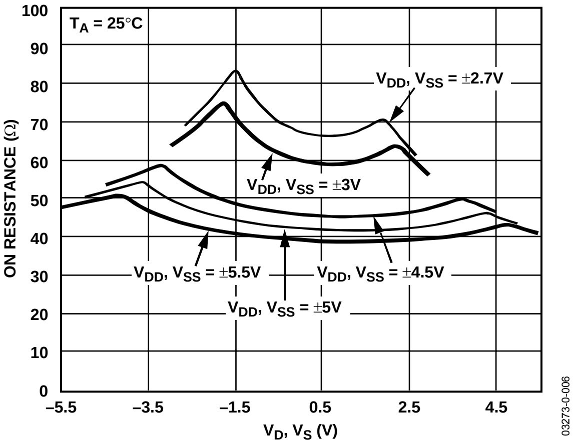


Figure 4. On Resistance vs. V_D (V_S) for Dual Supply

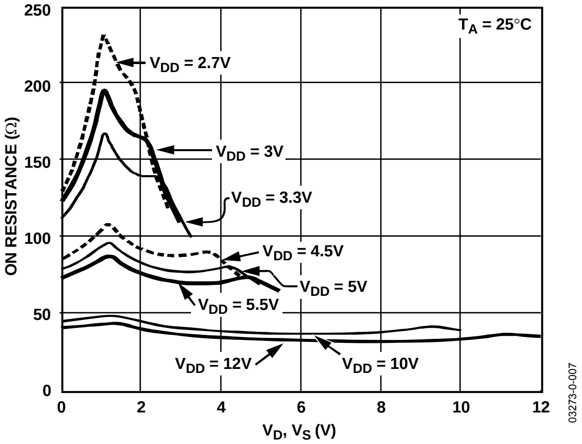


Figure 5. On Resistance vs. V_D (V_S) for Single Supply

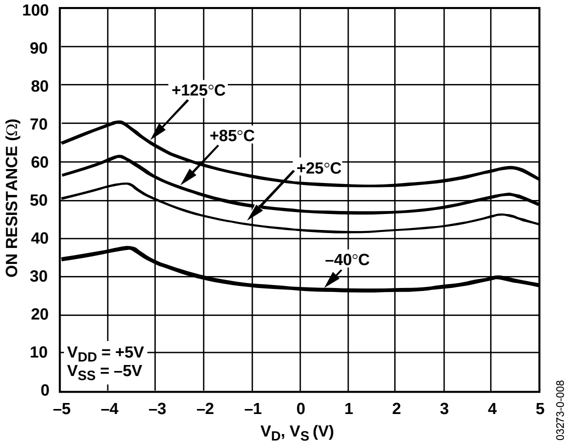


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)

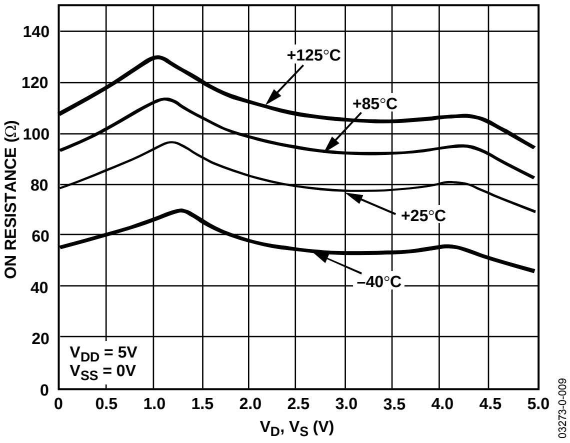


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

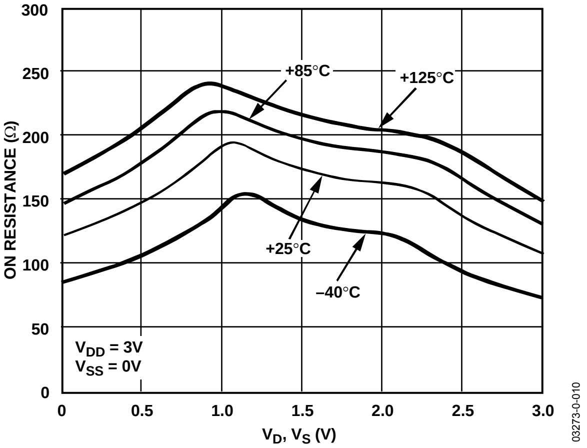


Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

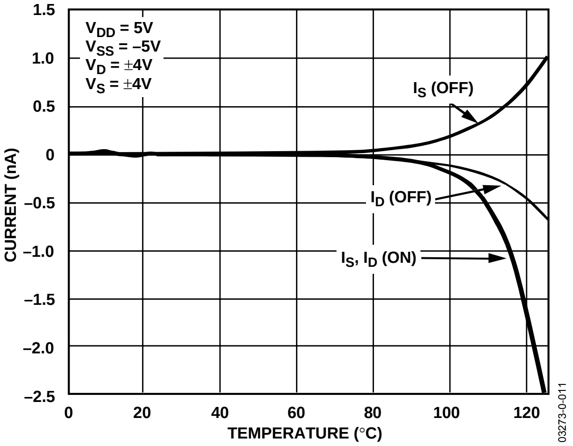


Figure 9. Leakage Current vs. Temperature (Dual Supply)

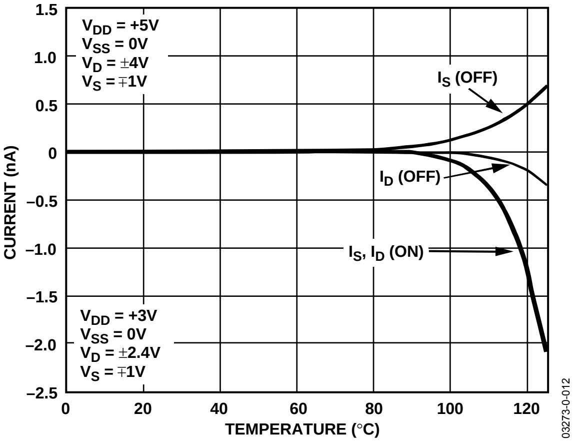


Figure 10. Leakage Current vs. Temperature (Single Supply)

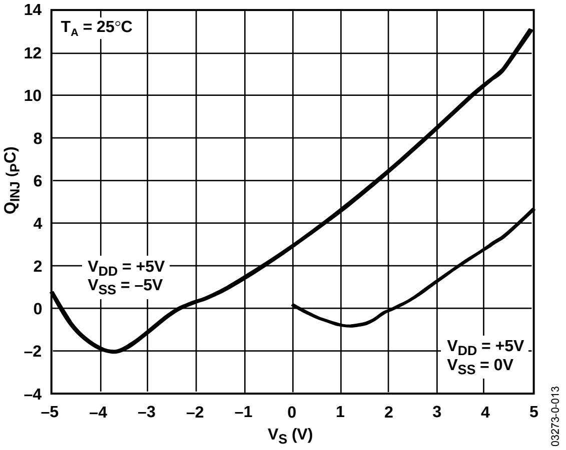


Figure 11. Charge Injection vs. Source Voltage

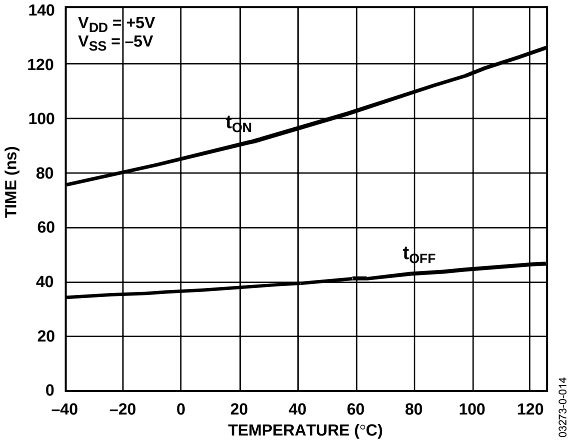


Figure 12. t_{ON}/t_{OFF} Times vs. Temperature (Dual Supply)

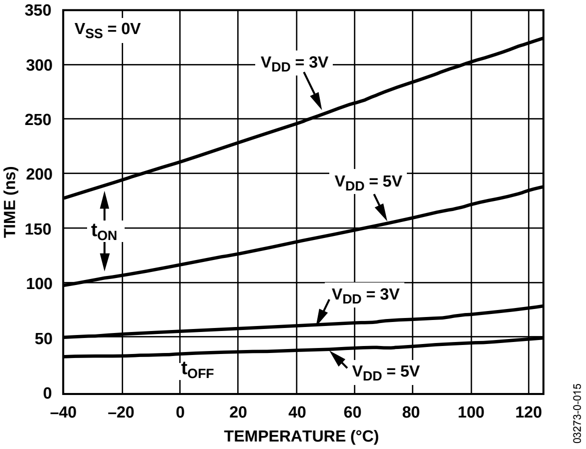


Figure 13. t_{ON}/t_{OFF} Times vs. Temperature (Single Supply)

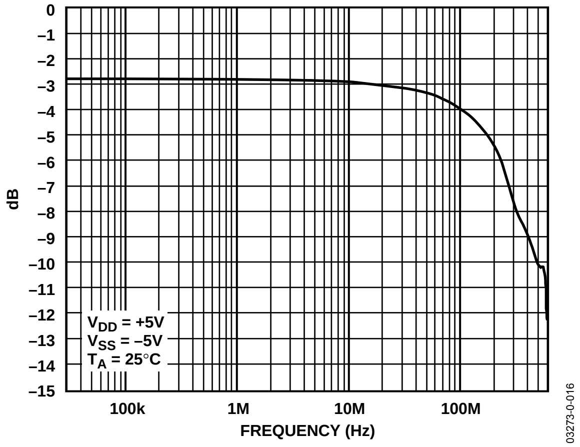


Figure 14. ON Response vs. Frequency (ADG658)

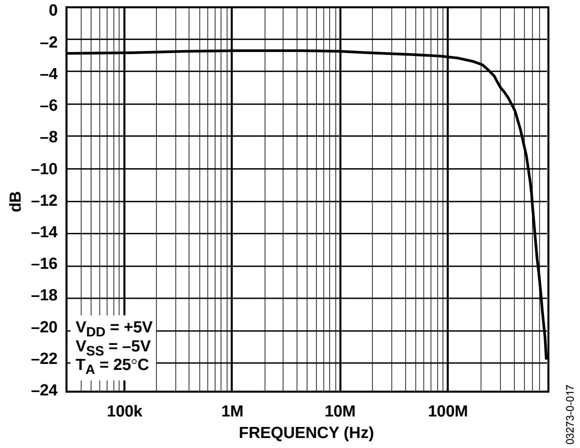


Figure 15. ON Response vs. Frequency (ADG659)

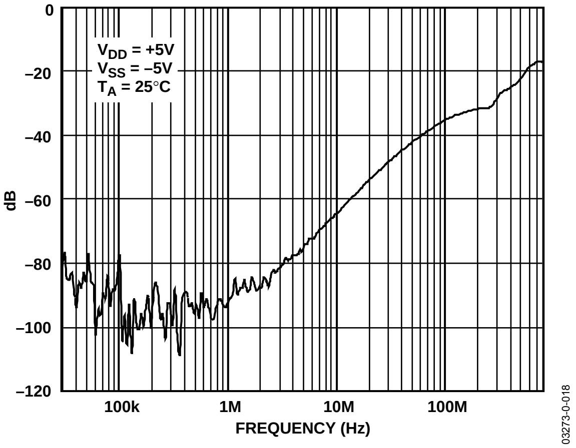


Figure 16. OFF Isolation vs. Frequency

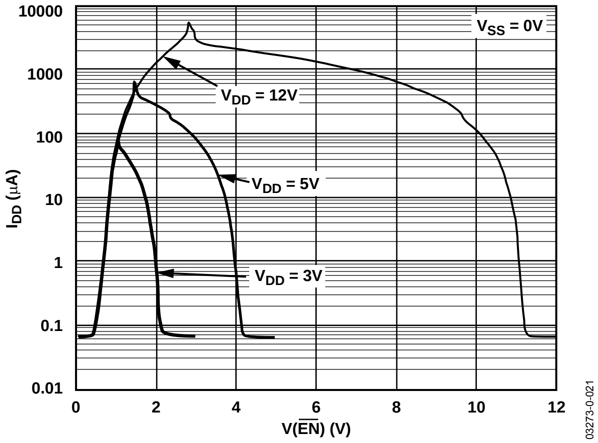


Figure 19. V_{DD} Current vs. Logic Level

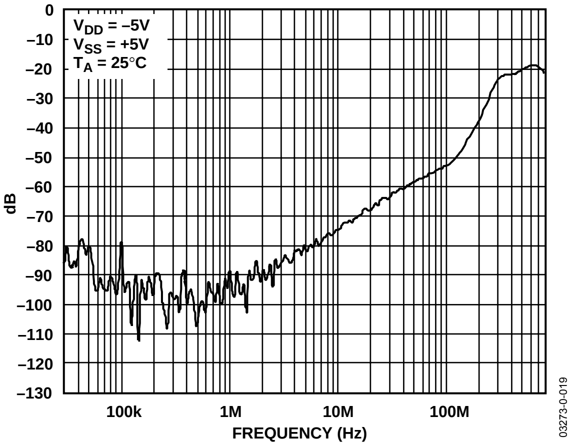


Figure 17. Crosstalk vs. Frequency

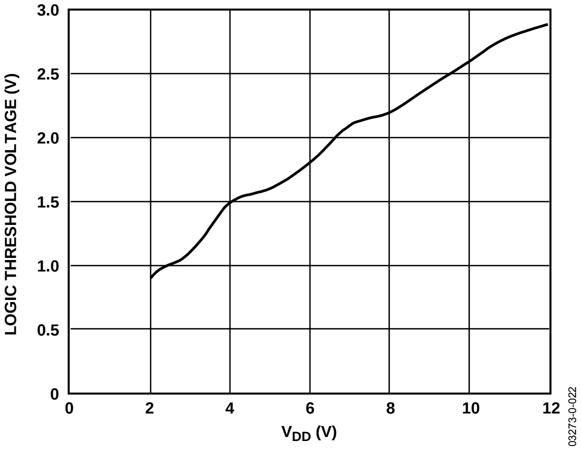


Figure 20. Logic Threshold Voltage vs. Supply Voltage

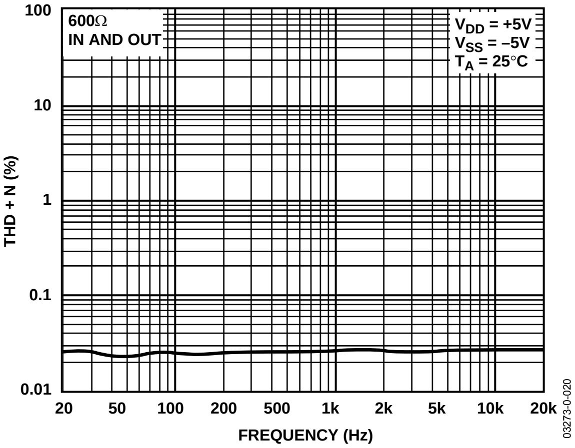


Figure 18. THD + Noise

TEST CIRCUITS

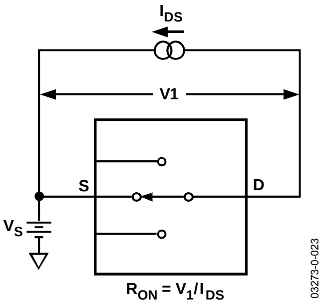


Figure 21. Test Circuit 1. ON Resistance

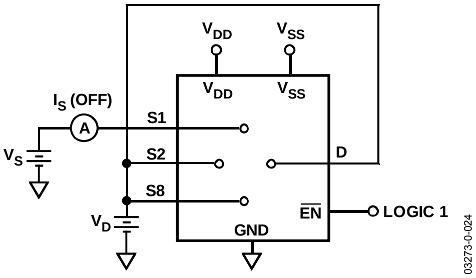


Figure 22. Test Circuit 2. I_S (OFF)

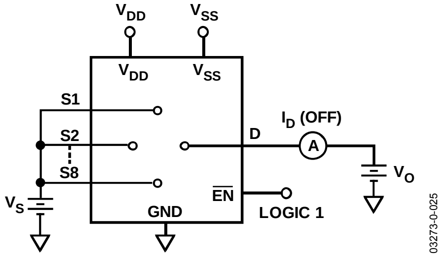


Figure 23. Test Circuit 3. I_D (OFF)

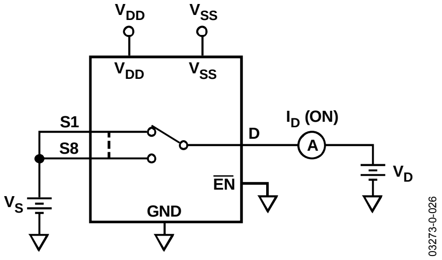
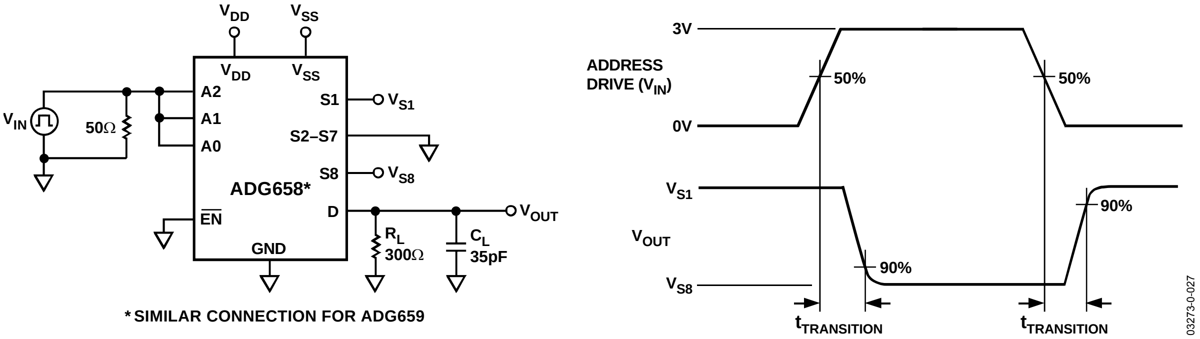


Figure 24. Test Circuit 4. I_D (ON)



*SIMILAR CONNECTION FOR ADG659

Figure 25. Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$

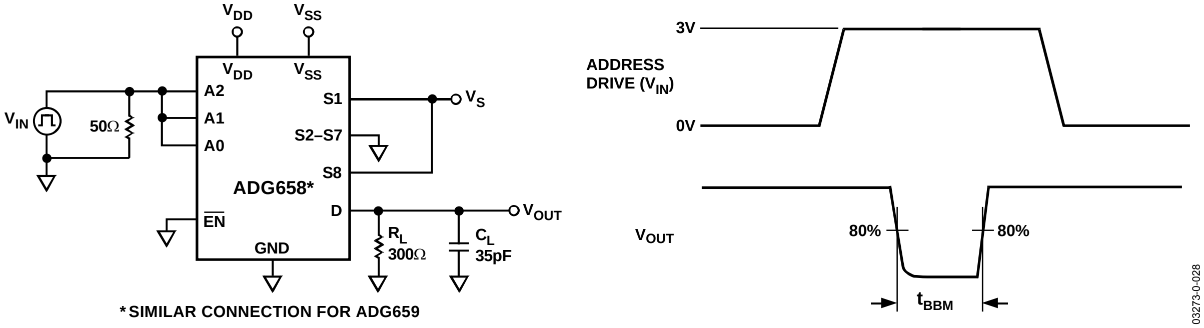


Figure 26. Test Circuit 6. Break-Before-Make Delay, t_{BBM}

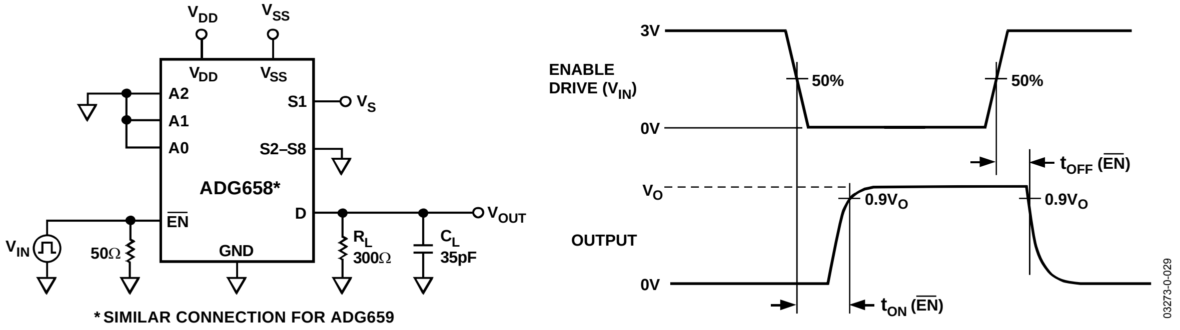


Figure 27. Test Circuit 7. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

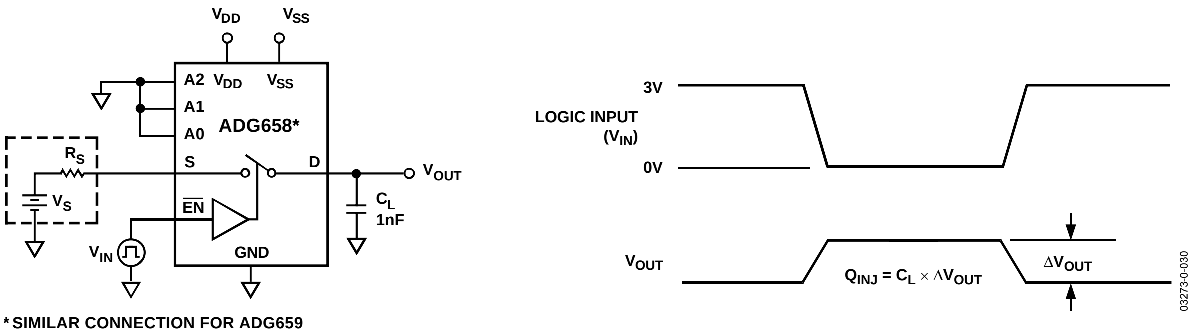


Figure 28. Test Circuit 8. Charge Injection

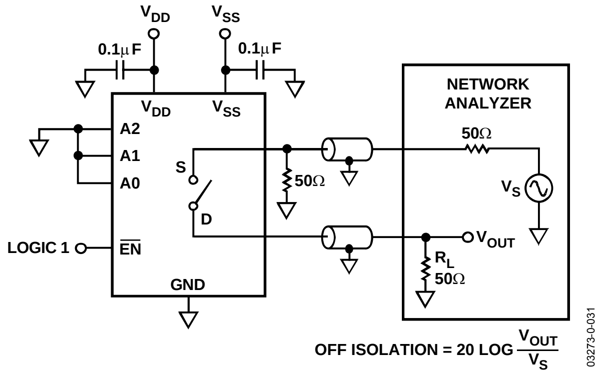


Figure 29. Test Circuit 9. Off Isolation

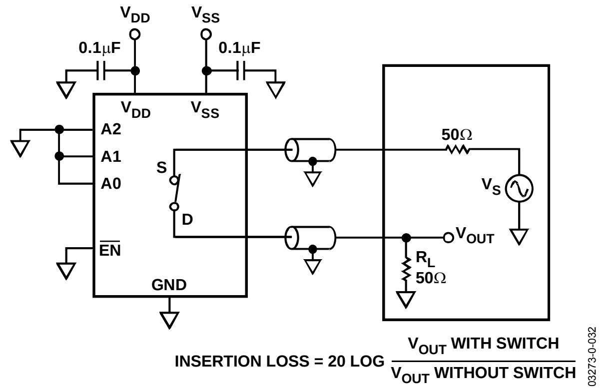


Figure 30. Test Circuit 10. Bandwidth

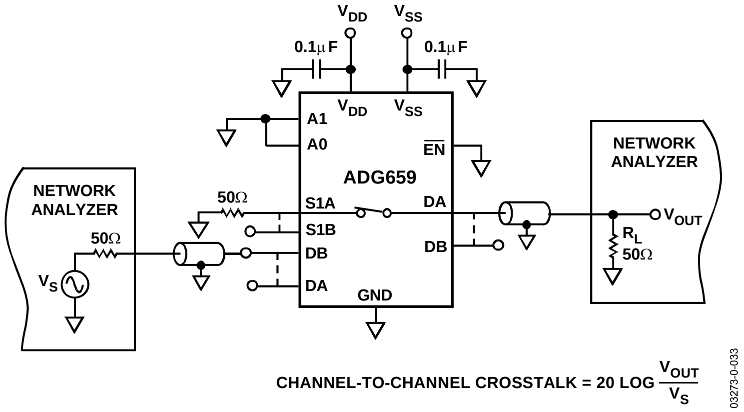
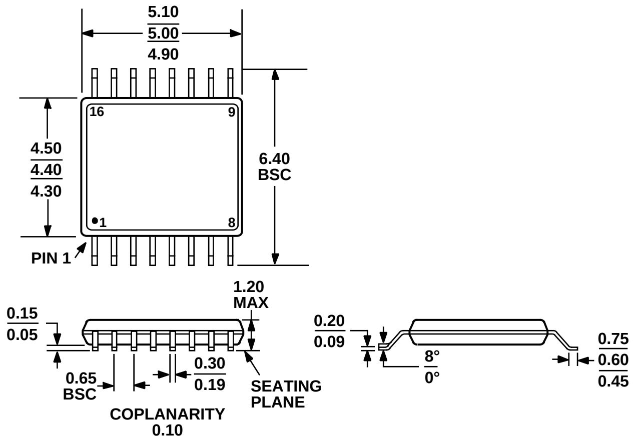


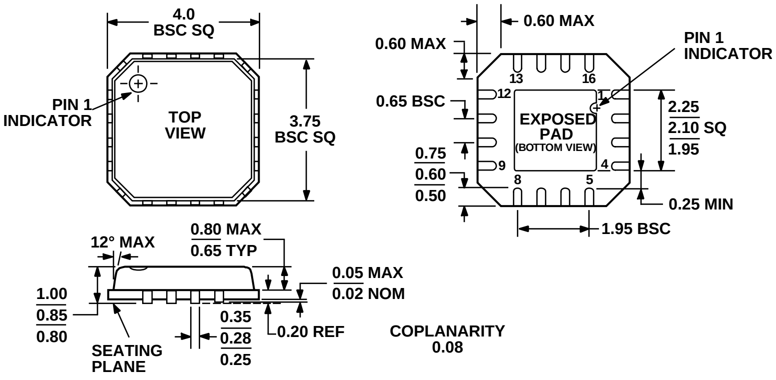
Figure 31. Test Circuit 11. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS



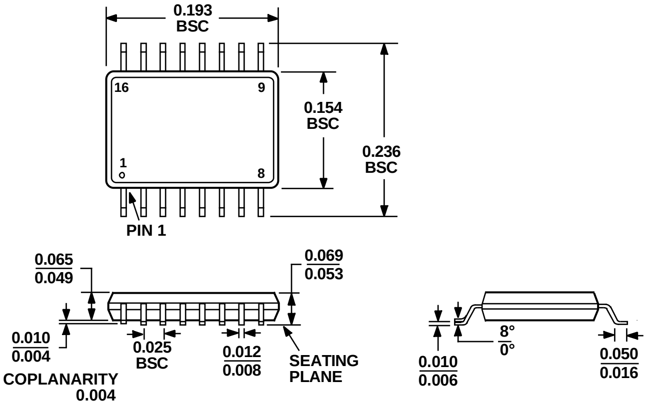
COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 32. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 33. 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16-4)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137AB

Figure 34. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG658YRU	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG658YRU-REEL7	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG658YCP	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-16
ADG658YCP-REEL7	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-16
ADG658YRQ	−40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG658YRQ-REEL	−40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG658YRQ-REEL7	−40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG659YRU	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG659YRU-REEL7	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG659YCP	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-16
ADG659YCP-REEL7	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-16
ADG659YCPZ[1]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-16
ADG659YCPZ-REEL7[1]	−40°C to +85°C	Lead Frame Chip Scale Package (LFCSP)	CP-16
ADG659YRQ	−40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG659YRQ-REEL	−40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16
ADG659YRQ-REEL7	−40°C to +125°C	Shrink Small Outline Package (QSOP)	RQ-16

[1] Z = Pb-free part.

C03273-0-7/04(A)