ANALOG DEVICES

8-/10-/12-/14-Bit, 175 MSPS TxDAC® D/A Converters

AD9704/AD9705/AD9706/AD9707

FEATURES

Pin-compatible family
Low power member of pin-compatible TxDAC product family
Power dissipation @ 3.3 V
- **22 mW @ 10 MSPS**
- **25 mW @ 25 MSPS**
- **30 mW @ 50 MSPS**

Sleep mode: 3.1 mW @ 3.3 V
Supply voltage: 1.7 V to 3.6 V
SFDR to Nyquist
- **AD9707: 84 dBc @ 5 MHz output**
- **AD9707: 83 dBc @ 10 MHz output**
- **AD9707: 75 dBc @ 20 MHz output**

AD9707 NSD @ 10 MHz output, 125 MSPS: −147 dBc/Hz
Differential current outputs: 1 mA to 5 mA
Data format: twos complement or straight binary
On-chip 1.0 V reference
CMOS-compatible digital interface
Edge-triggered latches
Clock input: single-ended and differential
Output common mode: adjustable 0 V to 1.2 V
Power-down mode < 2 mW @ 3.3 V (SPI® controllable)
Serial peripheral interface (SPI)
Self-calibration
32-lead LFCSP_VQ, Pb-free package

FUNCTIONAL BLOCK DIAGRAM

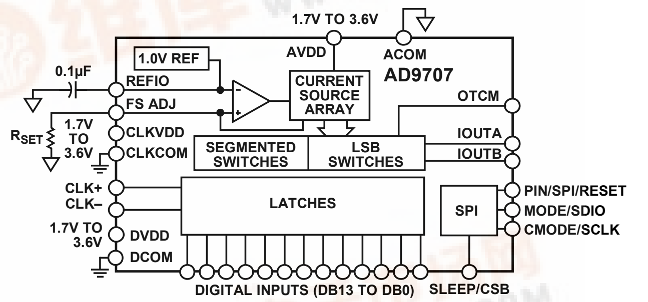


Figure 1. AD9707

PRODUCT HIGHLIGHTS

1. Pin Compatible. The AD970x line of TxDACs is pin-compatible with the AD974x TxDAC line (LFCSP_VQ package).
2. Low Power. Complete CMOS DAC operates on a single supply of 3.6 V down to 1.7 V, consuming 25 mW (3.3 V) and 10 mW (1.8 V). The DAC full-scale current can be reduced for lower power operation, and sleep and power-down modes are provided for low power idle periods.
3. Self-calibration. Self-calibration enables true 14-bit INL and DNL performance in the AD9707.
4. Twos Complement/Binary Data Coding Support. Data input supports twos complement or straight binary data coding.
5. CMOS Clock Input. High speed, single-ended, and differential CMOS clock input supports 175 MSPS conversion rate.
6. SPI Control. SPI control offers a higher level of programmability.
7. Easy Interfacing to Other Components. Adjustable output common mode from 0 V to 1.2 V allows for easy interfacing to other components that accept common-mode levels greater than 0 V.
8. On-Chip Voltage Reference. The AD970x includes a 1.0 V temperature-compensated band gap voltage reference.
9. Industry-Standard 32-Lead LFCSP_VQ Package.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

7/06—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9704/AD9705/AD9706/AD9707 are the fourth-generation family in the TxDAC series of high performance, CMOS digital-to-analog converters (DACs). This pin-compatible, 8–/10–/12–/14–bit resolution family is optimized for low power operation, while maintaining excellent dynamic performance. The AD970x family is pin-compatible with the AD9748/AD9740/AD9742/AD9744 family of TxDAC converters and is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface, LFCSP_VQ package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost. The AD970x offers exceptional ac and dc performance, while supporting update rates up to 175 MSPS.

The flexible power supply operating range of 1.7 V to 3.6 V and low power dissipation of the AD970x parts make them well-suited for portable and low power applications.

Power dissipation of the AD970x can be reduced to 15 mW, with a small trade-off in performance, by lowering the full-scale current output. In addition, a power-down mode reduces the standby power dissipation to approximately 2.2 mW.

The AD970x has an optional serial peripheral interface (SPI) that provides a higher level of programmability to enhance performance of the DAC. An adjustable output, common-mode feature allows for easy interfacing to other components that require common modes greater than 0 V.

Edge-triggered input latches and a 1.0 V temperature-compensated band gap reference have been integrated to provide a complete, monolithic DAC solution. The digital inputs support 1.8 V and 3.3 V CMOS logic families.

SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

Table 1.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	14			12			10			8			Bits
DC ACCURACY[1]													
Integral Nonlinearity (INL) Precalibration		±1.4	±6.0		±0.41	±1.48		±0.10	±0.36		±0.03	±0.09	LSB
Integral Nonlinearity (INL) Postcalibration		±0.9			±0.30			±0.10					LSB
Differential Nonlinearity (DNL) Precalibration		±1.2	±4.4		±0.35	±1.17		±0.09	±0.31		±0.02	±0.08	LSB
Differential Nonlinearity (DNL) Postcalibration		±0.4			±0.13			±0.03					LSB
ANALOG OUTPUT													
Offset Error	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	% of FSR
Gain Error (With External Reference)	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	% of FSR
Gain Error (With Internal Reference)	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	−2.7	−0.1	+2.7	% of FSR
Full-Scale Output Current[2]	1	2	5	1	2	5	1	2	5	1	2	5	mA
Output Compliance Range (From OTCM to IOUTA/IOUTB)	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	V
Output Resistance		200			200			200			200		MΩ
Output Capacitance		5			5			5			5		pF
REFERENCE OUTPUT													
Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Reference Output Current[3]		100			100			100			100		nA
REFERENCE INPUT													
Input Compliance Range	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
Reference Input Resistance (Reference Powered Up)		10			10			10			10		kΩ
Reference Input Resistance (Reference Powered Down)		1			1			1			1		MΩ
Small Signal Bandwidth		0.5			0.5			0.5			0.5		MHz
TEMPERATURE COEFFICIENTS													
Offset Drift		0			0			0			0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±29			±29			±29			±29		ppm of FSR/°C
Gain Drift (With Internal Reference)		±40			±40			±40			±40		ppm of FSR/°C
Reference Voltage Drift		±25			±25			±25			±25		ppm/°C
POWER SUPPLY													
Supply Voltages													
AVDD		3.3	3.6		3.3	3.6		3.3	3.6		3.3	3.6	V
DVDD		3.3	3.6		3.3	3.6		3.3	3.6		3.3	3.6	V
CLKVDD		3.3	3.6		3.3	3.6		3.3	3.6		3.3	3.6	V
Analog Supply Current (I_{AVDD})		5.2	6.7		5.2	6.7		5.1	6.7		5.1	6.7	mA
Digital Supply Current (I_{DVDD})[4]		5.9	6.6		5.4	6.6		5.0	6.6		4.6	6.6	mA
Clock Supply Current (I_{CLKVDD})[4]		4.1	4.7		4.1	4.7		4.1	4.7		4.1	4.7	mA
Power Dissipation[4]		50.2	57		48.5	57		46.9	57		45.5	57	mW
Supply Current Sleep Mode (I_{AVDD})		0.37	0.4		0.37	0.4		0.37	0.4		0.37	0.4	mA
Supply Current Power-Down Mode (I_{AVDD})		0.7	7.5		0.7	7.5		0.7			0.7	7.5	μA

Parameter	AD9707			AD9706			AD9705			AD9704			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Current Clock Power-Down Mode (I_{DVDD})[5]		0.6	1		0.6	1		0.6	1		0.6	1	mA
Supply Current Clock Power-Down Mode (I_{CLKVDD})		42.5	58		42.5	58		42.5	58		42.5	58	µA
Power Supply Rejection Ratio (AVDD)[6]	−0.2	+0.03	+0.2	−0.2	+0.03	+0.2	−0.2	+0.03	+0.2	−0.2	+0.03	+0.2	% of FSR/V
OPERATING RANGE	−40		+85	−40		+85	−40		+85	−40		+85	°C

[1] Measured at IOUTA, driving a virtual ground, at 25°C only.
[2] Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3] An external buffer amplifier with input bias current < 100 nA should be used to drive any external load.
[4] Measured at f_{CLOCK} = 175 MSPS and f_{OUT} = 1.0 MHz, using differential clock.
[5] Measured at f_{CLOCK} = 100 MSPS and f_{OUT} = 1.0 MHz, using differential clock.
[6] ±5% power supply variation.

DYNAMIC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, differential transformer coupled output, 453 Ω differentially terminated,[1] unless otherwise noted.

Table 2.

Parameter	AD9707			AD9706			AD9705			AD9704			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE													
Maximum Output Update Rate (f_{CLOCK})	175			175			175			175			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[2]		11			11			11			11		ns
Output Propagation Delay (t_{PD})		4			4			4			4		ns
Glitch Impulse		5			5			5			5		pV-s
Output Rise Time (10% to 90%)[2]		2.5			2.5			2.5			2.5		ns
Output Fall Time (10% to 90%)[2]		2.5			2.5			2.5			2.5		ns
AC LINEARITY													
Spurious-Free Dynamic Range to Nyquist													
f_{CLOCK} = 10 MSPS; f_{OUT} = 2.1 MHz		84			84			84			70		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 2.1 MHz		84			83			84			68		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 5.1 MHz		84			84			84			70		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10.1 MHz		83			83			83			71		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 1.0 MHz	74	83		72	82		72	82		66	70		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 15.1 MHz		78			78			78			68		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 25.1 MHz		77			77			76			69		dBc
f_{CLOCK} = 175 MSPS; f_{OUT} = 20.1 MHz		75			75			75			69		dBc
f_{CLOCK} = 175 MSPS; f_{OUT} = 40.1 MHz		72			71			71			67		dBc
Noise Spectral Density													
f_{CLOCK} = 175 MSPS; f_{OUT} = 6.0 MHz; I_{OUTFS} = 2 mA		−149			−146			−137			−127		dBc/Hz
ENOB at I_{OUTFS} = 2 mA		11.3			10.9			9.5			8.0		bits
f_{CLOCK} = 175 MSPS; f_{OUT} = 6.0 MHz; I_{OUTFS} = 5 mA		−157											dBc/Hz
ENOB at I_{OUTFS} = 5 mA		12.5											bits
f_{CLOCK} = 175 MSPS; f_{OUT} = 6.0 MHz; I_{OUTFS} = 1 mA		−145											dBc/Hz
ENOB at I_{OUTFS} = 1 mA		10.6											bits

[1] See Figure 71 for diagram.
[2] Measured single-ended into 500 Ω load.

DIGITAL SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

Table 3.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIGITAL INPUTS[1]													
Logic 1 Voltage	2.1	3		2.1	3		2.1	3		2.1	3		V
Logic 0 Voltage		0	0.9		0	0.9		0	0.9		0	0.9	V
Logic 1 Current	−10		+10	−10		+10	−10		+10	−10		+10	µA
Logic 0 Current			10			10			10			10	µA
Input Capacitance		5			5			5			5		pF
Input Setup Time (t_S)		1.3			1.3			1.3			1.3		ns
Input Hold Time (t_H)		0.7			0.7			0.7			0.7		ns
Latch Pulsewidth (t_{LPW})		2.8			2.8			2.8			2.8		ns
CLK INPUTS[2]													
Input Voltage Range	0		3	0		3	0		3	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	0.75	1.5	2.25	0.75	1.5	2.25	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		0.5	1.5		0.5	1.5		0.5	1.5		V

[1] Includes CLK+ pin in single-ended clock input mode.
[2] Applicable to CLK+ input and CLK– input when configured for differential clock input mode.

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 2 mA, unless otherwise noted.

Table 4.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	14			12			10			8			Bits
DC ACCURACY[1]													
Integral Nonlinearity (INL) Precalibration		±1.4	±6.03		±0.42	±1.50		±0.10	±0.36		±0.03	±0.09	LSB
Differential Nonlinearity (DNL) Precalibration		±1.2	±4.34		±0.36	±1.17		±0.09	±0.30		±0.02	±0.07	LSB
ANALOG OUTPUT													
Offset Error	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	−0.03	0	+0.03	% of FSR
Gain Error (With Internal Reference)	−2.7	−0.2	+2.7	−2.7	−0.2	+2.7	−2.7	−0.2	+2.7	−2.7	−0.2	+2.7	% of FSR
Full-Scale Output Current[2]	1	2	5	1	2	5	1	2	5	1	2	5	mA
Output Compliance Range (With OTCM = AGND)	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	−0.8		+0.8	V
Output Resistance		200			200			200			200		MΩ
Output Capacitance		5			5			5			5		pF
REFERENCE OUTPUT													
Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Reference Output Current[3]		100			100			100			100		nA
REFERENCE INPUT													
Input Compliance Range	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
Reference Input Resistance (Reference Powered Up)		10			10			10			10		kΩ
Reference Input Resistance (External Reference)		1			1			1			1		MΩ
Small Signal Bandwidth		0.5			0.5			0.5			0.5		MHz
TEMPERATURE COEFFICIENTS													
Offset Drift		0			0			0			0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±30			±30			±30			±30		ppm of FSR/°C
Gain Drift (With Internal Reference)		±60			±60			±60			±60		ppm of FSR/°C
Reference Voltage Drift		±25			±25			±25			±25		ppm/°C
POWER SUPPLY													
Supply Voltages													
AVDD	1.7	1.8		1.7	1.8		1.7	1.8		1.7	1.8		V
DVDD	1.7	1.8		1.7	1.8		1.7	1.8		1.7	1.8		V
CLKVDD	1.7	1.8		1.7	1.8		1.7	1.8		1.7	1.8		V
Analog Supply Current (I_{AVDD})		3.8	4.8		3.8	4.8		3.8	4.8		3.8	4.8	mA
Digital Supply Current (I_{DVDD})[4]		1.3	1.5		1.2	1.5		1.1	1.5		1.0	1.5	mA
Clock Supply Current (I_{CLKVDD})[4]		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5	mA
Power Dissipation[4]		11.5	13.2		11.3	13.2		11.1	13.2		11.0	13.2	mW
Supply Current Sleep Mode (I_{AVDD})		0.3	0.4		0.3	0.4		0.3	0.4		0.3	0.4	mA
Supply Current Power-Down Mode (I_{AVDD})		5	6		5	6		5	6		5	6	μA
Supply Current Power-Down Mode (I_{AVDD})		0.2	0.3		0.2	0.3		0.2	0.3		0.2	0.3	mA

Parameter	AD9707 Min	AD9707 Typ	AD9707 Max	AD9706 Min	AD9706 Typ	AD9706 Max	AD9705 Min	AD9705 Typ	AD9705 Max	AD9704 Min	AD9704 Typ	AD9704 Max	Unit
Supply Current Clock Power-Down Mode (I_{DVDD})[4]		0.22	0.28		0.22	0.28		0.22	0.28		0.22	0.28	mA
Supply Current Clock Power-Down Mode (I_{CLKVDD})[4]		9.5	16		9.5	16		9.5	16		9.5	16	μA
Power Supply Rejection Ratio (AVDD)[5]	−1	−0.1	+1	−1	−0.1	+1	−1	−0.1	+1	−1	−0.1	+1	% of FSR/V
OPERATING RANGE	−40		+85	−40		+85	−40		+85	−40		+85	°C

[1] Measured at IOUTA, driving a virtual ground, at 25°C only.
[2] Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3] An external buffer amplifier with input bias current < 100 nA should be used to drive any external load.
[4] Measured at f_{CLOCK} = 80 MSPS and f_{OUT} = 1 MHz, using differential clock.
[5] ±5% power supply variation, I_{OUTFS} = 1 mA, at 25°C only.

DYNAMIC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, differential transformer coupled output, 453 Ω differentially terminated,[1] unless otherwise noted.

Table 5.

Parameter	AD9707 Min	AD9707 Typ	AD9707 Max	AD9706 Min	AD9706 Typ	AD9706 Max	AD9705 Min	AD9705 Typ	AD9705 Max	AD9704 Min	AD9704 Typ	AD9704 Max	Unit
DYNAMIC PERFORMANCE													
Maximum Output Update Rate (f_{CLOCK})	80			80			80			80			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[2]		11			11			11			11		ns
Output Propagation Delay (t_{PD})		5.6			5.6			5.6			5.6		ns
Glitch Impulse		5			5			5			5		pV-s
Output Rise Time (10% to 90%)[2]		2.5			2.5			2.5			2.5		ns
Output Fall Time (10% to 90%)[2]		2.5			2.5			2.5			2.5		ns
AC LINEARITY													
Spurious-Free Dynamic Range to Nyquist													
f_{CLOCK} = 10 MSPS; f_{OUT} = 2.1 MHz		86			86			85			70		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 2.1 MHz		87			86			84			68		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 5.1 MHz		82			82			82			68		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10.1 MHz		82			79			78			70		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 15.1 MHz		77			76			74			69		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 1.0 MHz	74	82		72	82		72	82		66	70		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 15.1 MHz		77			77			77			68		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 30.1 MHz		60			59			59			60		dBc
Noise Spectral Density													
f_{CLOCK} = 80 MSPS; f_{OUT} = 10 MHz; I_{OUTFS} = 1 mA		−141.0			−139.4			−135.1			−126.3		dBc/Hz
ENOB at I_{OUTFS} = 1 mA		10.5			10.2			9.5			8.0		bits
f_{CLOCK} = 80 MSPS; f_{OUT} = 10 MHz; I_{OUTFS} = 2 mA		−145.7											dBc/Hz
ENOB at I_{OUTFS} = 2 mA		10.3											Bits

[1] See Figure 71 for diagram.
[2] Measured single-ended into 500 Ω load.

DIGITAL SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.

Table 6.

	AD9707			AD9706			AD9705			AD9704			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIGITAL INPUTS[1]													
Logic 1 Voltage	1.2	1.8		1.2	1.8		1.2	1.8		1.2	1.8		V
Logic 0 Voltage		0	0.5		0	0.5		0	0.5		0	0.5	V
Logic 1 Current	−10		+10	−10		+10	−10		+10	−10		+10	μA
Logic 0 Current			+10			+10			+10			+10	μA
Input Capacitance		5			5			5			5		pF
Input Setup Time (t_S)		2.4			2.4			2.4			2.4		ns
Input Hold Time (t_H)		0.4			0.4			0.4			0.4		ns
Latch Pulsewidth (t_{LPW})		6.2			6.2			6.2			6.2		ns
CLK INPUTS[2]													
Input Voltage Range	0		1.8	0		1.8	0		1.8	0		1.8	V
Common-Mode Voltage	0.4	0.9	1.3	0.4	0.9	1.3	0.4	0.9	1.3	0.4	0.9	1.3	V
Differential Voltage	0.5	1.5		0.5	1.5		0.5	1.5		0.5	1.5		V

[1] Includes CLK+ pin in single-ended clock input mode.
[2] Applicable to CLK+ input and CLK– input when configured for differential clock input mode.

TIMING DIAGRAM

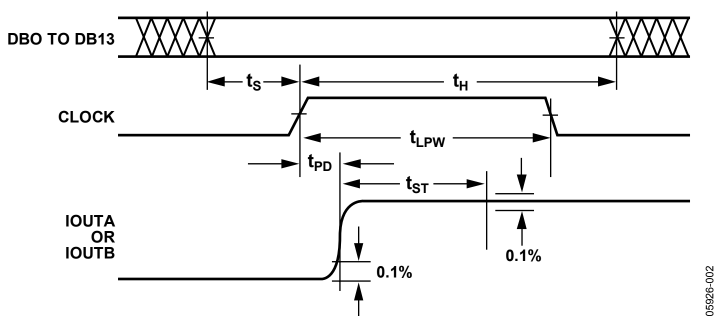


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	With Respect to	Rating
AVDD	ACOM	−0.3 V to +3.9 V
DVDD	DCOM	−0.3 V to +3.9 V
CLKVDD	CLKCOM	−0.3 V to +3.9 V
ACOM	DCOM	−0.3 V to +0.3 V
ACOM	CLKCOM	−0.3 V to +0.3 V
DCOM	CLKCOM	−0.3 V to +0.3 V
AVDD	DVDD	−3.9 V to +3.9 V
AVDD	CLKVDD	−3.9 V to +3.9 V
DVDD	CLKVDD	−3.9 V to +3.9 V
CLOCK, SLEEP	DCOM	−0.3 V to DVDD + 0.3 V
Digital Inputs, MODE	DCOM	−0.3 V to DVDD + 0.3 V
IOUTA, IOUTB	ACOM	−1.0 V to AVDD + 0.3 V
REFIO, REFLO, FS ADJ, OTCM	ACOM	−0.3 V to AVDD + 0.3 V
CLK+, CLK−, CMODE	CLKCOM	−0.3 V to CLKVDD + 0.3 V
Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS[1]

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead LFCSP_VQ	32.5	°C/W

[1] Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

AD9707

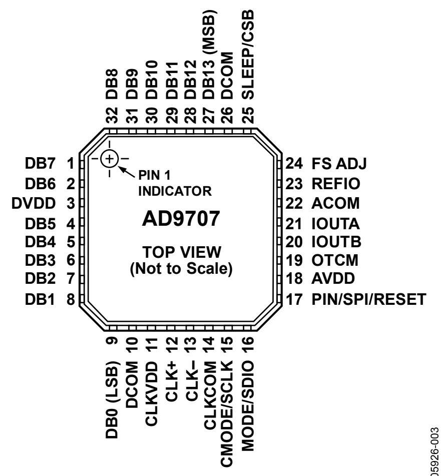


Figure 3. AD9707 Pin Configuration

Table 9. AD9707 Pin Function Descriptions

Pin No.	Mnemonic	Description
27	DB13 (MSB)	Most Significant Data Bit (MSB).
28 to 32, 1, 2, 4 to 8	DB12 to DB1	Data Bit 12 to Data Bit 1.
9	DB0 (LSB)	Least Significant Data Bit (LSB).
25	SLEEP/CSB	In pin mode, active high powers down chip.
		In SPI mode, this pin is the serial port chip select (active low).
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference activated. Requires a 0.1 μF capacitor to ACOM when internal reference activated.
24	FS ADJ	Full-Scale Current Output Adjust.
22	ACOM	Analog Common.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
17	PIN/SPI/RESET	Selects SPI mode or pin mode operation. Active high for pin mode operation. Active low for SPI mode operation. Pulse high to reset SPI registers to default values.
16	MODE/SDIO	In pin mode, this selects the input data format. Connect to DCOM for straight binary, DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
14	CLKCOM	Clock Common.
13	CLK–	Differential Clock Input.
12	CLK+	Differential Clock Input.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
10, 26	DCOM	Digital Common.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).

AD9706

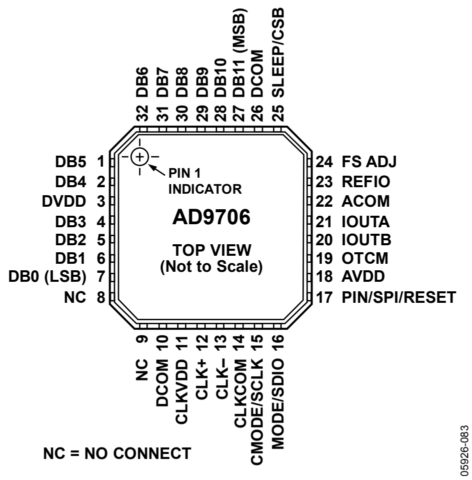


Figure 4. AD9706 Pin Configuration

Table 10. AD9706 Pin Function Descriptions

Pin No.	Mnemonic	Description
27	DB11 (MSB)	Most Significant Data Bit (MSB).
28 to 32, 1, 2, 4 to 6	DB10 to DB1	Data Bit 10 to Data Bit 1.
7	DB0 (LSB)	Least Significant Data Bit (LSB).
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
24	FS ADJ	Full-Scale Current Output Adjust.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference activated. Requires a 0.1 μF capacitor to ACOM when internal reference activated.
22	ACOM	Analog Common.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
17	PIN/SPI/RESET	Selects SPI mode or pin mode operation. Active high for pin mode operation. Active low for SPI mode operation. Pulse high to reset SPI registers to default values.
16	MODE/SDIO	In pin mode, this selects the input data format. Connect to DCOM for straight binary, DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
14	CLKCOM	Clock Common.
13	CLK–	Differential Clock Input.
12	CLK+	Differential Clock Input.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
10, 26	DCOM	Digital Common.
8, 9	NC	No Connect.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).

AD9705

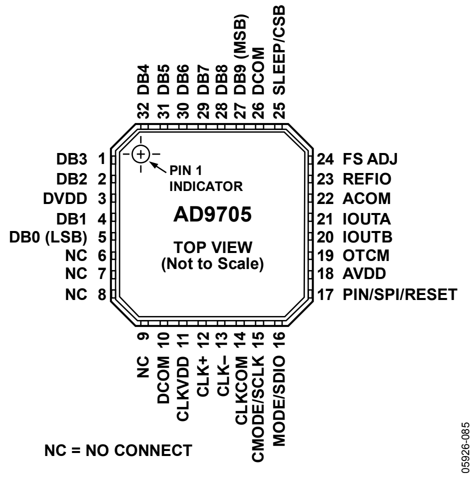


Figure 5. AD9705 Pin Configuration

Table 11. AD9705 Pin Function Descriptions

Pin No.	Mnemonic	Description
27	DB9 (MSB)	Most Significant Data Bit (MSB).
28 to 32, 1, 2, 4	DB8 to DB1	Data Bit 8 to Data Bit 1.
5	DB0 (LSB)	Least Significant Data Bit (LSB).
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
24	FS ADJ	Full-Scale Current Output Adjust.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference activated. Requires a 0.1 µF capacitor to ACOM when internal reference activated.
22	ACOM	Analog Common.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
17	PIN/SPI/RESET	Selects SPI mode or pin mode operation. Active high for pin mode operation. Active low for SPI mode operation. Pulse high to reset SPI registers to default values.
16	MODE/SDIO	In pin mode, this selects the input data format. Connect to DCOM for straight binary, DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
14	CLKCOM	Clock Common.
13	CLK–	Differential Clock Input.
12	CLK+	Differential Clock Input.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
10, 26	DCOM	Digital Common.
6 to 9	NC	No Connect.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).

AD9704

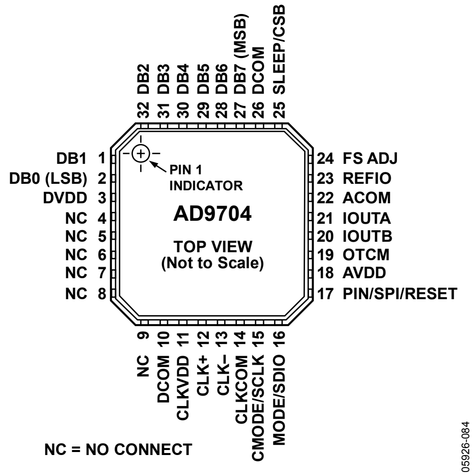


Figure 6. AD9704 Pin Configuration

Table 12. AD9704 Pin Function Descriptions

Pin No.	Mnemonic	Description
27	DB7 (MSB)	Most Significant Data Bit (MSB).
28 to 32, 1	DB6 to DB1	Data Bit 6 to Data Bit 1.
2	DB0 (LSB)	Least Significant Data Bit (LSB).
25	SLEEP/CSB	In pin mode, active high powers down chip. In SPI mode, this pin is the serial port chip select (active low).
24	FS ADJ	Full-Scale Current Output Adjust.
23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference activated. Requires a 0.1 μF capacitor to ACOM when internal reference activated.
22	ACOM	Analog Common.
21	IOUTA	DAC Current Output. Full-scale current is sourced when all data bits are 1s.
20	IOUTB	Complementary DAC Current Output. Full-scale current is sourced when all data bits are 0s.
19	OTCM	Adjustable Output Common Mode. Refer to the Theory of Operation section for details.
18	AVDD	Analog Supply Voltage (1.7 V to 3.6 V).
17	PIN/SPI/RESET	Selects SPI mode or pin mode operation. Active high for pin mode operation. Active low for SPI mode operation. Pulse high to reset SPI registers to default values.
16	MODE/SDIO	In pin mode, this selects the input data format. Connect to DCOM for straight binary, DVDD for twos complement. In SPI mode, this pin acts as SPI data input/output.
15	CMODE/SCLK	In pin mode, this pin selects the clock input type. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. In SPI mode, this pin is the serial data clock input.
14	CLKCOM	Clock Common.
13	CLK–	Differential Clock Input.
12	CLK+	Differential Clock Input.
11	CLKVDD	Clock Supply Voltage (1.7 V to 3.6 V).
10, 26	DCOM	Digital Common.
4 to 9	NC	No Connect.
3	DVDD	Digital Supply Voltage (1.7 V to 3.6 V).

TYPICAL PERFORMANCE CHARACTERISTICS

AD9707

VDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

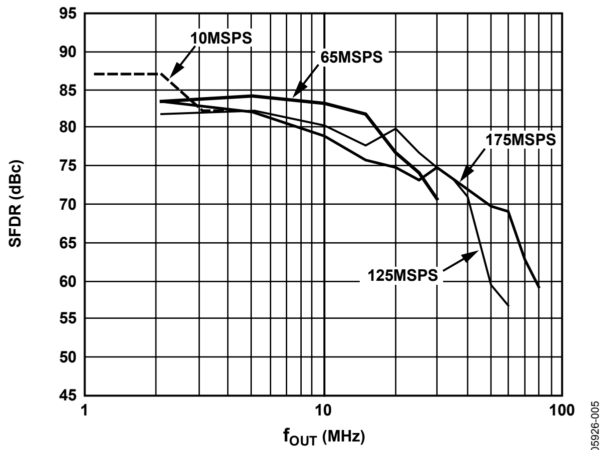


Figure 7. SFDR vs. f_{OUT}

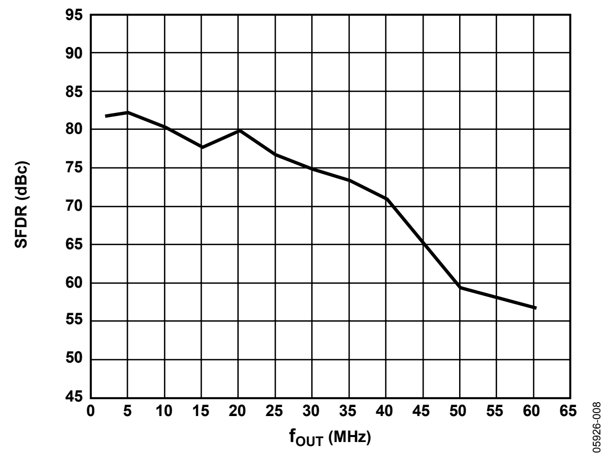


Figure 10. SFDR vs. f_{OUT} @ 125 MSPS

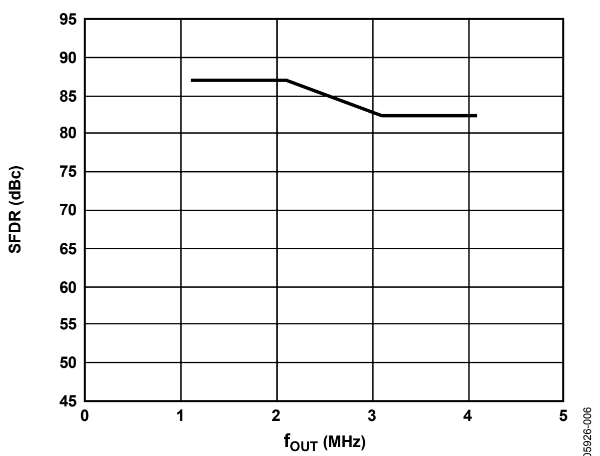


Figure 8. SFDR vs. f_{OUT} @ 10 MSPS

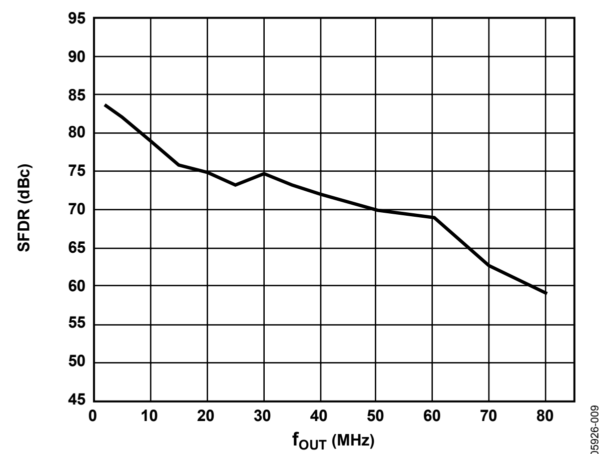


Figure 11. SFDR vs. f_{OUT} @ 175 MSPS

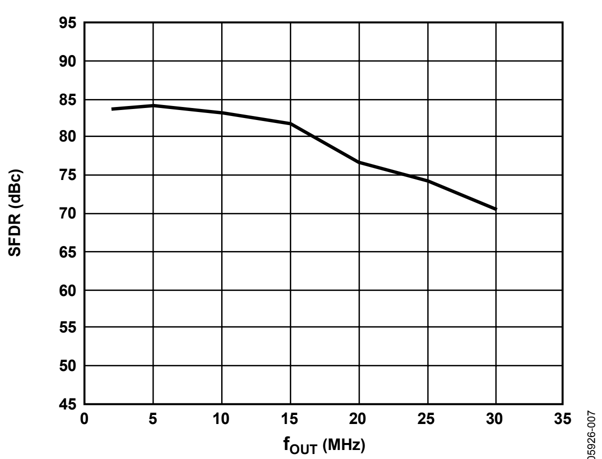


Figure 9. SFDR vs. f_{OUT} @ 65 MSPS

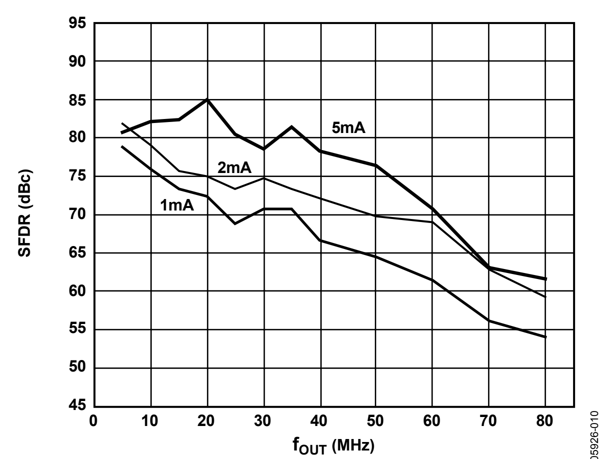


Figure 12. SFDR vs. f_{OUT} and I_{OUTFS} @ 175 MSPS

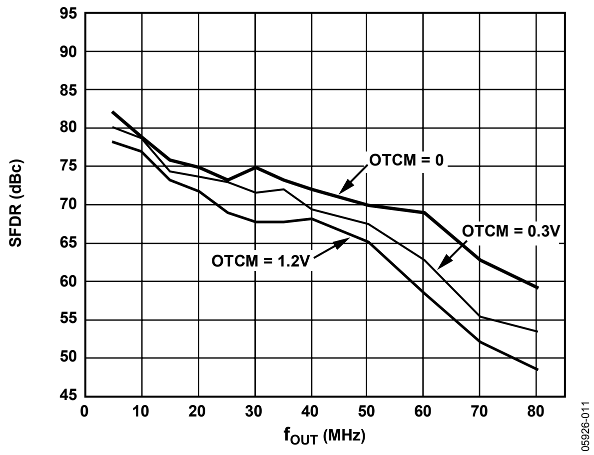


Figure 13. SFDR vs. f_{OUT} and OTCM @ 175 MSPS

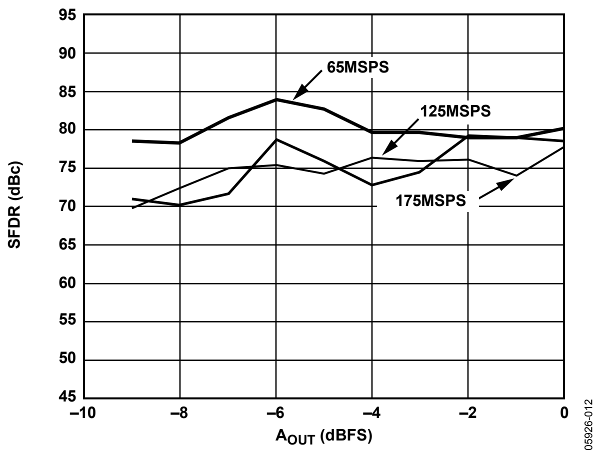


Figure 14. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

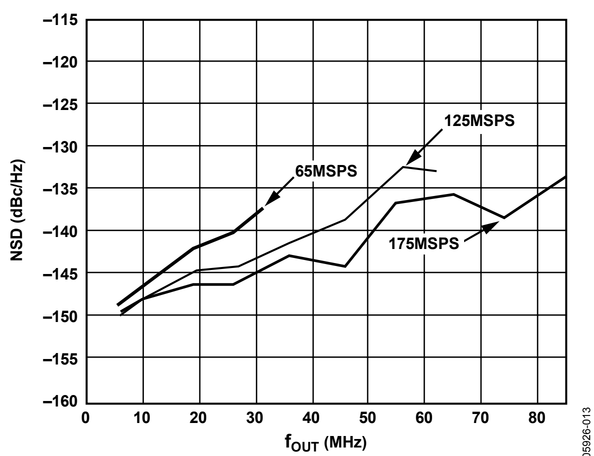


Figure 15. NSD vs. f_{OUT} and f_{CLOCK} @ 0 dBFS

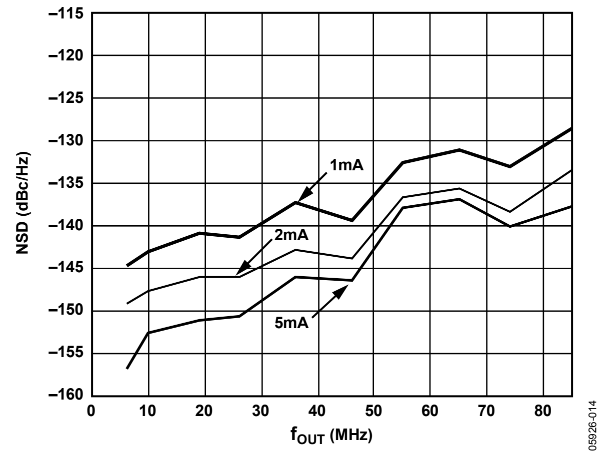


Figure 16. NSD vs. f_{OUT} and I_{OUTFS} @ 175 MSPS

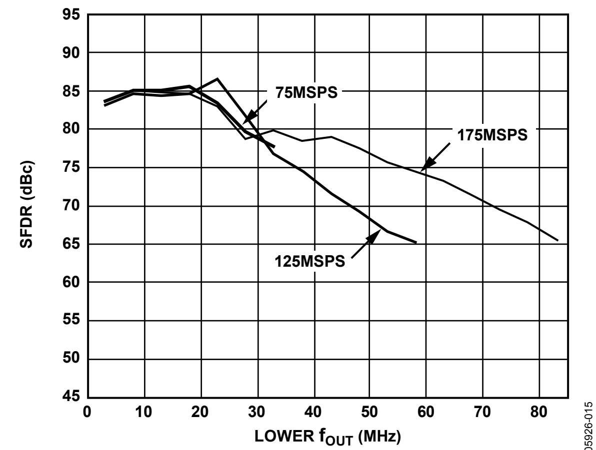


Figure 17. Dual-Tone IMD vs. f_{OUT} @ 0 dBFS

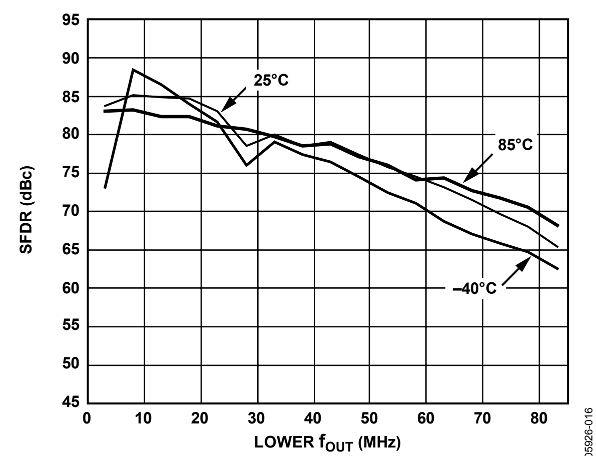


Figure 18. Dual-Tone IMD vs. f_{OUT} and Temperature @ 0 dBFS

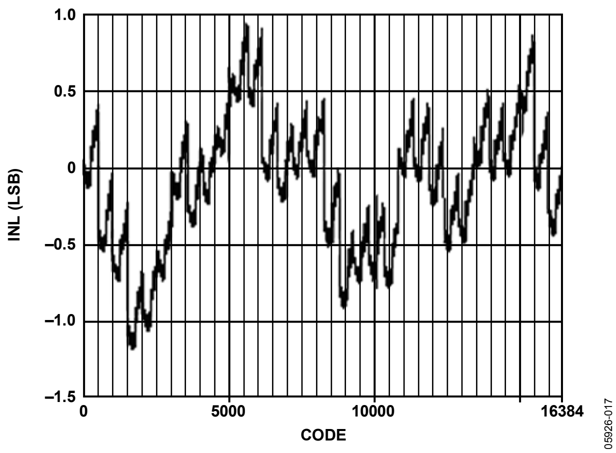


Figure 19. Typical Uncalibrated INL

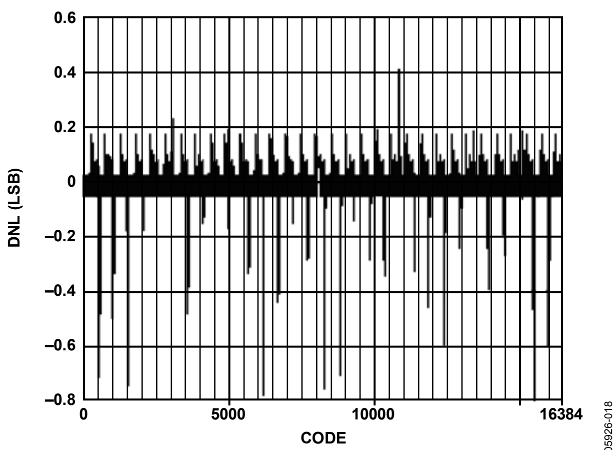


Figure 20. Typical Uncalibrated DNL

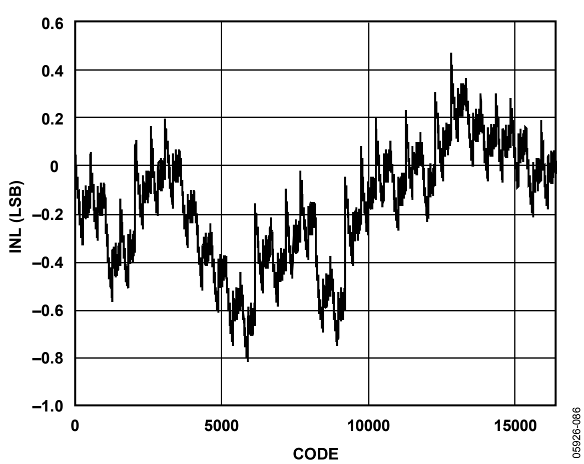


Figure 21. Typical Calibrated INL

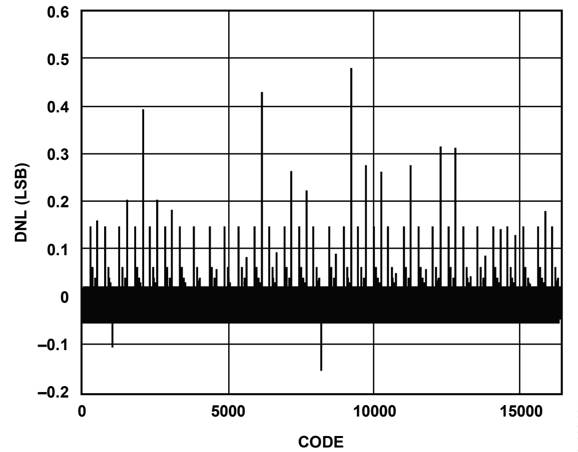


Figure 22. Typical Calibrated DNL

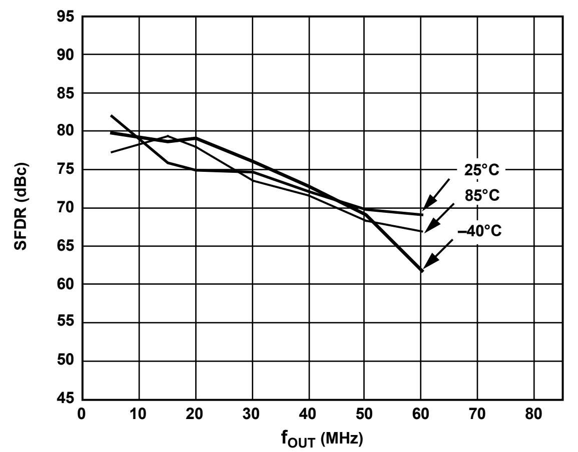


Figure 23. SFDR vs. Temperature @ 175 MSPS

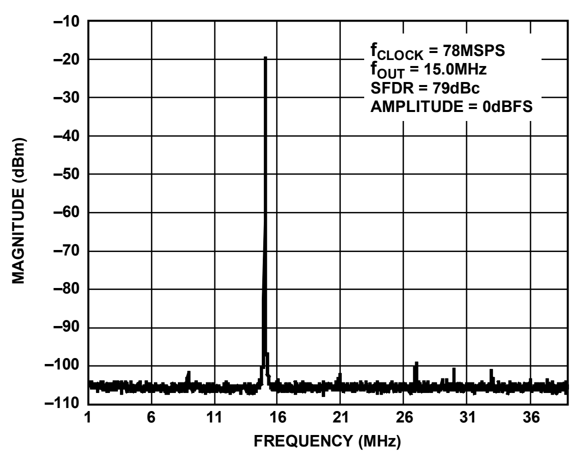


Figure 24. Single-Tone SFDR

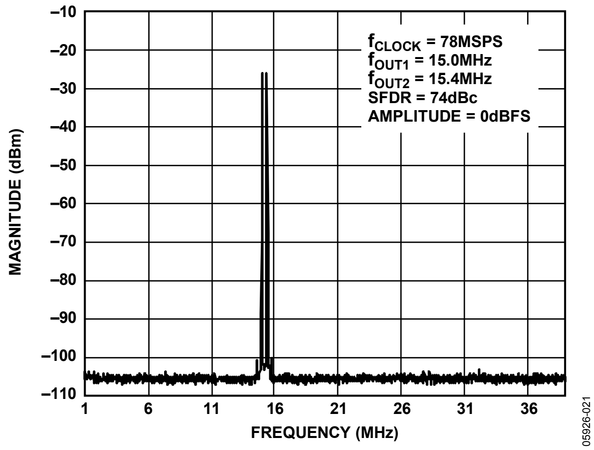


Figure 25. Dual-Tone SFDR

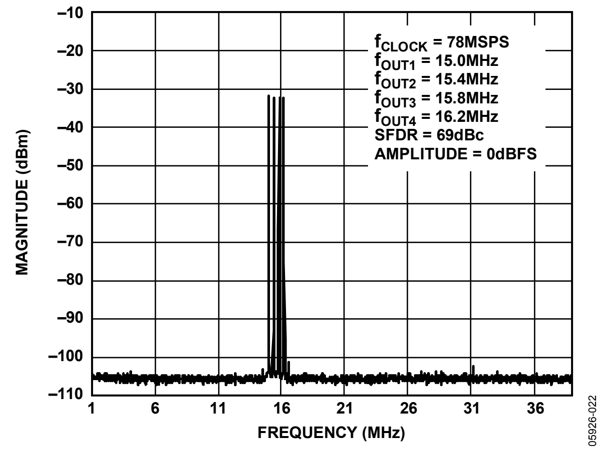


Figure 26. Four-Tone SFDR

VDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.

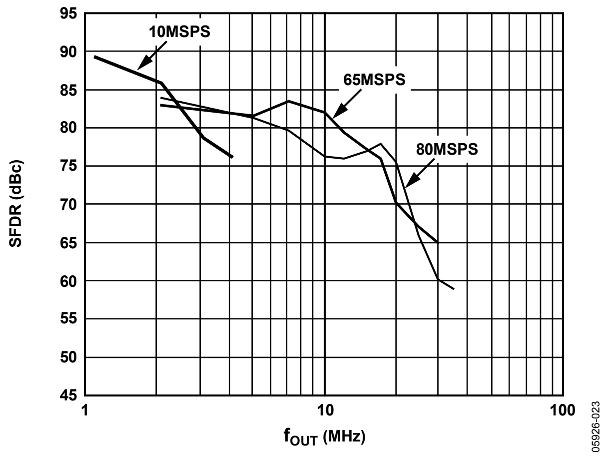


Figure 27. SFDR vs. f_{OUT}

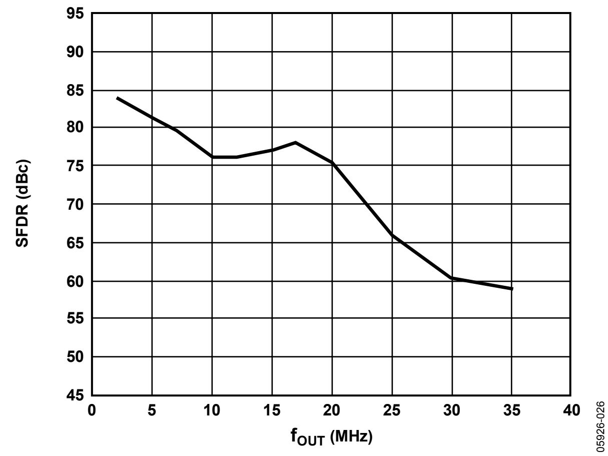


Figure 30. SFDR vs. f_{OUT} @ 80 MSPS

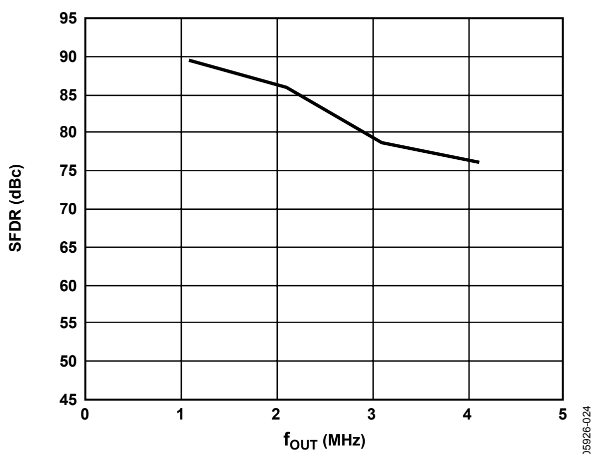


Figure 28. SFDR vs. f_{OUT} @ 10 MSPS

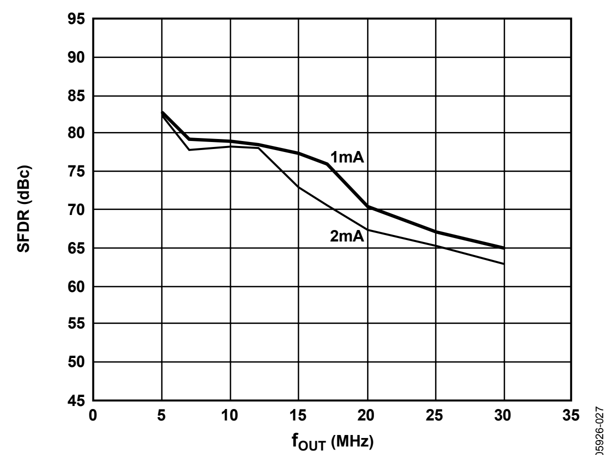


Figure 31. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS

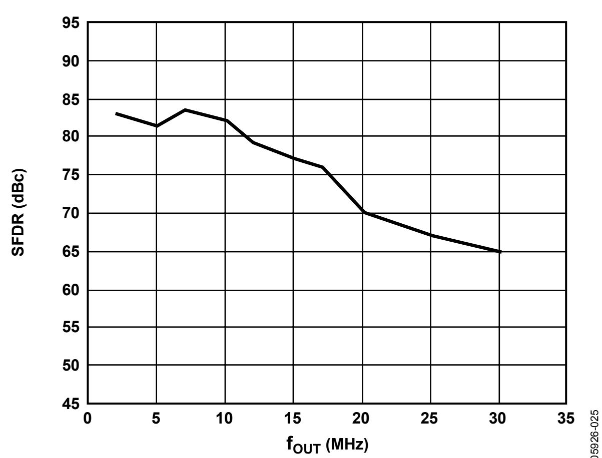


Figure 29. SFDR vs. f_{OUT} @ 65 MSPS

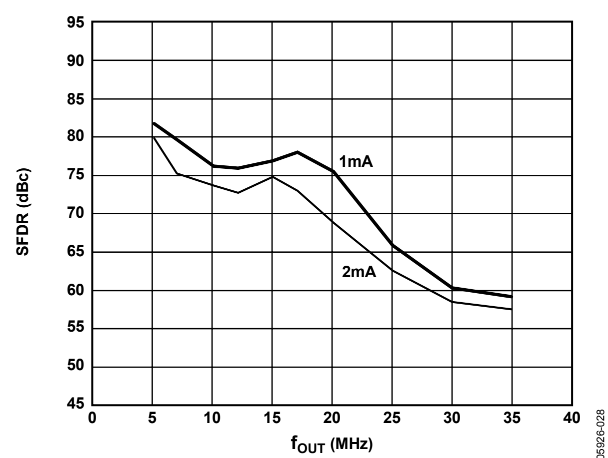


Figure 32. SFDR vs. f_{OUT} and I_{OUTFS} @ 80 MSPS

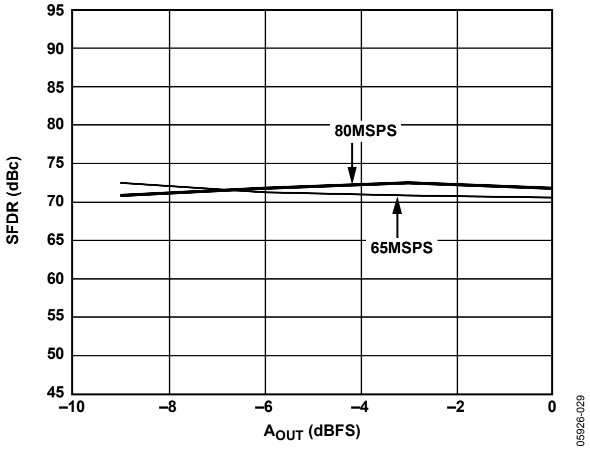


Figure 33. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

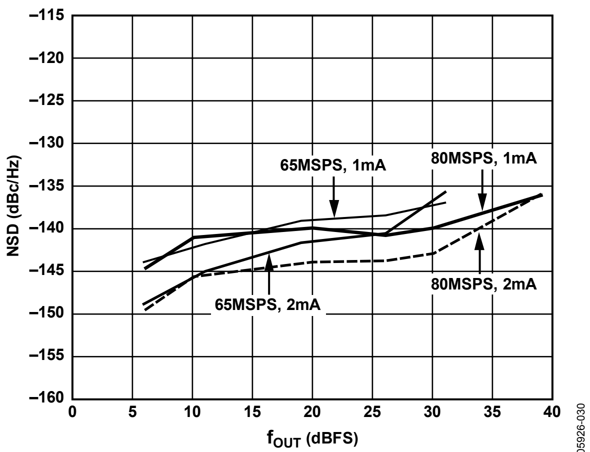


Figure 34. NSD vs. f_{OUT}, f_{CLOCK}, and I_{OUTFS} @ 0 dBFS

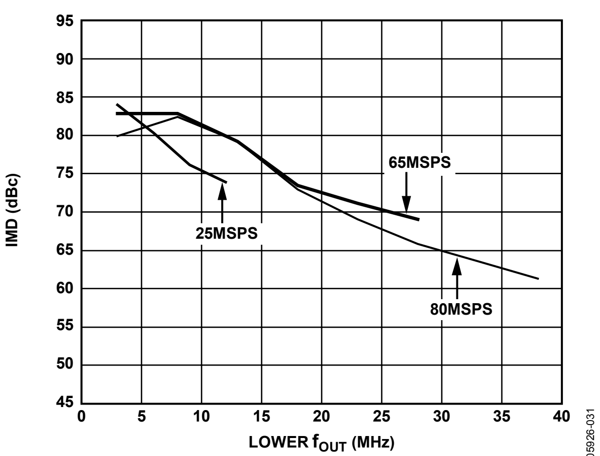


Figure 35. Dual-Tone IMD vs. f_{OUT} @ I_{OUTFS} = 1 mA and 0 dBFS

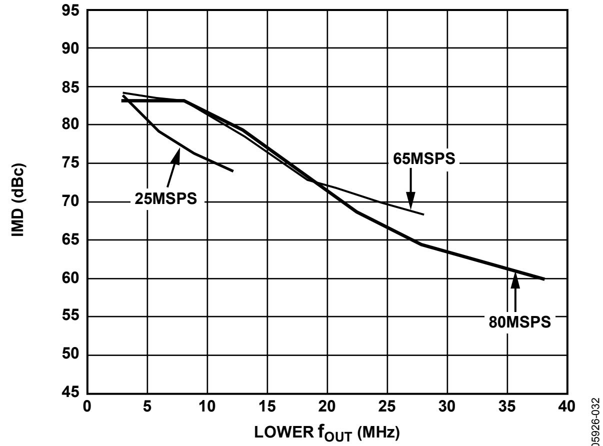


Figure 36. Dual-Tone IMD vs. f_{OUT} @ I_{OUTFS} = 2 mA and 0 dBFS

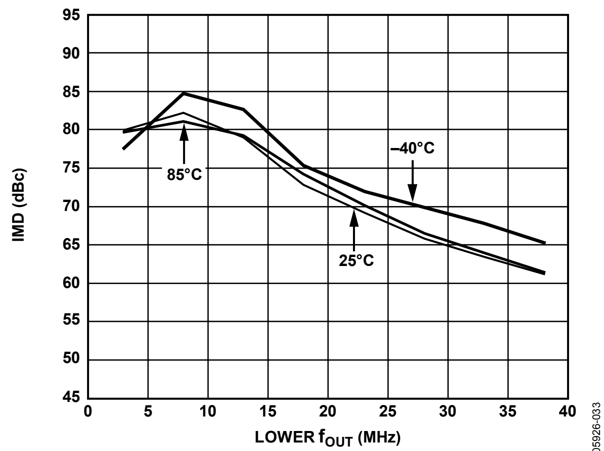


Figure 37. Dual-Tone IMD vs. f_{OUT} and Temperature @ 80 MSPS, I_{OUTFS} = 1 mA and 0 dBFS

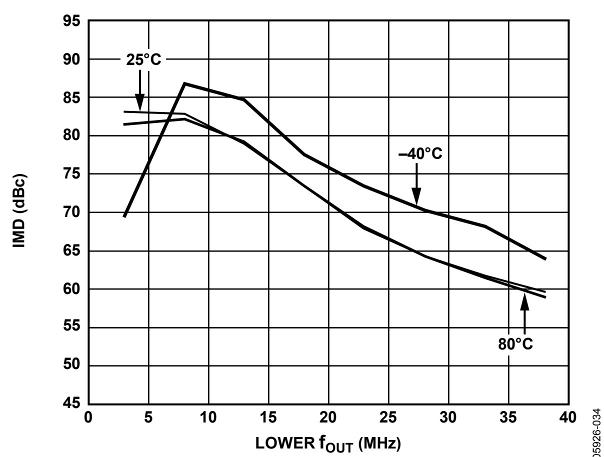


Figure 38. Dual-Tone IMD vs. f_{OUT} and Temperature @ 80 MSPS, I_{OUTFS} = 2 mA and 0 dBFS

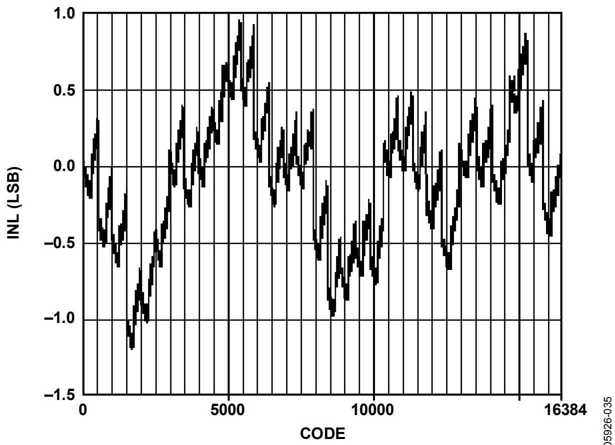


Figure 39. Typical Uncalibrated INL

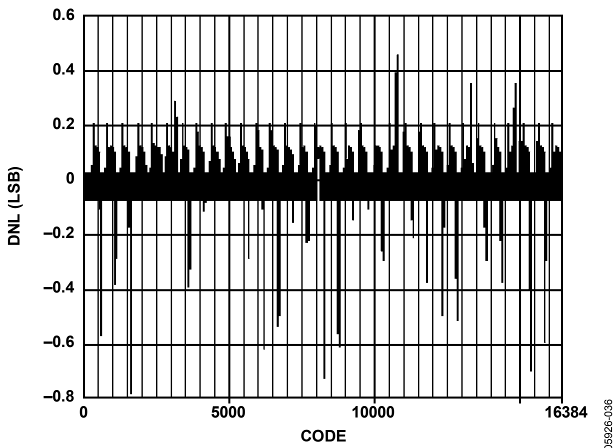


Figure 40. Typical Uncalibrated DNL

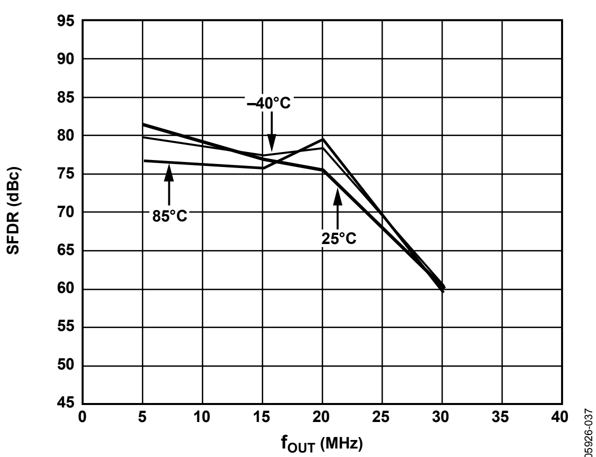


Figure 41. SFDR vs. Temperature @ 80 MSPS

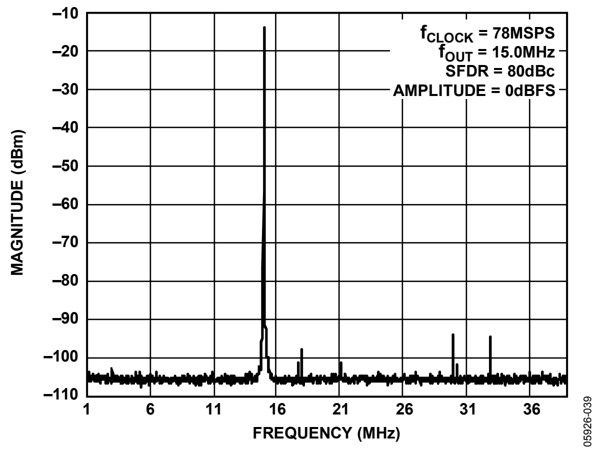


Figure 42. Single-Tone SFDR

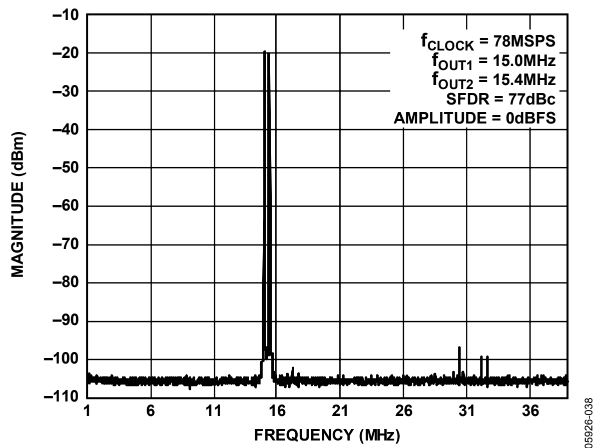


Figure 43. Dual-Tone SFDR

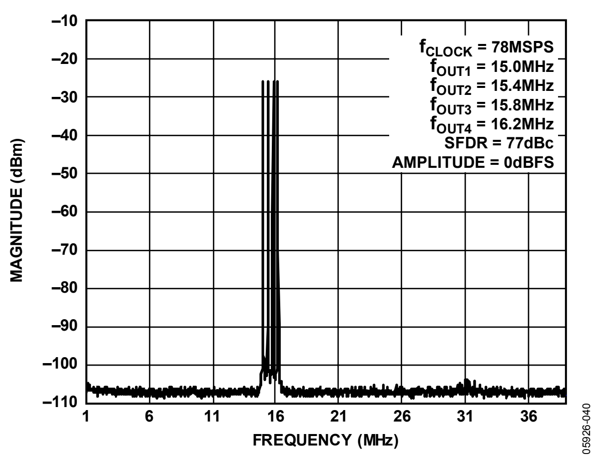


Figure 44. Four-Tone SFDR

AD9704, AD9705, AND AD9706

VDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.

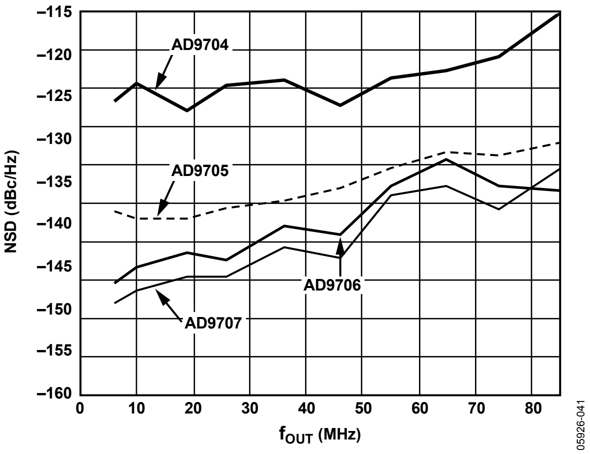


Figure 45. AD9704, AD9705, AD9706 NSD vs. f_{OUT} @ 0 dBFS

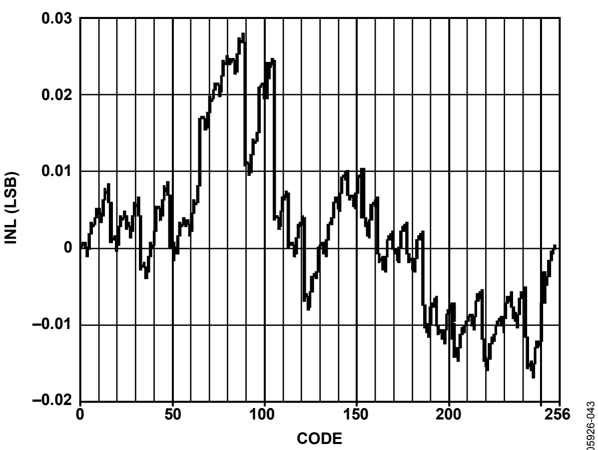


Figure 46. AD9704 Typical Uncalibrated INL

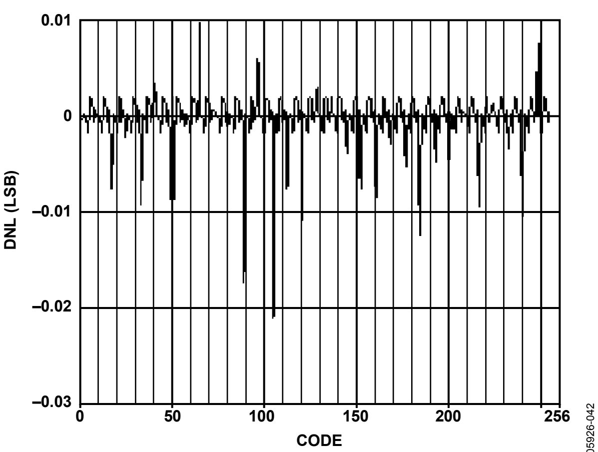


Figure 47. AD9704 Typical Uncalibrated DNL

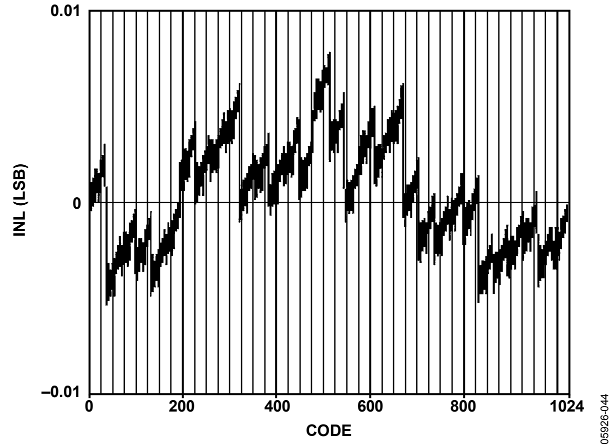


Figure 48. AD9705 Typical Uncalibrated INL

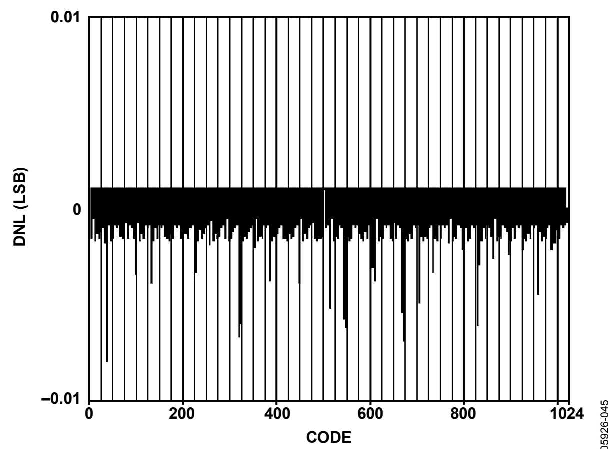


Figure 49. AD9705 Typical Uncalibrated DNL

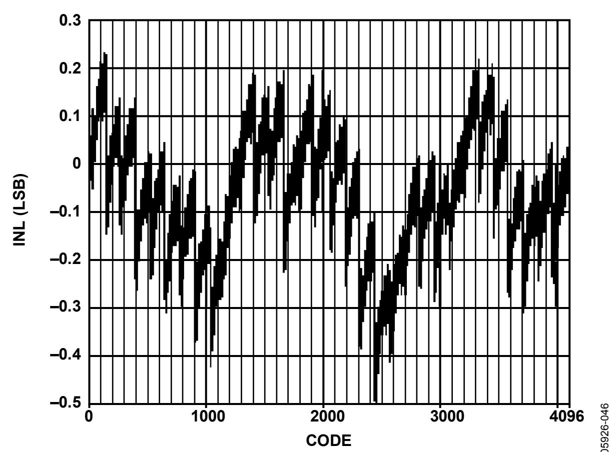


Figure 50. AD9706 Typical Uncalibrated INL

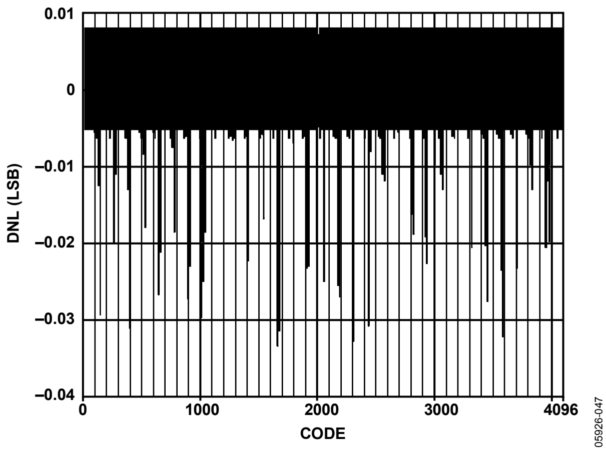


Figure 51. AD9706 Typical Uncalibrated DNL

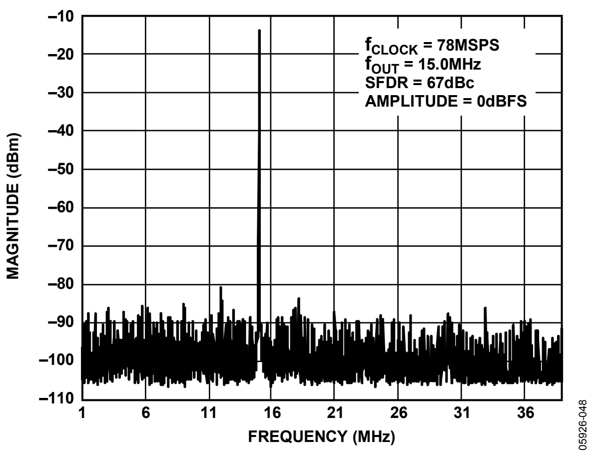


Figure 52. AD9704 Single-Tone SFDR

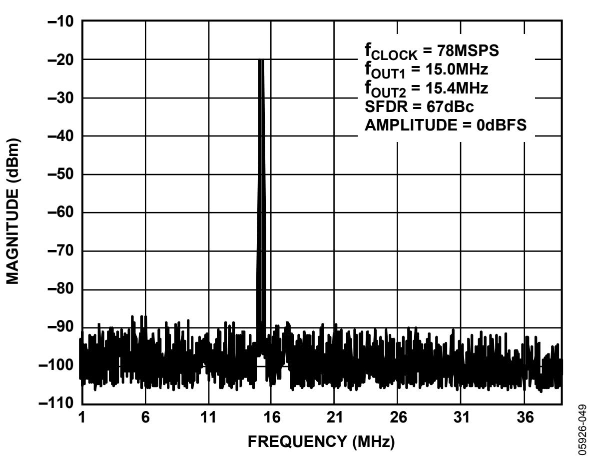


Figure 53. AD9704 Dual-Tone SFDR

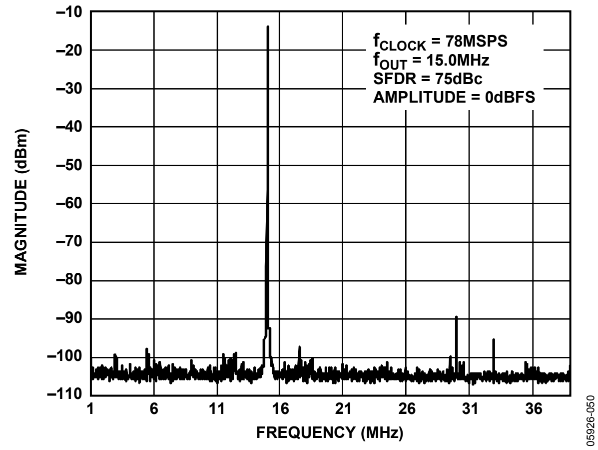


Figure 54. AD9705 Single-Tone SFDR

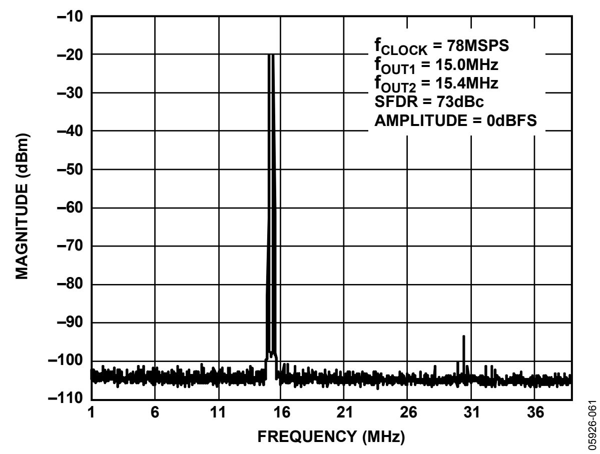


Figure 55. AD9705 Dual-Tone SFDR

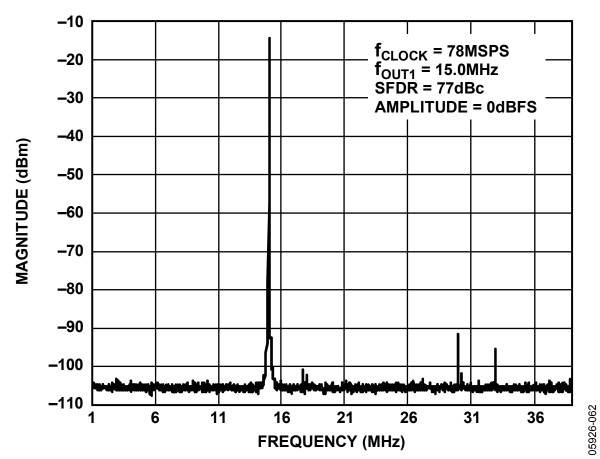


Figure 56. AD9706 Single-Tone SFDR

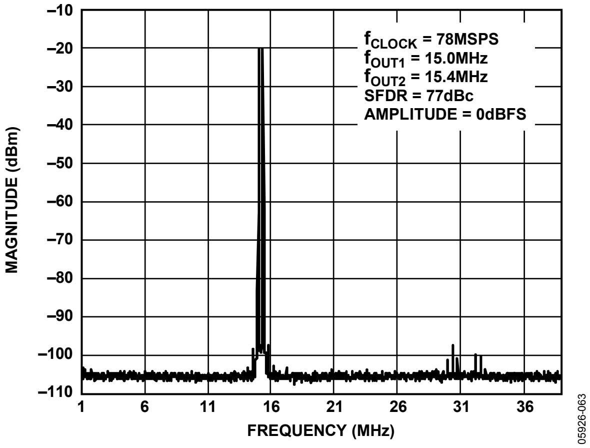


Figure 57. AD9706 Dual-Tone SFDR

VDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.

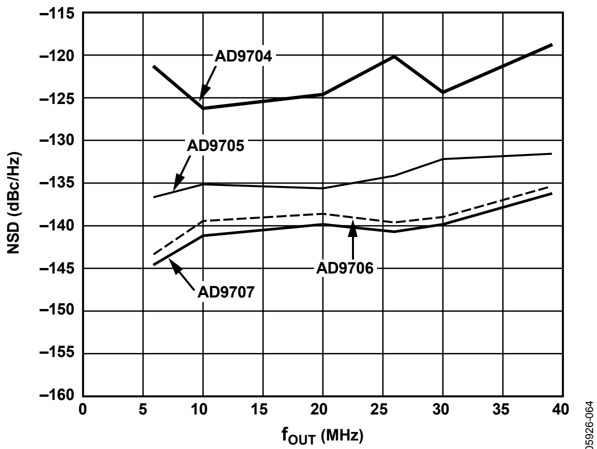


Figure 58. AD9704, AD9705, AD9706 NSD vs. f_{OUT} @ 0 dBFS

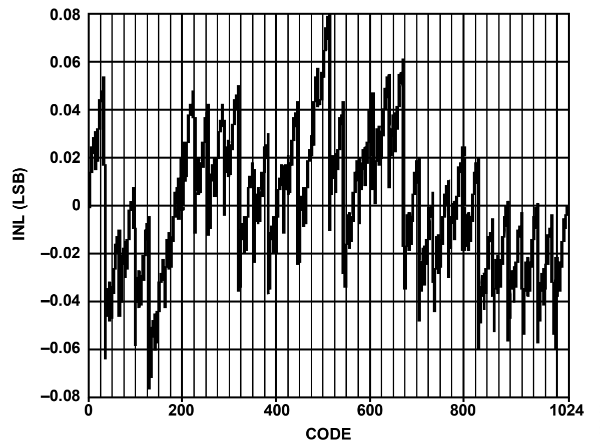


Figure 61. AD9705 Typical Uncalibrated INL

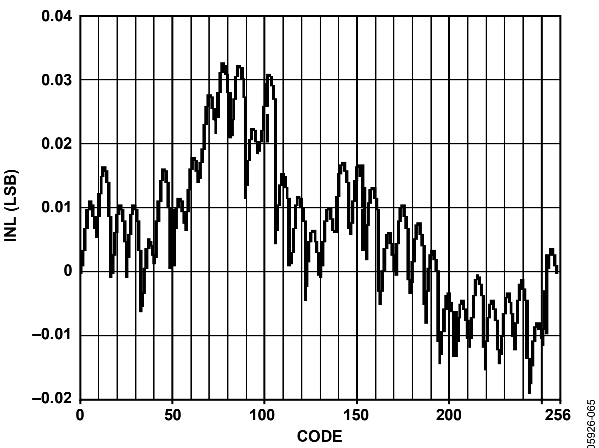


Figure 59. AD9704 Typical Uncalibrated INL

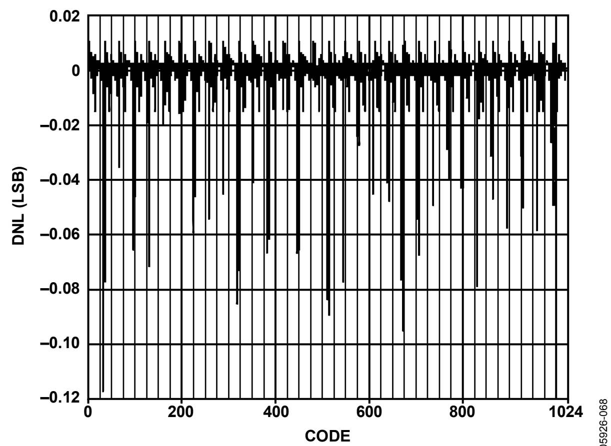


Figure 62. AD9705 Typical Uncalibrated DNL

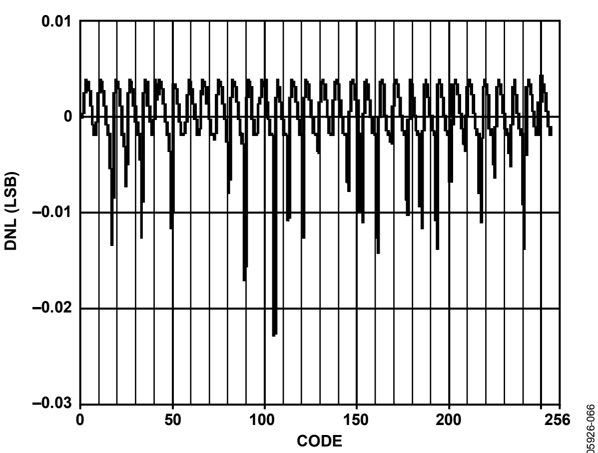


Figure 60. AD9704 Typical Uncalibrated DNL

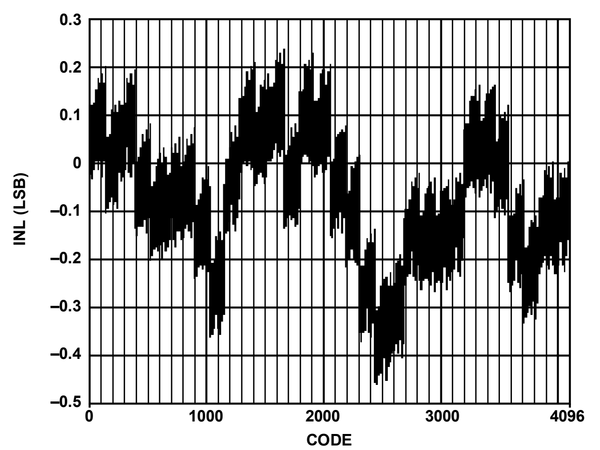


Figure 63. AD9706 Typical Uncalibrated INL

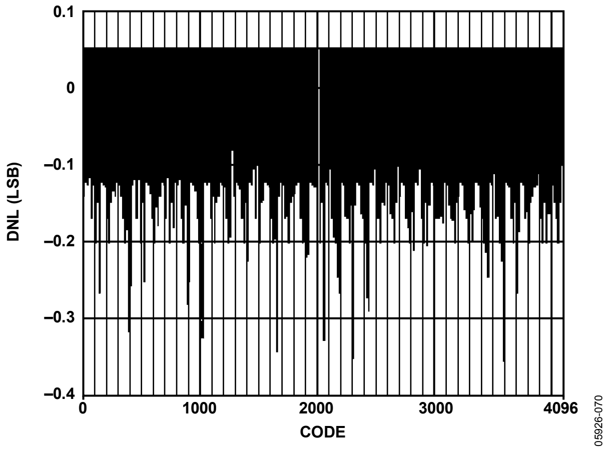


Figure 64. AD9706 Typical Uncalibrated DNL

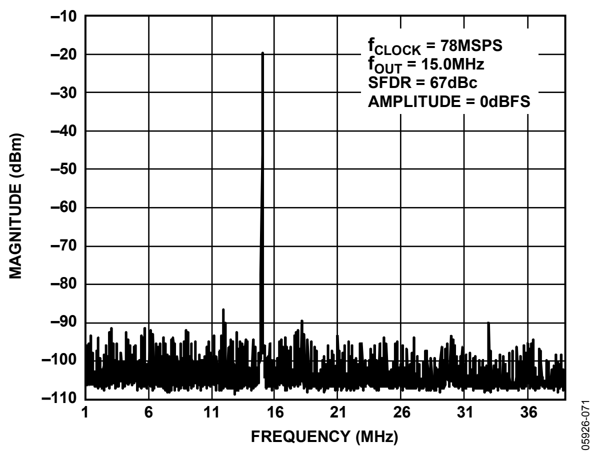


Figure 65. AD9704 Single-Tone SFDR

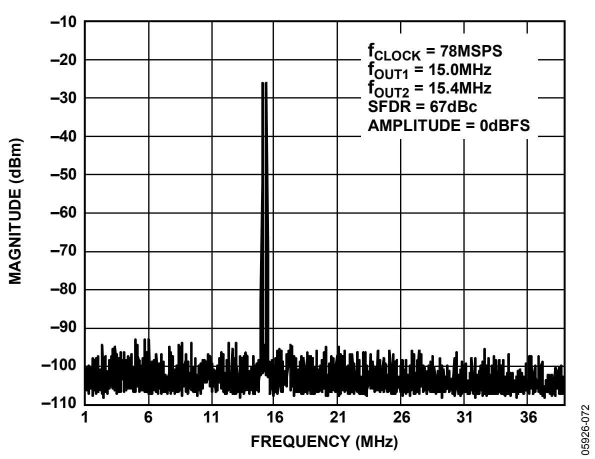


Figure 66. AD9704 Dual-Tone SFDR

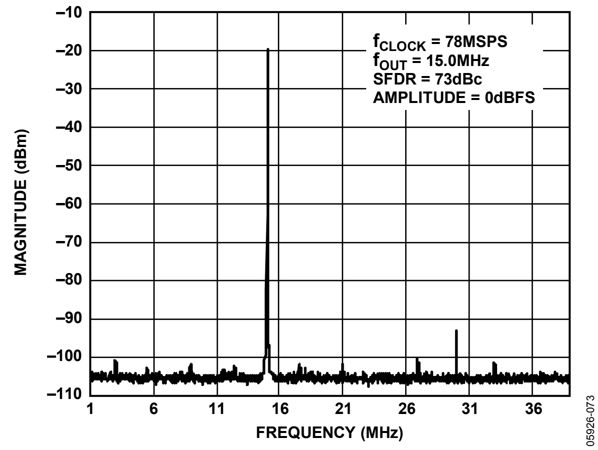


Figure 67. AD9705 Single-Tone SFDR

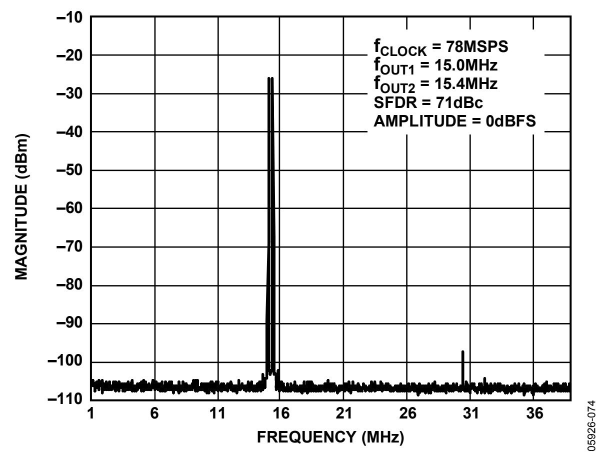


Figure 68. AD9705 Dual-Tone SFDR

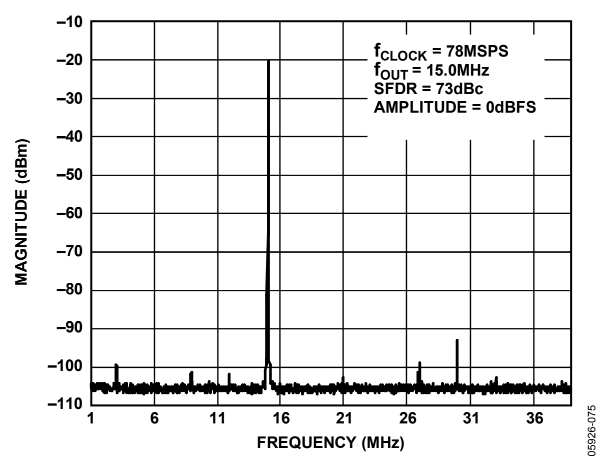


Figure 69. AD9706 Single-Tone SFDR

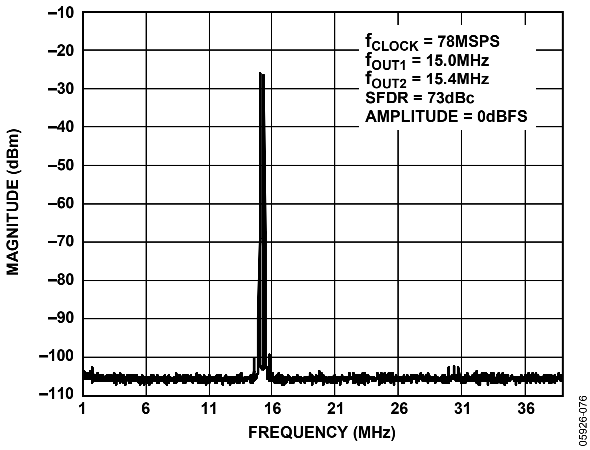


Figure 70. AD9706 Dual-Tone SFDR

TERMINOLOGY

Linearity Error (Also Called Integral Nonlinearity or INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called the offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured VREF. Therefore, the gain error does not include effects of the reference.

Output Compliance Range
Output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolt-seconds (pV-s).

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
Multitone power ratio is the spurious-free dynamic range containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

Noise Spectral Density (NSD)
Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

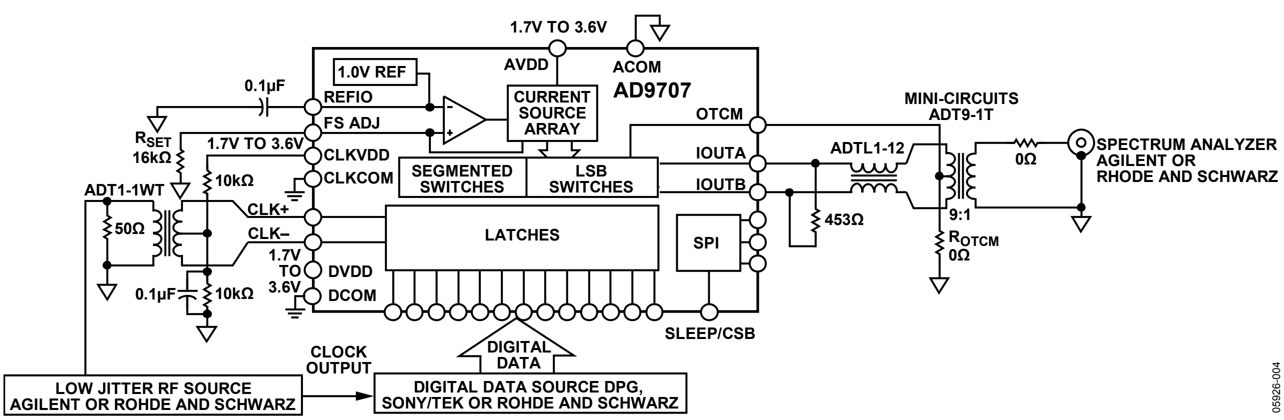


Figure 71. Basic AC Characterization Test Setup

THEORY OF OPERATION

Figure 72 shows a simplified block diagram of one of the AD970x parts, the AD9707 The AD970x consists of a DAC, digital control logic, and full-scale output current control. The DAC contains a PMOS current source array capable of providing a nominal full-scale current (I_{OUTFS}) of 2 mA and a maximum of 5 mA. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16 of an MSB current source. The remaining LSBs are binary weighted fractions of the current sources of the middle bits. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances the AD970x dynamic performance for multitone or low amplitude signals and helps maintain the high output impedance of the DAC (that is, >200 MΩ).

All of these current sources are switched to one of the two output nodes (IOUTA or IOUTB) via PMOS differential current switches. The switches are based on the architecture pioneered in the AD9764 family, with further refinements made to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD970x have separate power supply inputs (AVDD and DVDD) that can operate independently over a 1.7 V to 3.6 V range. The digital section, which is capable of operating at a rate of up to 175 MSPS, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.0 V band gap voltage reference, and a reference control amplifier.

The DAC full-scale output current is regulated by the reference control amplifier and can be set from 1 mA to 5 mA via an external resistor, R_{SET}, connected to the full-scale adjust (FS ADJ) pin.

The external resistor, in combination with both the reference control amplifier and voltage reference, V_{REFIO}, sets the reference current, I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is $32 \times I_{REF}$.

The AD970x provides the option of setting the output common mode to a value other than ACOM via the output common mode (OTCM) pin. This facilitates interfacing the output of the AD970x directly to components that require common-mode levels greater than 0 V.

SERIAL PERIPHERAL INTERFACE

The AD970x serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD970x. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial interface port of the AD970x is configured as a single pin I/O.

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD970x. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD970x, coincident with the first eight SCLK rising edges. The instruction byte provides the AD970x serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD970x.

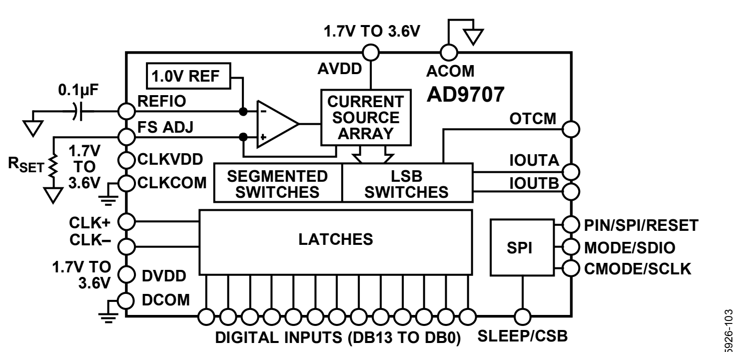


Figure 72. Simplified Block Diagram

A logic high on Pin 17 (PIN/SPI/RESET), followed by a logic low, resets the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD970x and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes, as determined by the instruction byte. Using one multibyte transfer is the preferred method. Single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the information shown in the following bit map:

MSB **LSB**

7	6	5	4	3	2	1	0
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation. N1 and N0, Bit 6 and Bit 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 13.

A4, A3, A2, A1, and A0, which are Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte, respectively, determine which register is accessed during the data transfer portion of the communication cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD970x, based on the DATADIR bit (Register 0x00, Bit 6).

Table 13. Byte Transfer Count

N1	N0	Description
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

Serial Interface Port Pin Descriptions

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD970x and to run the internal state machines. The SCLK maximum frequency is 20 MHz. All data input to the AD970x is registered on the rising edge of SCLK. All data is driven out of the AD970x on the falling edge of SCLK.

CSB—Chip Select. Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O. This pin is used as a bidirectional data line to transmit and receive data.

MSB/LSB Transfers

The AD970x serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the DATADIR bit (Register 0x00, Bit 6). The default is MSB first (DATADIR = 0).

When DATADIR = 0 (MSB first), the instruction and data bytes must be written from most significant bit to least significant bit. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When DATADIR = 1 (LSB first), the instruction and data bytes must be written from least significant bit to most significant bit. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The AD970x serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB first mode is active.

Notes on Serial Port Operation

The AD970x serial port configuration is controlled by Register 0x00, Bit 7. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register can occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the software reset, SWRST (Register 0x00, Bit 5). All registers are set to their default values except Register 0x00, which remains unchanged.

Use of single byte transfers is recommended when changing serial port configurations or initiating a software reset to prevent unexpected device behavior.

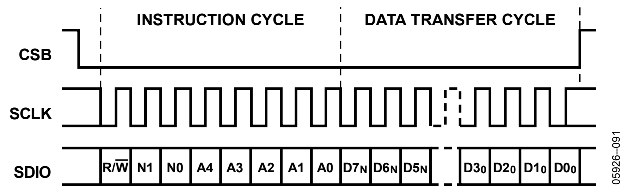


Figure 73. Serial Register Interface Timing, MSB First Write

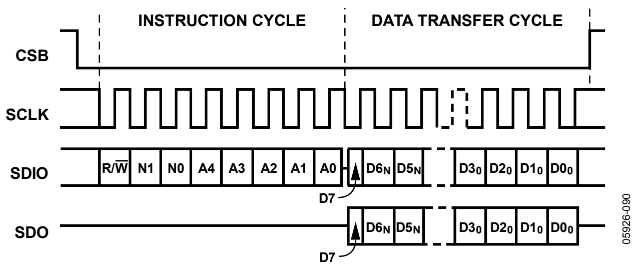


Figure 74. Serial Register Interface Timing, MSB First Read

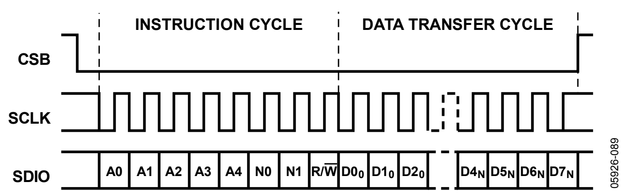


Figure 75. Serial Register Interface Timing, LSB First Write

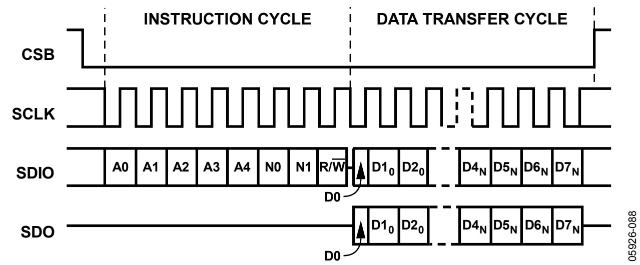


Figure 76. Serial Register Interface Timing, LSB First Read

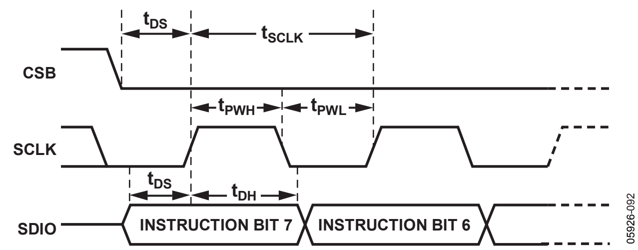


Figure 77. Timing Diagram for SPI Register Write

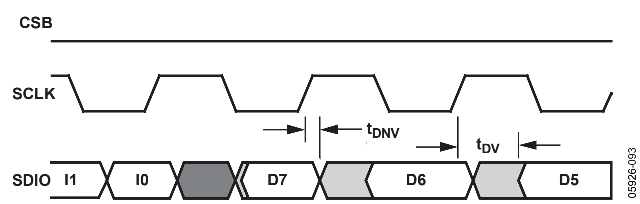


Figure 78. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Table 14.

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI CTL	0x00	SDIODIR	DATADIR	SWRST	LNGINS	PDN	SLEEP	CLKOFF	EXREF
DATA	0x02	DATAFMT			DCLKPOL	DESKEW	CLKDIFF		CALCLK
VERSION	0x0D					VER[3]	VER[2]	VER[1]	VER[0]
CALMEM	0x0E			CALMEM[1]	CALMEM[0]		DIVSEL[2]	DIVSEL[1]	DIVSEL[0]
MEMRDWR	0x0F	CALSTAT	CALEN			SMEMWR	SMEMRD		UNCAL
MEMADDR	0x10			MEMADDR[5]	MEMADDR[4]	MEMADDR[3]	MEMADDR[2]	MEMADDR[1]	MEMADDR[0]
MEMDATA	0x11			MEMDATA[5]	MEMDATA[4]	MEMDATA[3]	MEMDATA[2]	MEMDATA[1]	MEMDATA[0]
TRIM	0x14				CALDACFS				

SPI REGISTER DESCRIPTIONS

Table 15. SPI CTL—Register 0x00

Bit Name	Bit	Direction (I/O)	Default	Description
SDIODIR	7	I	1	0: SDIO pin configured for input only during data transfer (4-wire interface) 1: SDIO pin configured for input or output during data transfer (3-wire interface)
DATADIR	6	I	0	0: Serial data uses MSB first format 1: Serial data uses LSB first format
SWRST	5	I	0	1: Initiate a software reset; this bit is set to 0 upon reset completion
LNGINS	4	I	0	0: Use 1 byte preamble (5 address bits) 1: Use 2 byte preamble (13 address bits)
PDN	3	I	0	1: All analog and digital circuitry off, except serial interface
SLEEP	2	I	0	1: DAC output current off
CLKOFF	1	I	0	1: Disables internal master clock.
EXREF	0	I	0	0: Internal bandgap reference 1: External reference

Table 16. DATA—Register 0x02

Bit Name	Bit	Direction (I/O)	Default	Description
DATAFMT	7	I	0	0: Unsigned binary input data format 1: Twos complement input data format
DCLKPOL	4	I	0	0: Data latched on DATACLK rising edge always 1: Data latched on DATACLK falling edge (only active in DESKEW mode)
DESKEW	3	I	0	0: DESKEW mode disabled 1: DESKEW mode enabled (adds a register in digital data path to remove skew in received data; one clock cycle of latency is introduced)
CLKDIFF	2	I	0	0: Single-ended clock input 1: Differential clock input
CALCLK	0	I	0	0: Calibration clock disabled 1: Calibration clock enabled

Table 17. VERSION—Register 0x0D

Bit Name	Bit	Direction (I/O)	Default	Description
VER[3:0]	[3:0]	O		Hardware version identifier

Table 18. CALMEM—Register 0x0E

Bit Name	Bit	Direction (I/O)	Default	Description
CALMEM[1:0]	[5:4]	O	00	Calibration memory 00: Uncalibrated 01: Self-calibration 10: Not Used 11: User input
DIVSEL[2:0]	[2:0]	I	000	Calibration clock divide ratio from DAC clock rate 000: /256 001: /128 : 110: /4 111: /2

Table 19. MEMRDWR—Register 0x0F

Bit Name	Bit	Direction (I/O)	Default	Description
CALSTAT	7	O	0	1: Calibration cycle complete
CALEN	6	I	0	1: Initiate device self-calibration
SMEMWR	3	I	0	1: Write to static memory (calibration coefficients)
SMEMRD	2	I	0	1: Read from static memory (calibration coefficients)
UNCAL	0	I	0	1: Reset calibration coefficients to default (uncalibrated)

Table 20. MEMADDR—Register 0x10

Bit Name	Bit	Direction (I/O)	Default	Description
MEMADDR[5:0]	[5:0]	I/O	000000	Address of static memory to be accessed

Table 21. MEMDATA—Register 0x11

Bit Name	Bit	Direction (I/O)	Default	Description
MEMDATA[5:0]	[5:0]	I/O	111111	Data for static memory access

Table 22. TRIM—Register 0x14

Bit Name	Bit	Direction (I/O)	Default	Description
CALDACFS	4	I	0	0: Calibration DAC full-scale uses AVDD 1: Calibration DAC full-scale uses AVDD/2

REFERENCE OPERATION

The AD970x contains an internal 1.0 V band gap reference. The internal reference can be disabled by writing a Logic 1 to Register 0x00, Bit 0 (EXREF) in the SPI.

To use the internal reference, decouple the REFIO pin to ACOM with a 0.1 µF capacitor, enable the internal reference, and write a Logic 0 to Register 0x00, Bit 0 in the SPI. (Note that this is the default configuration.) The internal reference voltage is present at REFIO. If the voltage at REFIO is to be used anywhere else in the circuit, an external buffer amplifier with an input bias current of less than 100 nA should be used. An example of the use of the internal reference is shown in Figure 79.

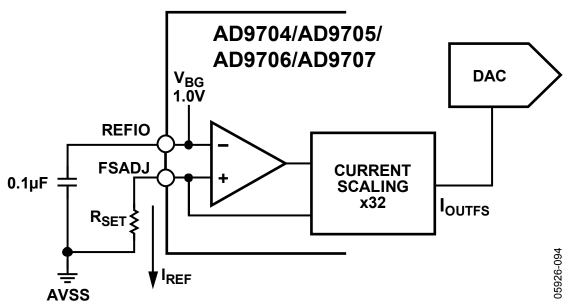


Figure 79. Internal Reference Configuration

REFIO serves as either an input or an output, depending on whether the internal or an external reference is used. Table 23 summarizes the reference operation.

Table 23. Reference Operation

Reference Mode	REFIO Pin	Register Setting
Internal	Connect 0.1 µF capacitor	Register 0x00, Bit 0 = 0 (default)
External	Apply external reference	Register 0x00, Bit 0 = 1 (for power saving)

An external reference can be used in applications requiring tighter gain tolerances or lower temperature drift. Also, a variable external voltage reference can be used to implement a method for gain control of the DAC output. The external reference is applied to the REFIO pin. Note that the 0.1 µF compensation capacitor is not required. The internal reference can be directly overdriven by the external reference, or the internal reference can be powered down. The input impedance of REFIO is 10 kΩ when powered up and 1 MΩ when powered down.

REFERENCE CONTROL AMPLIFIER

The AD970x contains a control amplifier that regulates the full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 79. The output current, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is mirrored to the segmented current sources with the proper scale factor to set I_{OUTFS}, as stated in Equation 3.

The control amplifier allows a 5:1 adjustment span of I_{OUTFS} from 1 mA to 5 mA by setting I_{REF} between 31.25 µA and 156.25 µA (R_{SET} between 6.4 kΩ and 32 kΩ). The wide adjustment span of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD970x, which is proportional to I_{OUTFS} (see the Power Dissipation section). The second benefit relates to the ability to adjust the output over a 14 dB range, which is useful for controlling the transmitted power.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz. This allows the device to be used for low frequency, small signal multiplying applications.

DAC TRANSFER FUNCTION

The AD970x provides complementary current outputs, IOUTA and IOUTB. IOUTA provides a near full-scale current output, I_{OUTFS}, when all bits are high (that is, DAC CODE = $2^N - 1$, where N = 8, 10, 12, or 14 for the AD9704, AD9705, AD9706, and AD9707, respectively); while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and I_{OUTFS} and can be expressed as

$$IOUTA = (DAC\ CODE/2^N) \times I_{OUTFS} \quad (1)$$

$$IOUTB = ((2^N - 1) - DAC\ CODE)/2^N \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to $2^N - 1$ (that is, decimal representation).

I_{OUTFS} is a function of the reference current, I_{REF}, which is nominally set by a reference voltage, V_{REFIO}, and an external resistor, R_{SET}. It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is

$$V_{IOUTA} = IOUTA \times R_{LOAD} \quad (5)$$

$$V_{IOUTB} = IOUTB \times R_{LOAD} \quad (6)$$

Note: To achieve the maximum output compliance of 1 V at the nominal 2 mA output current, R_{LOAD} must be set to 500 Ω.

Also note that the full-scale value of V_{IOUTA} and V_{IOUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF} = (IOUTA - IOUTB) \times R_{LOAD} \quad (7)$$

Substituting the values of IOUTA, IOUTB, I_{REF}, and V_{DIFF} can be expressed as

$$V_{DIFF} = \{(2 \times DAC\ CODE - (2^N - 1))/2^N\} \times (32 \times V_{REFIO}/R_{SET}) \times R_{LOAD} \quad (8)$$

Equation 7 and Equation 8 highlight some of the advantages of operating the AD970x differentially. First, the differential operation helps cancel common-mode error sources associated with IOUTA and IOUTB, such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (that is, V_{IOUTA} or V_{IOUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended output (V_{IOUTA} and V_{IOUTB}) or differential output (V_{DIFF}) of the AD970x can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET}, because of their ratiometric relationship, as shown in Equation 8.

ANALOG OUTPUTS

The complementary current outputs in each DAC, IOUTA, and IOUTB can be configured for single-ended or differential operation. IOUTA and IOUTB can be converted into complementary single-ended voltage outputs, V_{IOUTA} and V_{IOUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equation 5 through Equation 8. The differential voltage, V_{DIFF}, existing between V_{IOUTA} and V_{IOUTB}, can also be converted to a single-ended voltage via a transformer or a differential amplifier configuration. The ac performance of the AD970x is optimum and is specified using a differential transformer-coupled output in which the voltage swing at IOUTA and IOUTB is limited to ±0.5 V.

The distortion and noise performance of the AD970x can be enhanced when it is configured for differential operation. The common-mode error sources of both IOUTA and IOUTB can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (assuming no source termination). Because the output currents of IOUTA and IOUTB are complementary, they become additive when processed differentially.

When the AD970x is being used at its nominal operating point of 2 mA output current, and 0.5 V output swing is desired, R_{LOAD} must be set to 250 Ω. A properly selected transformer allows the AD970x to provide the required power and voltage levels to different loads.

The output impedance of IOUTA and IOUTB is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 200 MΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (that is, V_{IOUTA} and V_{IOUTB}) due to the nature of a PMOS device. As a result, maintaining IOUTA and/or IOUTB at a virtual ground via an I-V op amp configuration results in the optimum dc linearity. Note that the INL/DNL specifications for the AD970x are measured with IOUTA maintained at a virtual ground via an op amp.

IOUTA and IOUTB also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The absolute maximum negative output compliance range of −1 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit can result in a breakdown of the output stage and affect the reliability of the AD970x.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.0 V for an I_{OUTFS} = 2 mA to 0.8 V for an I_{OUTFS} = 1 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUTA and IOUTB does not exceed 0.5 V.

ADJUSTABLE OUTPUT COMMON MODE

The AD970x provides the ability to set the output common mode to a value other than ACOM via Pin 19 (OTCM). This extends the compliance range of the outputs and facilitates interfacing the output of the AD970x to components that require common-mode levels other than 0 V. The OTCM pin demands dynamically changing current and should be driven by a low source impedance to prevent a common-mode signal from appearing on the DAC outputs. For optimum performance, set the voltage on OTCM equal to the center of the output swing on IOUTA and IOUTB.

Note that setting OTCM to a voltage greater than ACOM allows the peak of the output signal to be closer to the positive supply rail. To prevent distortion in the output signal due to limited available headroom, the common-mode level must be chosen such that the following expression is satisfied:

$$AVDD - V_{OTCM} > 1.8\ V \quad (10)$$

DIGITAL INPUTS

The AD9707, AD9706, AD9705, and AD9704 have data inputs of 14, 12, 10, and 8 bits, respectively; and each has a clock input. The parallel data inputs can follow standard positive binary or twos complement coding. IOUTA produces a full-scale output current when all data bits are at Logic 1. IOUTB produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

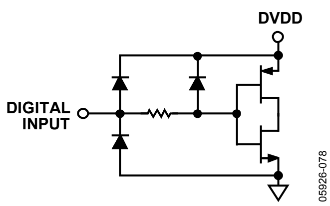


Figure 80. Equivalent Digital Input

The digital interface is implemented using an edge-triggered master/slave latch. The DAC output updates on the rising edge of the clock and is designed to support a clock rate as high as 175 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup and hold times can also be varied within the clock cycle, as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

CLOCK INPUT

A configurable clock input allows the device to be operated in a single-ended or a differential clock mode. The mode selection can be controlled either by the CMODE pin, if the device is in pin mode; or through SPI Register 0x02, Bit 2 (CLKDIFF), if the SPI is enabled. Connecting CMODE to CLKCOM selects the single-ended clock input. In this mode, the CLK+ input is driven with rail-to-rail swings, and the CLK− input is left floating. If CMODE is connected to CLKVDD, the differential receiver mode is selected. In this mode, both inputs are high impedance. Table 24 gives a summary of clock mode control. There is no significant performance difference between the clock input modes.

Table 24. Clock Mode Selection

SPI Disabled CMODE Pin	SPI Enabled Register 0x02, Bit 2	Clock Input Mode
CLKCOM	0	Single-ended
CLKVDD	1	Differential

In differential input mode, the clock input functions as a high impedance differential pair. The common-mode level of the CLK+ and CLK− inputs can vary from 0.75 V to 2.25 V, and the differential voltage can be as low as 0.5 V p-p. This mode can be used to drive the clock with a differential sine wave because the high gain bandwidth of the differential inputs converts the sine wave into a single-ended square wave internally.

DAC TIMING

Input Clock and Data Timing Relationship

Dynamic performance in a DAC is dependent on the relationship between the position of the clock edges and the time at which the input data changes. The AD970x is rising-edge triggered and so exhibits dynamic performance sensitivity when the data transition is close to this edge. In general, the goal when applying the AD970x is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 81 shows the relationship of SFDR to clock placement with different sample rates.

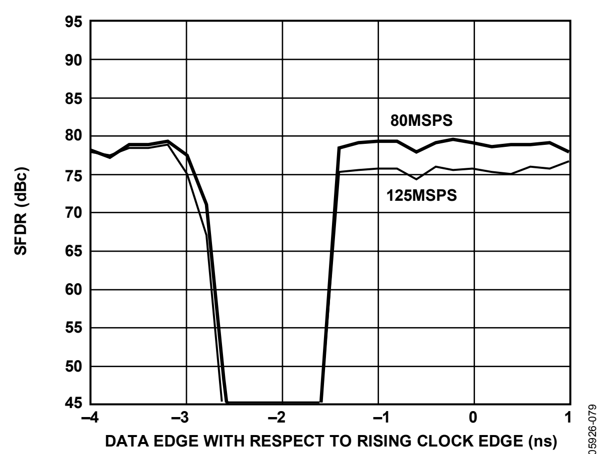


Figure 81. SFDR vs. Clock Placement

POWER DISSIPATION

The power dissipation, P_D, of the AD970x is dependent on several factors that include

- The power supply voltages (AVDD, CLKVDD, and DVDD)
- The full-scale current output, I_{OUTFS}
- The update rate, f_{CLOCK}
- The reconstructed digital input waveform

Power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is equal to a fixed current plus I_{OUTFS}, as shown in Figure 82. I_{DVDD} is proportional to f_{CLOCK} and increases with increasing analog output frequencies. Figure 84 shows I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 3.3 V. I_{CLKVDD} is directly proportional to f_{CLOCK} and is higher for differential clock operation than for single-ended operation, as shown in Figure 86. This difference in clock current is due primarily to the differential clock receiver, which is disabled in single-ended clock mode.

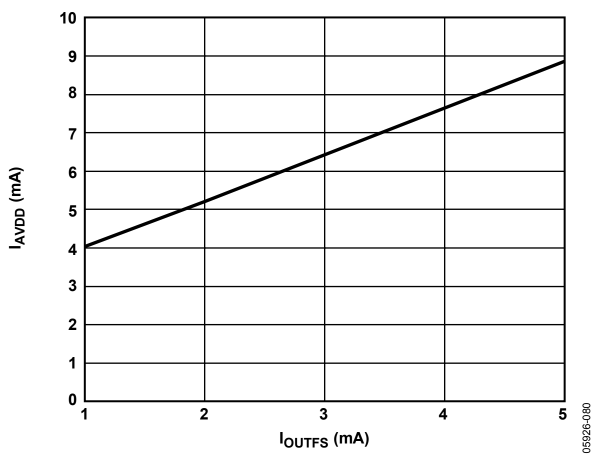


Figure 82. I_{AVDD} vs. I_{OUTFS} @ AVDD = 3.3 V

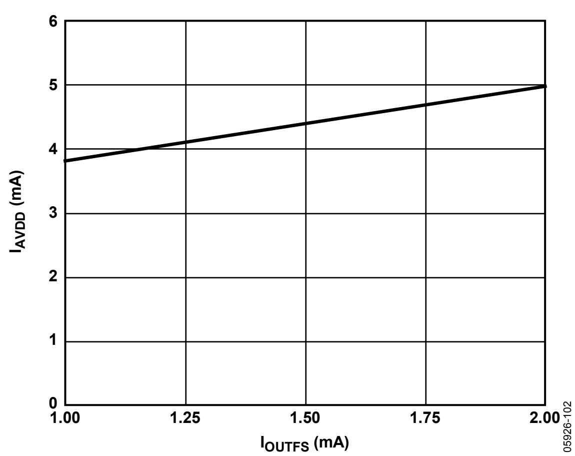


Figure 83. I_{AVDD} vs. I_{OUTFS} @ AVDD = 1.8 V

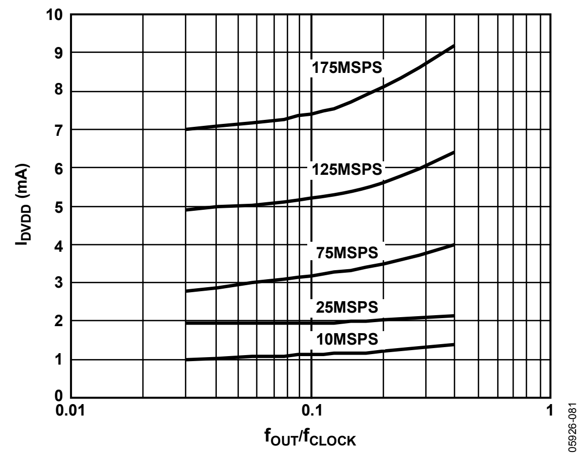


Figure 84. I_{DVDD} vs. f_{OUT}/f_{CLOCK} Ratio @ DVDD = 3.3 V

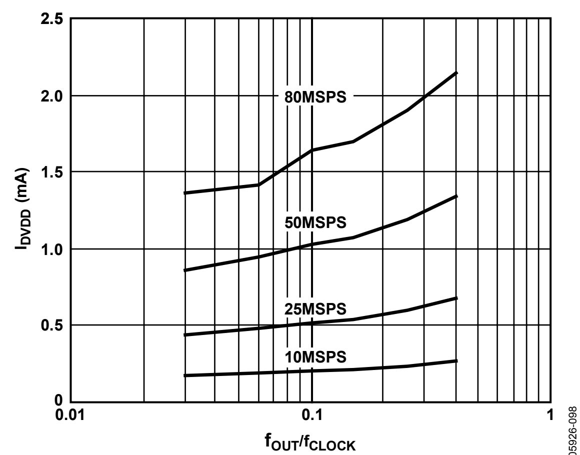


Figure 85. I_{DVDD} vs. f_{OUT}/f_{CLOCK} Ratio @ DVDD = 1.8 V

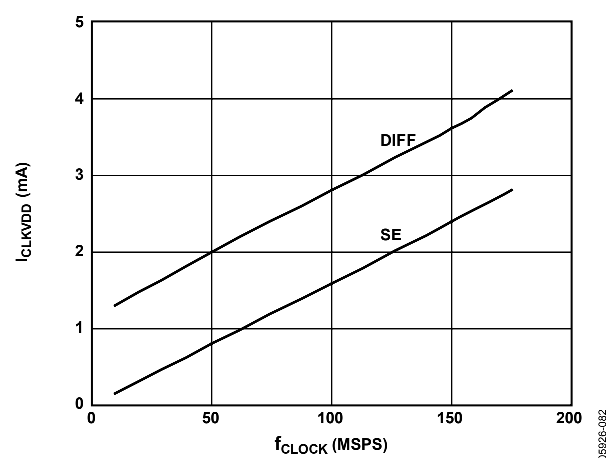


Figure 86. I_{CLKVDD} vs. f_{CLOCK} @ CLKVDD = 3.3 V

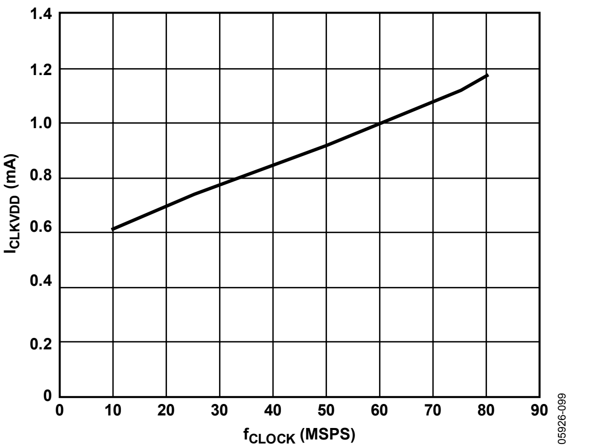


Figure 87. I_{CLKVDD} vs. f_{CLOCK} (Differential Clock Mode) @ CLKVDD = 1.8 V

Sleep and Power-Down Operation (Pin Mode)

The AD970x has a sleep mode that turns off the output current and reduces the total power consumed by the device. This mode is activated by applying a Logic 1 to the SLEEP/CSB pin. The SLEEP/CSB pin logic threshold is equal to 0.5 × AVDD. This digital input also contains an active pull-down circuit.

The AD970x takes less than 50 ns to power down and approximately 5 μs to power back up.

Sleep and Power-Down Operation (SPI Mode)

The AD970x offers three power-down functions that can be controlled through the SPI. These power-down modes can be used to minimize the power dissipation of the device. The power-down functions are controlled through SPI Register 0x00, Bit 1 to Bit 3. Table 25 summarizes the power-down functions that can be controlled through the SPI. The power-down mode can be enabled by writing a Logic 1 to the corresponding bit in Register 0x00.

Table 25. Power-Down Mode Selection

Power-Down Mode	(Reg. 0x00) Bit #	Functional Description
Clock Off	1	Turn off clock
Sleep	2	Turn off output current
Power Down	3	Turn off output current and internal voltage reference

SELF-CALIBRATION

The AD970x has a self-calibration feature that improves the DNL of the device. Performing a self-calibration on the device improves device performance in low frequency applications. The device performance in applications where the analog output frequencies are above 1 MHz are generally influenced more by dynamic device behavior than by DNL, and in these cases, self-calibration is unlikely to provide any benefits for single-tones, as shown in Figure 88. Figure 89 shows that self-calibration is helpful up to 20 MHz for two-tone IMD spaced 10 kHz apart.

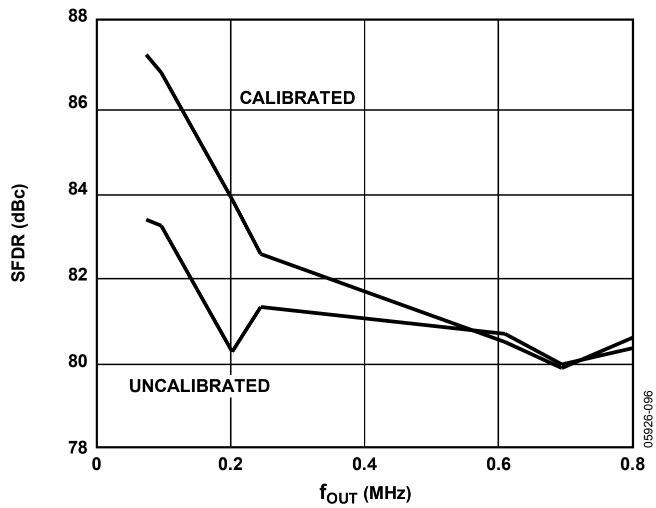


Figure 88. AD9707 SFDR vs. f_{OUT} @ 175 MSPS and I_{OUTFS} = 2 mA

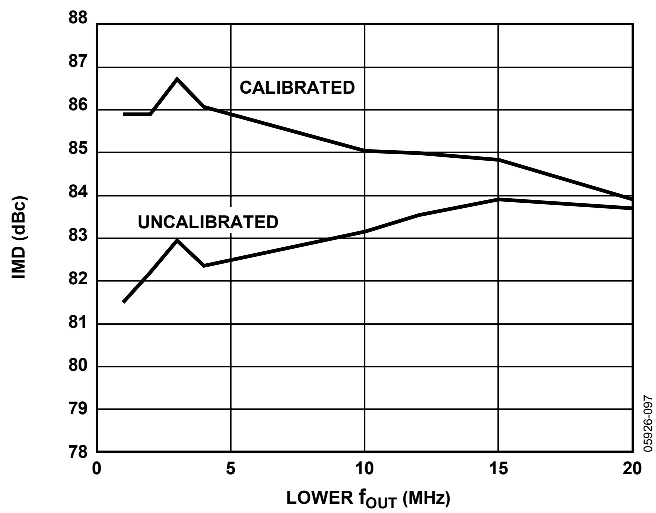


Figure 89. IMD vs. f_{OUT} @ 175 MSPS and I_{OUTFS} = 2 mA

To perform a device self-calibration, the following procedure can be used.

The calibration clock frequency is equal to the DAC clock divided by the division factor chosen by the DIVSEL value. The frequency of the calibration clock must be set to under 10 MHz for reliable calibrations. Best results are obtained by setting DIVSEL[2:0] (Register 0x0E, Bit 2 to Bit 0) to produce the lowest frequency calibration clock frequency that your system requirements allow.

1. Enable the calibration clock by setting the CALCLK bit (Register 0x02, Bit 0).
2. Enable self-calibration by writing 0x40 to Register 0x0F.
3. Wait approximately 4500 calibration clock cycles. Each calibration clock cycle is between 2 and 256 DAC clock cycles, depending on the value of DIVSEL[2:0].
4. Check if the self-calibration has completed by reading the CALSTAT bit (Register 0x0F, Bit 7). A Logic 1 indicates the calibration has completed.
5. When the self-calibration has completed, write 0x00 to Register 0x0F.
6. Disable the calibration clock by clearing the CALCLK Bit (Register 0x02, Bit 0).

The AD970x devices allow reading and writing of the calibration coefficients. There are 33 coefficients in total. The read/write feature of the coefficients could be useful for improving the results of the self-calibration routine by averaging the results of several calibration results and loading the averaged results back into the device. The reading and writing routines follow.

To read the calibration coefficients

1. Enable the calibration clock by setting the CALCLK bit (Register 0x02, Bit 0).
2. Write the address of the first coefficient (0x00) to Register 0x10.
3. Set the SMEMRD bit (Register 0x0F, Bit 2) by writing 0x04 to Register 0x0F.
4. Read the value of the first coefficient by reading the contents of Register 0x11.
5. Clear the SMEMRD bit by writing 0x00 to Register 0x0F.
6. Repeat Step 2 through Step 5 for each of the remaining 32 coefficients by incrementing the address by one each read.
7. Disable the calibration clock by clearing the CALCLK Bit (Register 0x02, Bit 0).

To write the calibration coefficients to the device:

1. Enable the calibration clock by setting the CALCLK bit (Register 0x02, Bit 0).
2. Set the SMEMWR bit (Register 0x0F, Bit 3) by writing 0x08 to Register 0x0F.
3. Write the address of the first coefficient (0x00) to Register 0x10.
4. Write the value of the first coefficient to Register 0x11.
5. Repeat Step 2 and Step 3 for each of the remaining 32 coefficients by incrementing the address by one each write.
6. Clear the SMEMWR bit by writing 0x00 to Register 0x0F.
7. Disable the calibration clock by clearing the CALCLK bit (Register 0x02, Bit 0).

APPLICATIONS

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD970x. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 2 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application that allows ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, signal gain, and/or a low output impedance.

A single-ended output is suitable for applications where low cost and low power consumption are primary concerns.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion, as shown in Figure 90. The distortion performance of a transformer typically exceeds that available from standard op amps, particularly at higher frequencies. Transformer coupling provides excellent rejection of common-mode distortion (that is, even-order harmonics) over a wide frequency range. It also provides electrical isolation and can deliver voltage gain without adding noise. Transformers with different impedance ratios can also be used for impedance matching purposes. The main disadvantages of transformer coupling are the low frequency roll-off, lack of power gain, and the higher output impedance.

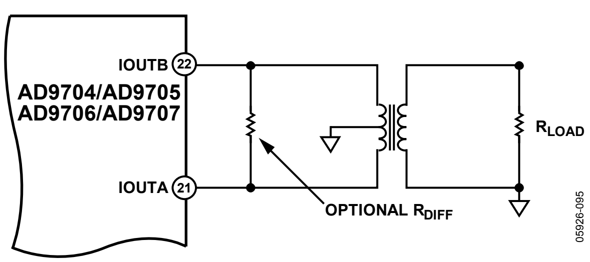


Figure 90. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to a voltage that keeps the voltages on IOUTA and IOUTB within the output common voltage range of the device. It should be noted that the dc component of the DAC output current is equal to $I_{FS}/2$ and flows out of both IOUTA and IOUTB. The center tap of the transformer should provide a path for this dc current. In many applications, AGND provides the most convenient voltage for the transformer center tap. The complementary voltages appearing at IOUTA and IOUTB (that is, V_{IOUTA} and V_{IOUTB}) swing symmetrically around AGND and should be maintained with the specified output compliance range of the AD970x.

A differential resistor, R_{DIFF}, can be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF}, as reflected by the transformer, is chosen to provide a source termination that results in a low VSWR. Note that approximately half the signal power is dissipated across R_{DIFF}.

SINGLE-ENDED BUFFERED OUTPUT USING AN OP AMP

An op amp can be used to perform a single-ended current-to-voltage conversion, as shown in Figure 91. The AD970x is configured with a pair of series resistors, R_S, off each output. The feedback resistor, R_{FB}, determines the peak single-ended output voltage by the formula

$$V_{OUT} = R_{FB} \times \frac{I_{FS}}{2}$$

The common-mode voltage of the output is determined by the formula

$$V_{CM} = V_{REF} \times (1 + \frac{R_{FB}}{R_B}) - V_{OUT}$$

The maximum and minimum voltages out of the amplifier are

$$V_{MAX} = V_{REF} \times (1 + \frac{R_{FB}}{R_B})$$

$$V_{MIN} = V_{MAX} - I_{FS} \times R_{FB}$$

respectively.

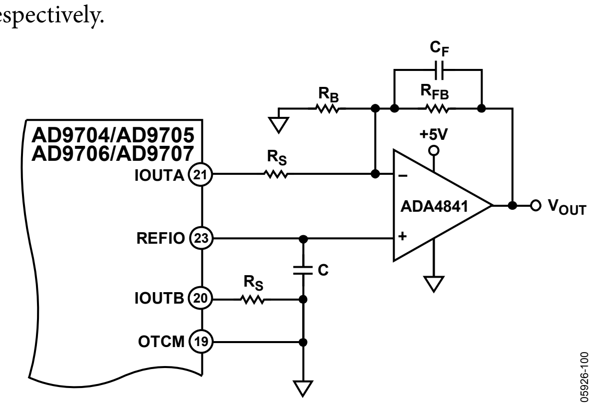


Figure 91. *Single-Supply Single-Ended Buffer*

DIFFERENTIAL BUFFERED OUTPUT USING AN OP AMP

A dual op amp (see the circuit shown in Figure 92) can be used in a differential version of the single-ended buffer shown in Figure 91. The same R-C network is used to form a 1-pole differential, low-pass filter to isolate the op amp inputs from the high frequency images produced by the DAC outputs. The feedback resistors, R_{FB}, determine the peak differential output voltage by the formula

$$V_{OUT} = R_{FB} \times I_{FS}$$

The maximum and minimum voltages out of the amplifier are

$$V_{MAX} = V_{REF} \times (1 + \frac{R_{FB}}{R_B})$$

$$V_{MIN} = V_{MAX} - V_{OUT}$$

respectively. The common-mode voltage of the output is determined by the formula

$$V_{CM} = V_{MAX} - \frac{V_{OUT}}{2}$$

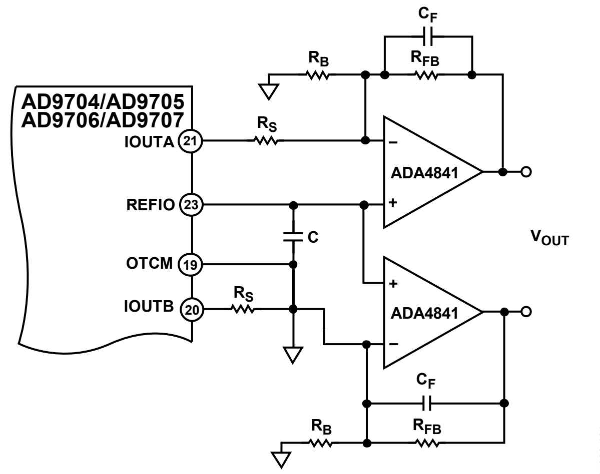


Figure 92. Single-Supply Differential Buffer

EVALUATION BOARD

GENERAL DESCRIPTION

The TxDAC family evaluation boards allow for easy setup and testing of any TxDAC products. Careful attention to layout and circuit design, combined with a prototyping area, allows the user to evaluate the AD970x easily and effectively in any application where a low power, high resolution, high speed conversion is required.

The AD970x board allows the user the flexibility to operate the part in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs are designed to be driven from various data pattern generators, with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD970x with either the internal or external reference, or to exercise the power-down feature.

EVALUATION BOARD SCHEMATICS

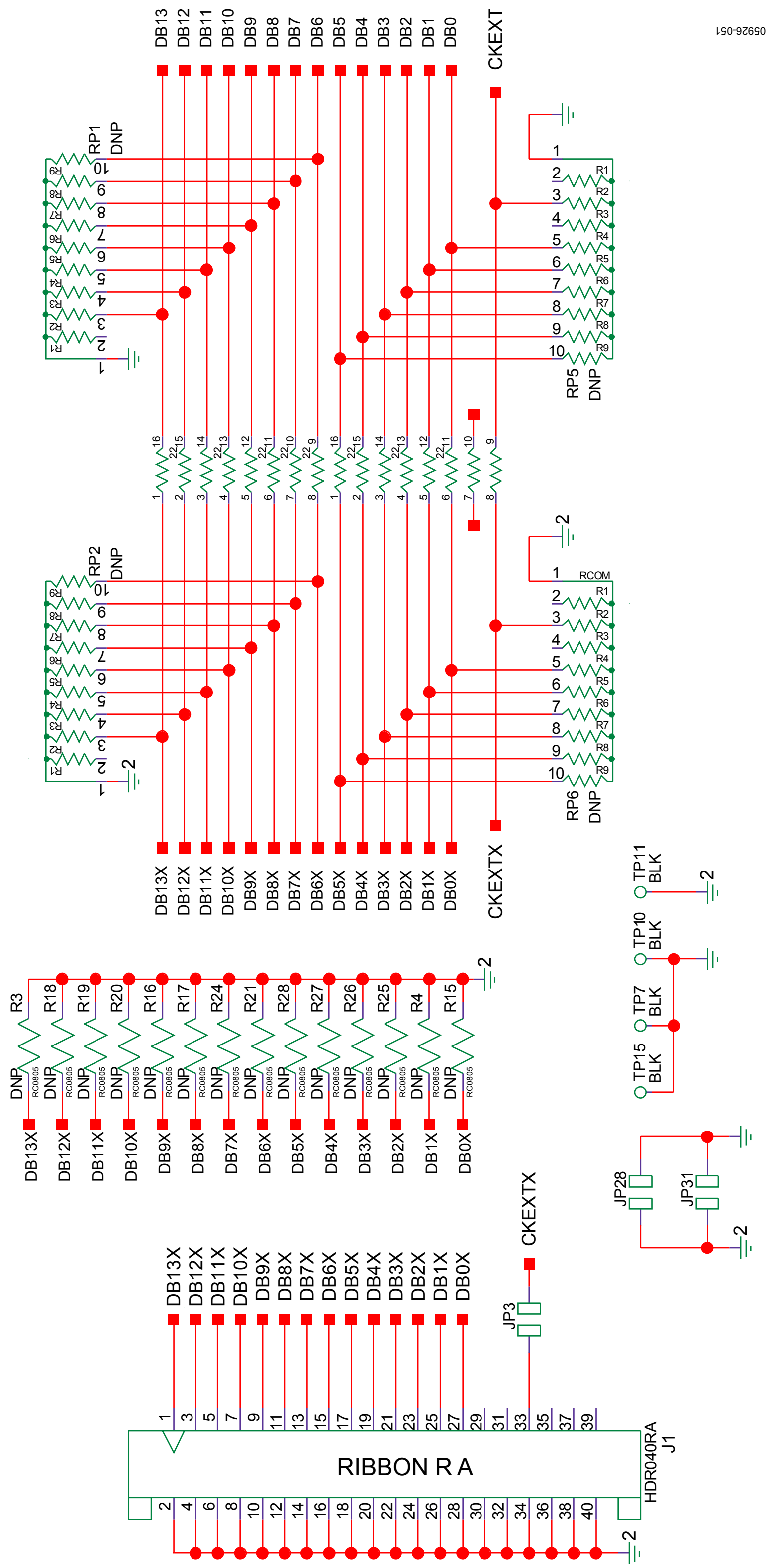


Figure 93. Digital Inputs

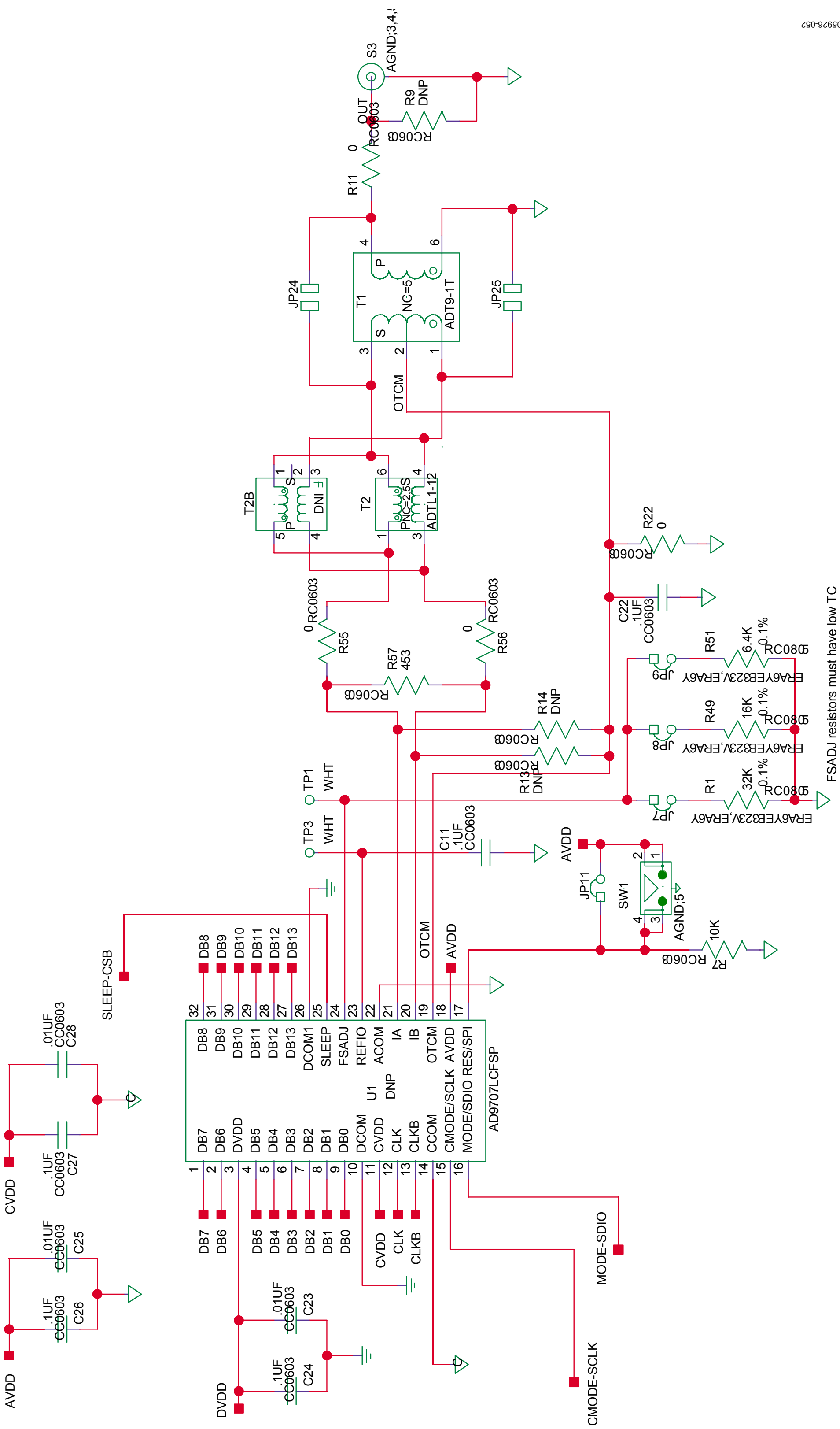


Figure 94. Output Signal Conditioning

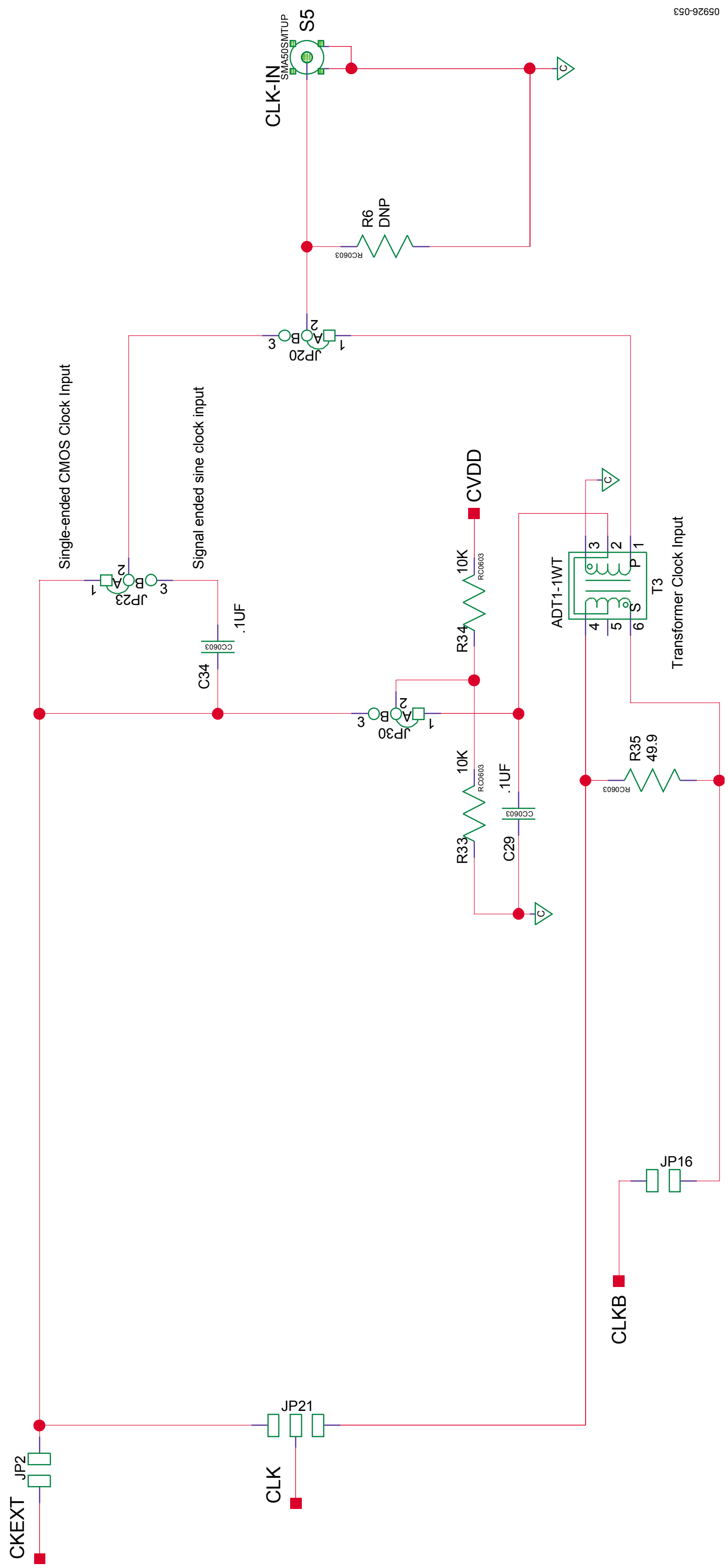


Figure 95. Clock

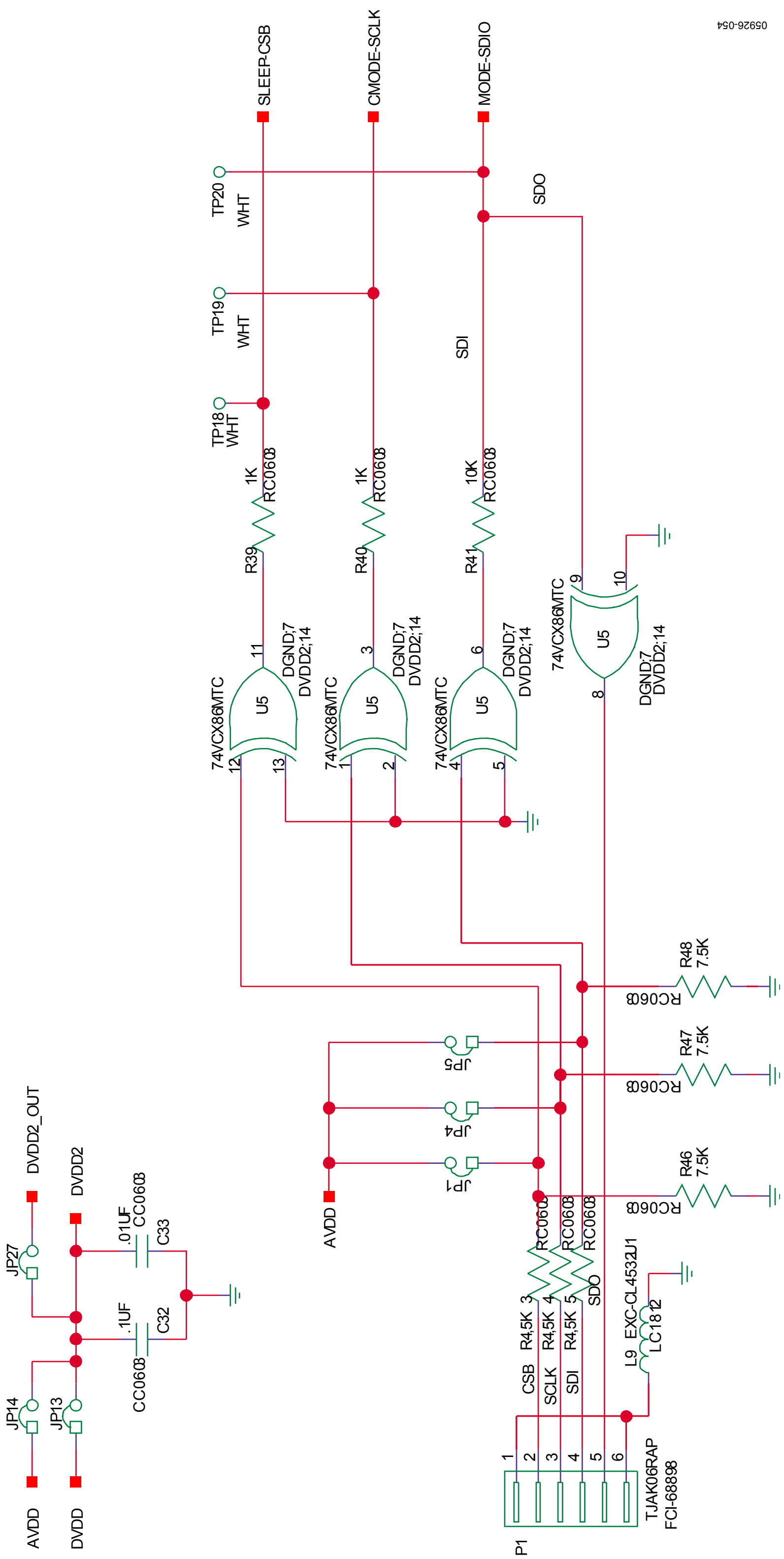


Figure 96. SPI

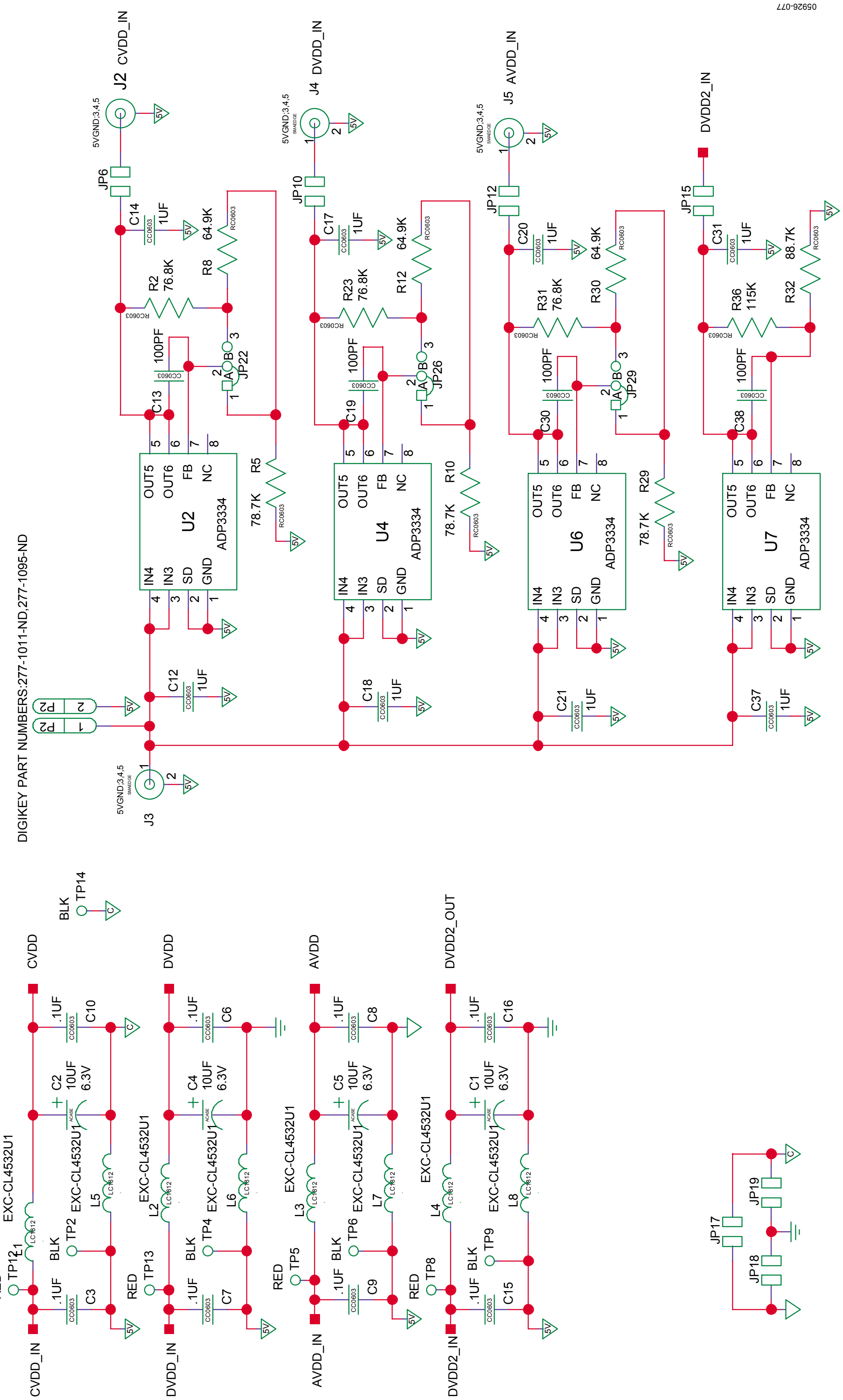


Figure 97. Power Supplies

EVALUATION BOARD LAYOUT

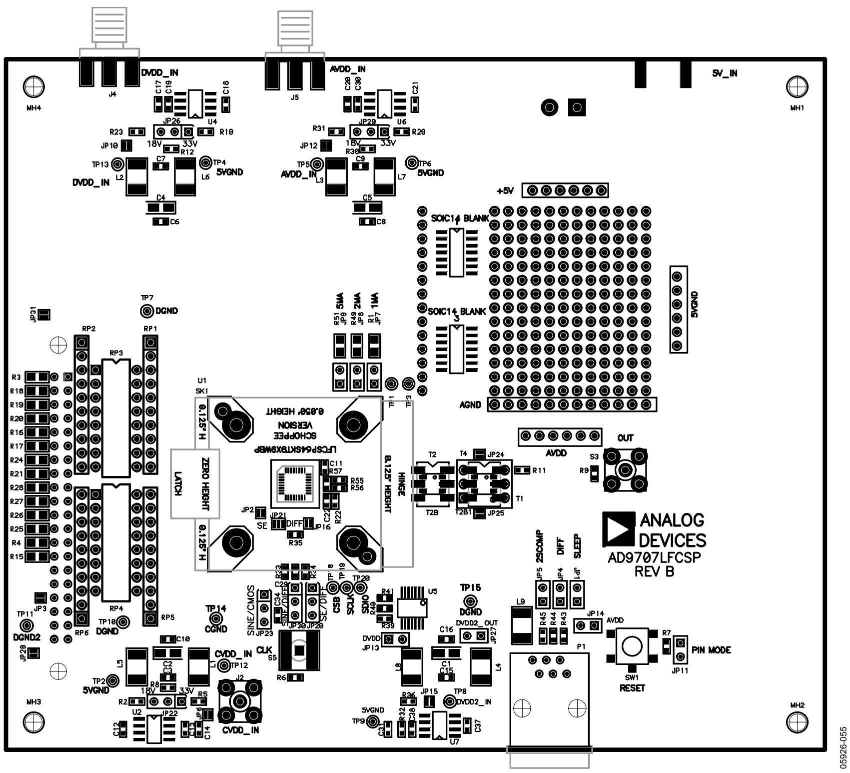


Figure 98. Assembly—Primary Side

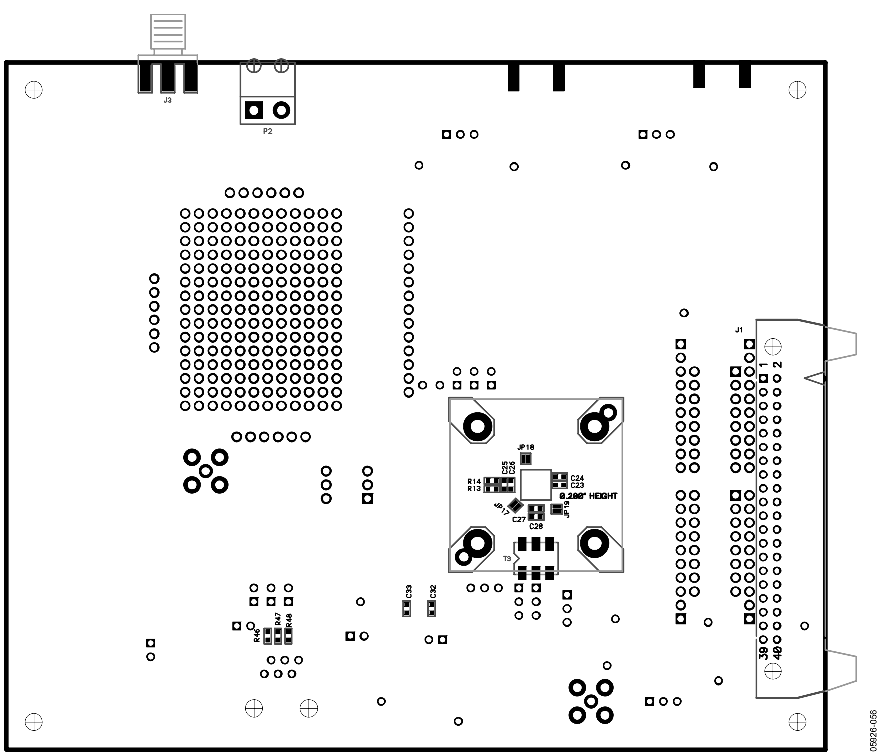


Figure 99. Assembly—Secondary Side

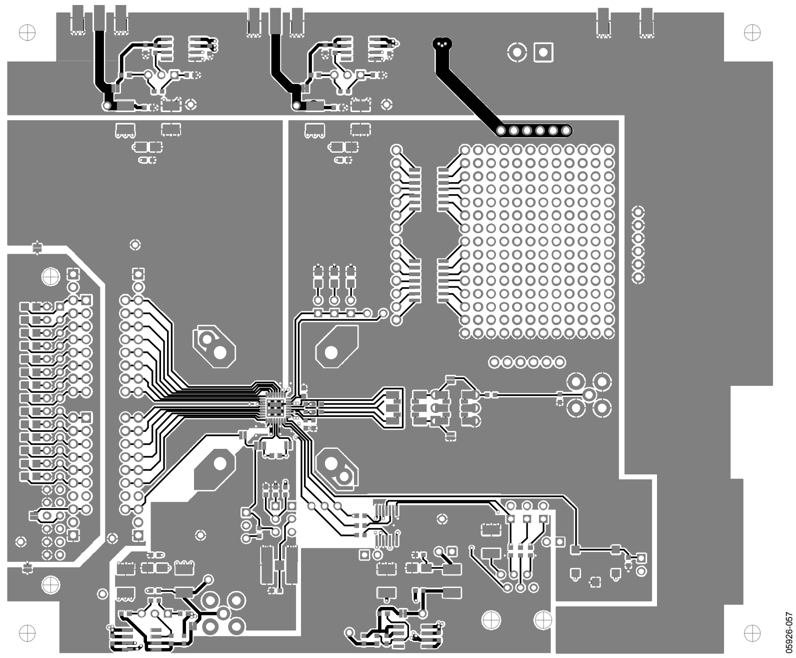


Figure 100. Layer 1—Primary Side

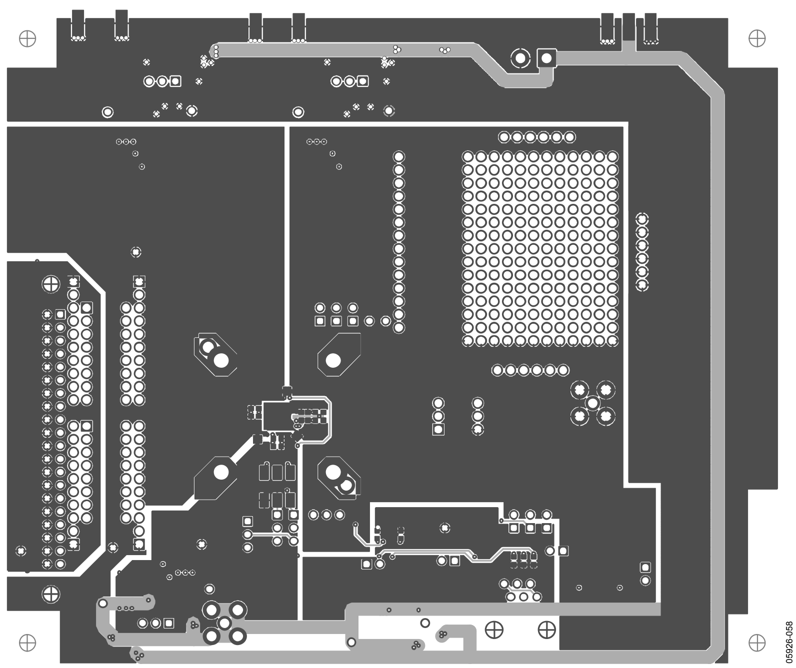


Figure 101. Layer 4—Secondary Side

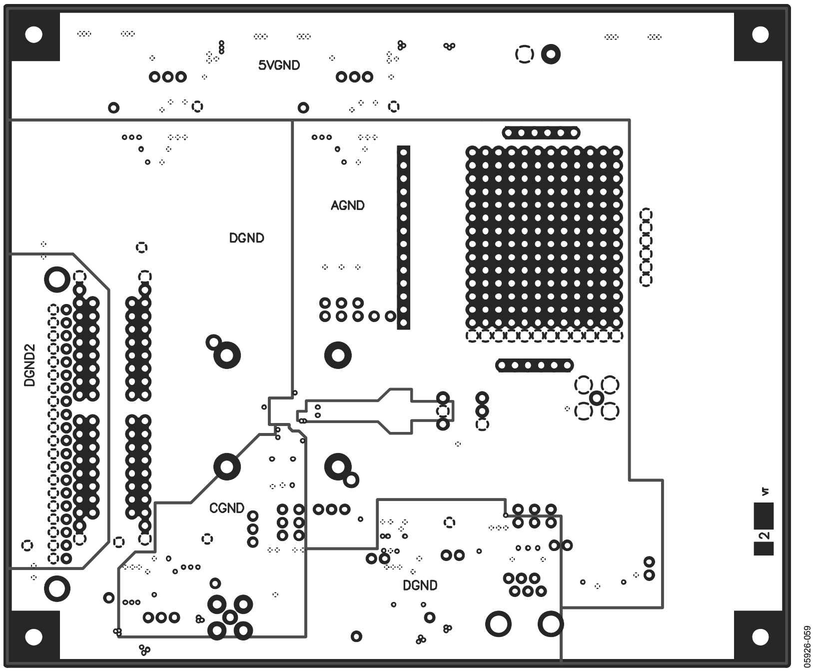


Figure 102. Layer 2—Ground Plane

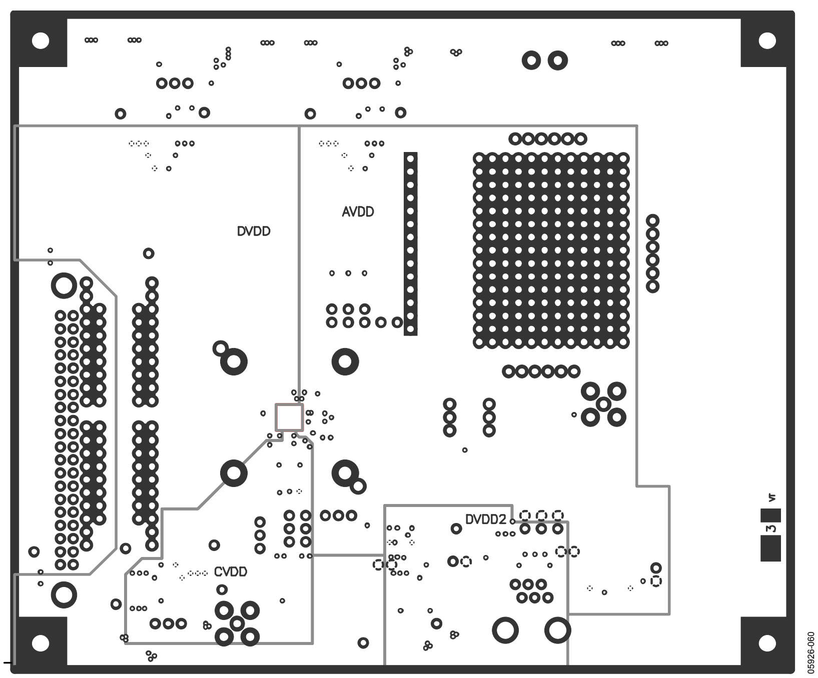
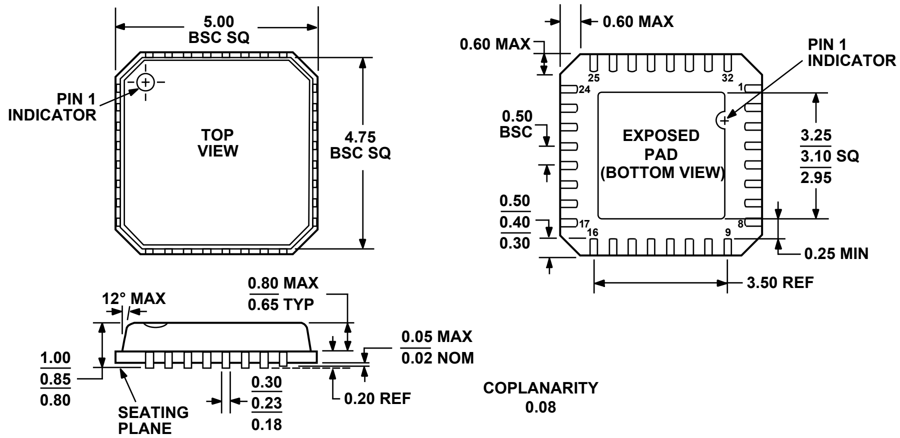


Figure 103. Layer 3—Power Plane

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 104. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9704BCPZ[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9704BCPZRL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9705BCPZ[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9705BCPZRL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9706BCPZ[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9706BCPZRL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9707BCPZ[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9707BCPZRL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9704-EB		Evaluation Board	
AD9705-EB		Evaluation Board	
AD9706-EB		Evaluation Board	
AD9707-EB		Evaluation Board	

[1] Z = Pb-free part.

NOTES