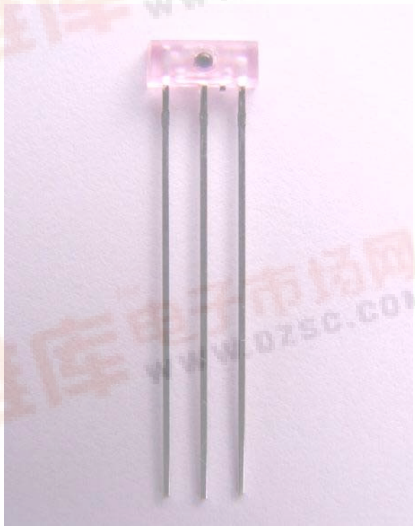
Technical Data Sheet

Photo link Light Receiver Unit

PLR135



Features

1. High PD sensitivity optimized for red light
2. Data : NRZ signal
3. Low power consumption for extended battery life
4. Built-in threshold control for improved noise Margin
5. Good ESD protection: up to 8KV
6. Pb Free
7. Receiver sensitivity: up to –27dBm (Min. for 16Mbps)
   up to –21dBm (Min. for 25Mbps
8. The product itself will remain within RoHS compliant version.

Descriptions

The optical receiver is packaged with custom optic data link interface, integrated on a proprietary CMOS PDIC process.

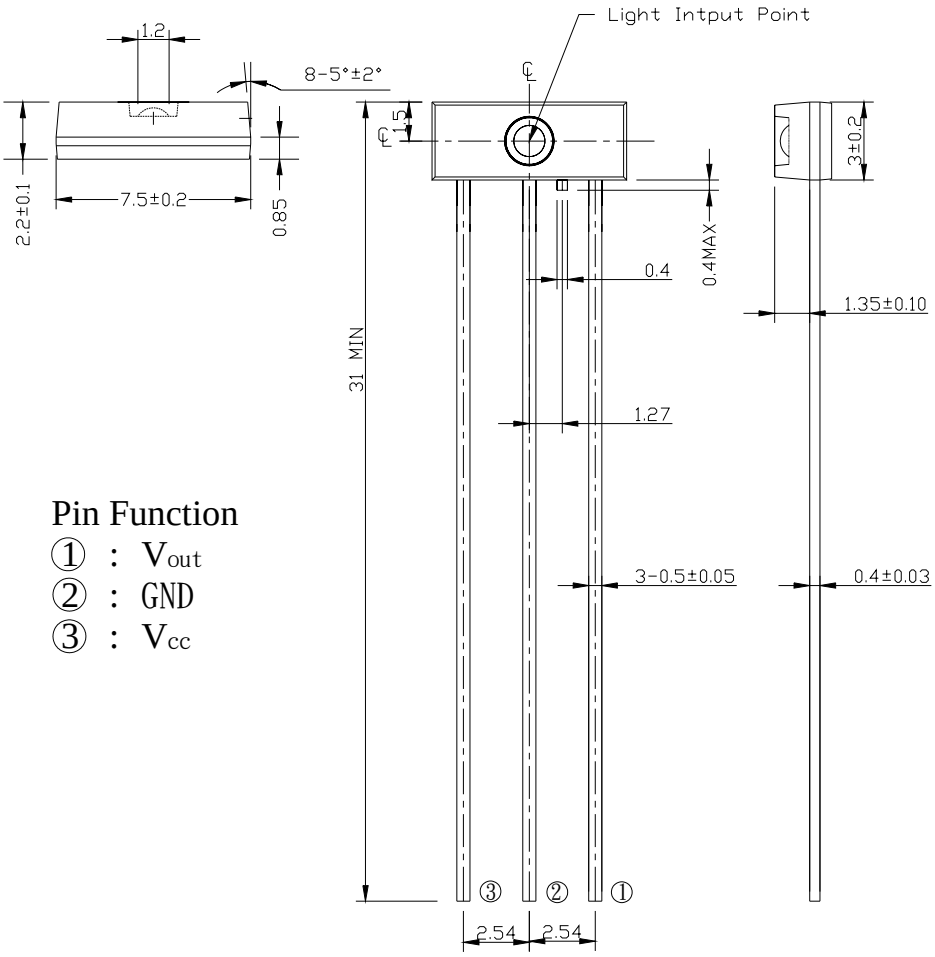
The unit functions by converting optical signals into electric ones.

The unit is operated at 2.4 ~ 5.5 V and the signal output interface is TTL compatible with high performance at low power consumption.

Applications

1. Digital Optical Data-Link
2. Dolby AC-3 Digital Audio Interface

Package Dimensions



Pin Function
① : V_{out}
② : GND
③ : V_{cc}

Notes: 1.All dimensions are in mm.
2.General Tolerance: Pin length tolerance is ±0.25 mm
others are ±0.10 mm

Absolute Maximum Ratings(Ta = 25 ºC)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 ~ +5.5	V
Output Voltage	Vout	Vcc +0.3	V
Storage Temperature	Tstg	-40 to 85	ºC
Operating Temperature	Topr	-20 to 70	ºC
Soldering Temperature	Tsol	260*	ºC

* Soldering time ≤ 10 s.

Electro-Optical Characteristics(Ta=-20~70℃,Vcc=3V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	Vcc	-	2.40	3.00	5.50	V
Peak sensitivity wavelength	λp	-	-	650	-	nm
Maximum receiver power	Pc,max	Refer to Fig.1	-	-	-14	dBm
Minimum receiver power	Pc,min	Refer to Fig.1	-27	-	-	dBm
Dissipation current	Icc	Refer to Fig.2	-	4	12	mA
High level output voltage	VOH	Refer to Fig.3	2.1	2.5	-	V
Low level output voltage	VOL	Refer to Fig.3	-	0.2	0.4	V
Rise time	tr	Refer to Fig.3		10	20	ns
Fall time	tf	Refer to Fig.3		10	20	ns
Propagation delay Low to High	t_{PLH}	Refer to Fig.3	-	-	120	ns
Propagation delay High to Low	t_{PHL}	Refer to Fig.3	-	-	120	ns
Pulse Width Distortion	Δtw	Refer to Fig.3	-25	-	+25	ns
Jitter	Δtj	Refer to Fig.3, Pc=-14dBm	-	1	15	ns
		Refer to Fig.3, Pc=-27dBm	-	5	20	ns
Transfer rate	T	NRZ signal	0.1	-	16	Mb/s

Measuring Method

*Fig.1 Measuring Method of Maximum and Minimum Input Power that Receiver Unit Need

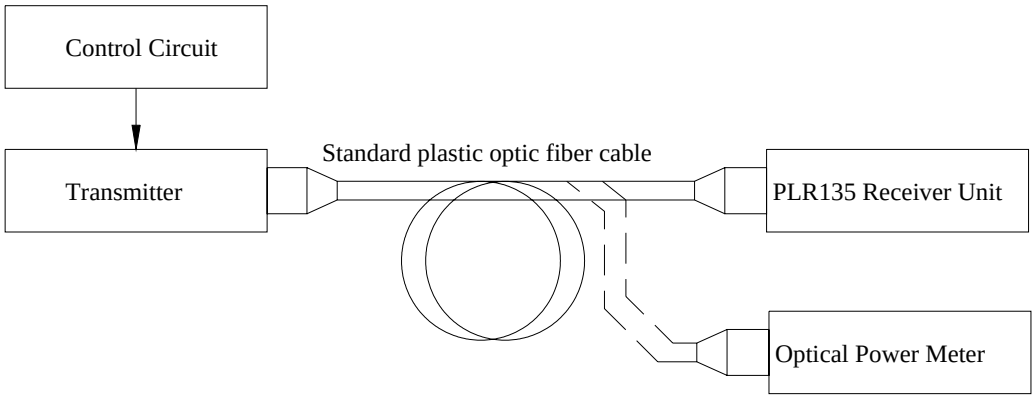


*Fig.2 Measuring Method of Dissipation Current

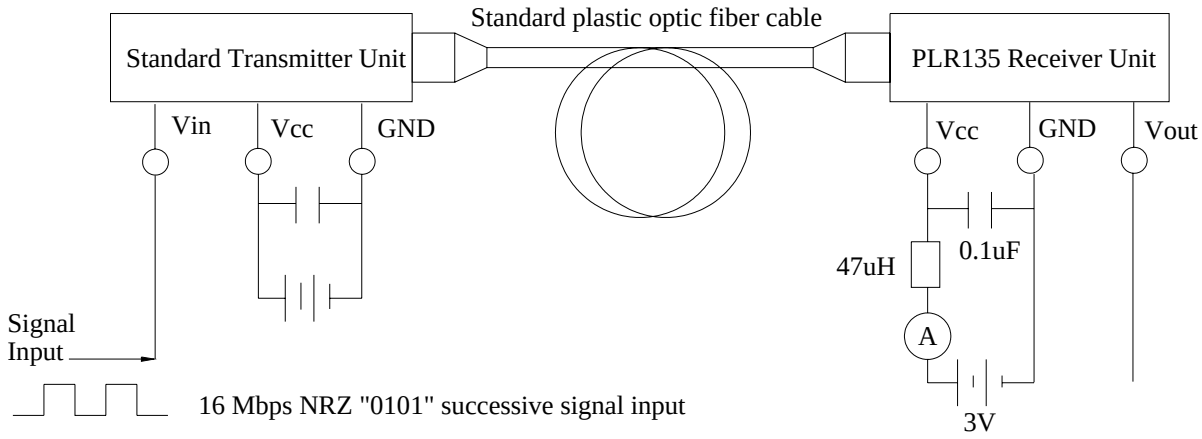
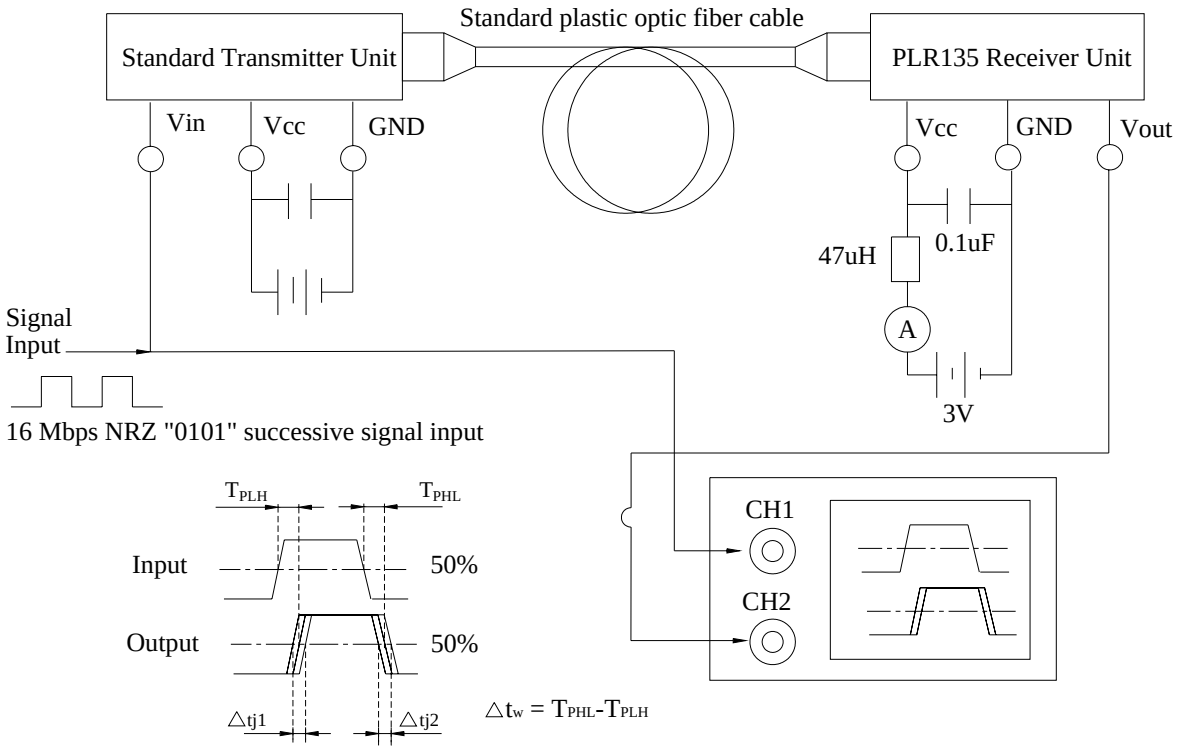
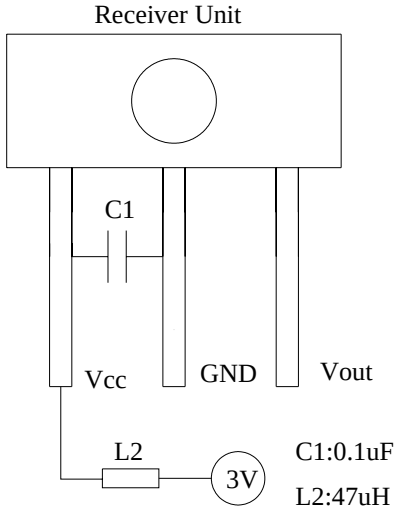


*Fig.3 Measuring Method of Output Voltage, Pulse and Jitter

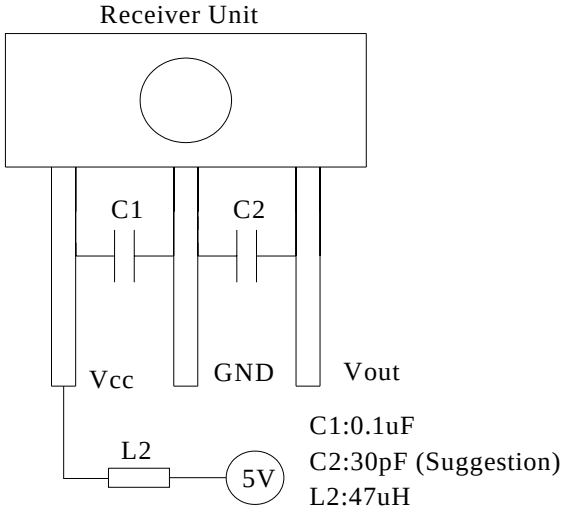


Application Circuit

(1) General application circuit for Vcc=3V



(2) General application circuit for Vcc=5V



Note: For having good coupling, the C1,C2 capacitor must be placed within 7mm

Typical Electro-Optical Characteristics Curves

*Fig.4 Power supply voltage vs. Minimum receiver power

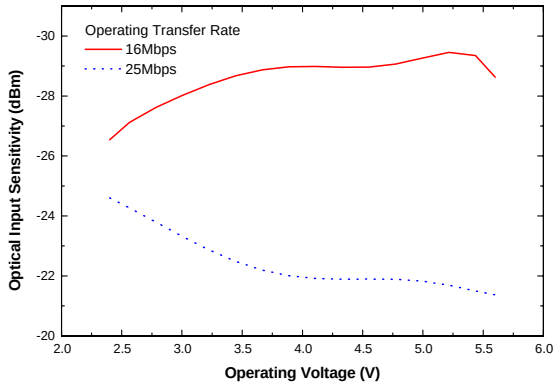
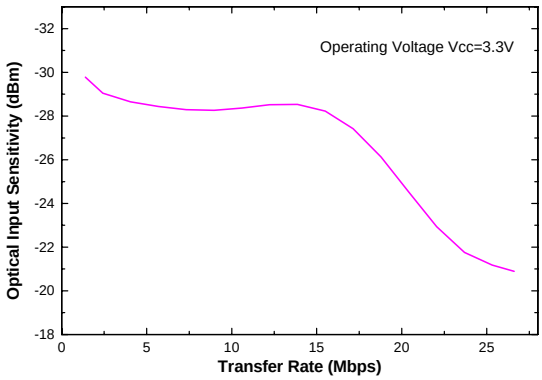


*Fig.5 Transfer rate vs. Minimum receiver power



Note: Before using the PLR135 device, please confirm the minimum sensitivity at different operating voltage and transmission rate.

RELIABILITY TEST ITEMS

No.	Item	Test Condition	Test Hour/Cycle	Sample Size (Piece)	Number (n) Failure (c)
1	Soldering Heat	260°C±5°C	10 seconds	22	n=22, c=0
2	High Temp. Storage	Ta=100°C	1000hrs	22	n=22, c=0
3	Low Temp. Storage	Ta=-55°C	1000hrs	22	n=22, c=0
4	High Temp. & Humid. Test	Ta=85°C, RH=85%	1000hrs	22	n=22, c=0
5	Temperature Cycle	-55°C ~~~~ 85°C (30min) (5min) (30min)	300cycle	22	n=22, c=0
6	Thermal Shock	-10°C ~~~~ 100°C (5min) (10sec) (5min)	300cycle	22	n=22, c=0
7	DC Operating Life	Vcc=3V, Ta=25°C	1000hrs	22	n=22, c=0

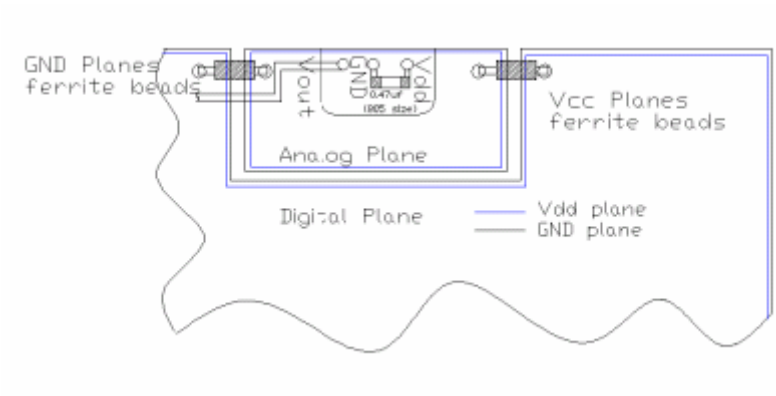
Application Notes: PLR135 Series PCB layout for motherboard integration

To achieve better jitter and low input optical power performances, several PCB layout guidelines must be followed. These guidelines ensure the most reliable PLR135 POF performance for the motherboard integration. Failed to implement these PCB guidelines may affect the PLR135 jitter and low input power performances.

1. Careful decoupling of the power supplies is very important. Place a 0.1uf surface mount (size 805 or smaller) capacitor as close as (less than 2cm) to the POF Vdd and Gnd leads. The 0.1uf act as a low impedance path to ground for any stray high frequency transient noises.

2. To reduce the digital noises form the digital IC on the motherboard, the planar capacitance formed by an isolated Vcc and Gnd planes is critical. The POF device must be mounted directly on these two planes to reduce the lead parasitic inductance.

3. The isolated Vdd and Gnd planes must be connected to the main Vcc and Gnd (digital) planes at a single point using ferrite beads. The beads are used to block the high frequency noises from the digital planes while still allowing the DC connections between the planes



EVERLIGHT ELECTRONICS CO., LTD.
Office: No 25, Lane 76, Sec 3, Chung Yang Rd,
Tucheng, Taipei 236, Taiwan, R.O.C
Tel: 886-2-2267-2000, 2267-9936
Fax: 886-2267-6244, 2267-6189, 2267-6306
http://www.everlight.com