AAT2500M
400mA Step-Down Converter and 300mA LDO

SystemPower™

General Description

The AAT2500M is a high efficiency 400mA step-down converter and 300mA low dropout (LDO) linear regulator for applications where power efficiency and solution size are critical. The typical input power source can be a single-cell Lithium-ion/polymer battery or a 5V or 3.3V power bus.

The step-down converter is capable of delivering up to 400mA output current, uses a typical switching frequency of 1.8MHz to greatly reduce the size of external components, offers high speed turn-on and maintains a low 25µA no load quiescent current.

The LDO is capable of delivering up to 300mA output current.

The AAT2500M is available in the Pb-free, space-saving 12-pin TSOPJW package and is rated over the -40°C to +85°C operating temperature range.

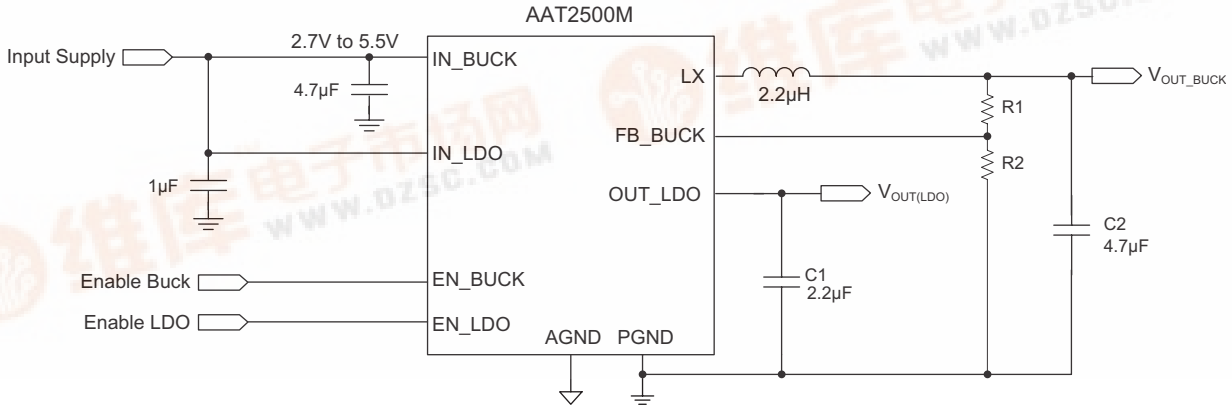
Features

- V_{IN} Range: 2.7V to 5.5V
- Output Current:
  - — Step-Down Converter: 400mA
  - — LDO: 300mA
- Low Quiescent Current
  - — 130µA Combined for Both Step-Down Converter plus LDO
- 90% Efficient Step-down Converter (at 100mA)
- Integrated Power Switches
- 100% Duty Cycle
- 1.8MHz Switching Frequency
- Current Limit Protection
- Automatic Soft-Start
- Over Temperature Protection
- TSOPJW-12 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Micro Hard Disc Drives
- Microprocessor / DSP Core / IO Power
- Optical Storage Devices
- PDAs and Handheld Computers
- Portable Media Players

Typical Application

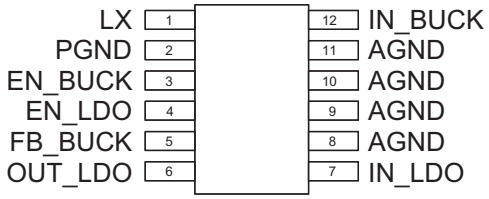


Pin Descriptions

Pin #	Symbol	Function
1	LX	Step-down converter switching node.
2	PGND	Power ground for step-down converter.
3	EN_BUCK	Enable pin for step-down converter.
4	EN_LDO	Enable pin for LDO.
5	FB_BUCK	Feedback input pin for step-down converter. Regulated at 0.6V for adjustable version.
6	OUT_LDO	LDO power output.
7	IN_LDO	Input supply voltage for LDO.
8, 9, 10, 11	AGND	Analog signal ground.
12	IN_BUCK	Input supply voltage for step-down converter.

Pin Configuration

TSOPJW-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_P	Input Voltage	-0.3 to 6.0	V
AGND, PGND	Ground Pins	-0.3 to +0.3	V
V_{EN}, V_{FB}	Enable and Feedback Pins	V_{IN} + 0.3	V
I_{OUT}	Maximum DC Output Current (continuous)	1000	mA
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance[2]	110	°C/W
P_D	Maximum Power Dissipation	909	mW

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

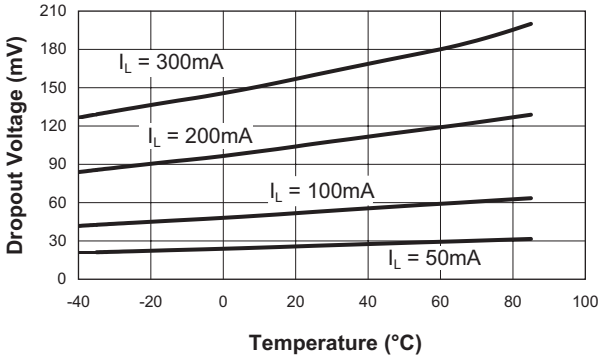
V_{IN_BUCK} = V_{IN_LDO} = 5.0V. T_A = -40°C to +85°C unless noted otherwise. Typical values are at T_A = +25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{INBUCK}, V_{INLDO}	Input Voltage		2.7		5.5	V
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising			2.7	V
		V_{IN} Falling		2.35		V
I_Q	Quiescent Current	V_{EN} = V_{IN}, No Load		130		µA
I_{SHDN}	Shutdown Current	V_{EN} = GND			1.0	µA
Step-Down Converter						
V_{FB}	Feedback Voltage Tolerance	No Load, T_A = 25°C	0.591		0.609	V
		I_{OUT} = 0 to 400mA; V_{IN} = 2.7 to 5.5V	-3		+3	%
I_{LXLEAK}	LX Reverse Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}, V_{EN} = GND	-1.0		1.0	µA
I_{FB}	Feedback Leakage	V_{FB} = 1.0 V			0.2	µA
I_{LIM}	P-Channel Current Limit			1.2		A
$R_{DS(ON)H}$	High Side Switch On Resistance			0.4		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.25		Ω
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{LOAD} = 0 to 400mA		0.25		%
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.3		%
F_{OSC}	Oscillator Frequency			1.8		MHz
T_S	Start-Up Time	From Enable to Output Regulation		120		µs
LDO (V_{OUT} = 3.3V)						
V_{OUT}	Output Voltage Tolerance	No Load, 25°C	3.24	3.30	3.36	V
V_{OUT}	Output Voltage Range	I_{OUT} = 0 to 300mA	-3		3	%
V_{IN}	Input Voltage		V_{OUT} + V_{DO}[2]		5.5	V
I_{OUT}	Output Current		300			mA
I_{LIM}	Current Limit			1		A
V_{DO}	Dropout Voltage[3]	I_{OUT} = 300mA		160	240	mV
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{LOAD} = 0 to 300mA		1.2		%
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	V_{IN} = 3.7V to 5.5V		0.6		%
T_S	Start-Up Time	From Enable to Output Regulation		100		µs
Logic Signals						
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.5			V
$I_{EN(H)}$	Enable Current Consumption		-1.0		1.0	µA
T_{SD}	Over-Temperature Shutdown Threshold			150		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C

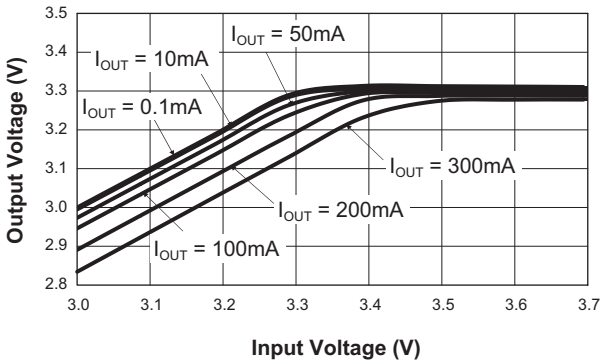
1. Specification over the -40°C to +85°C operating temperature ranges is assured by design, characterization and correlation with statistical process controls.
2. To calculate the minimum LDO input voltage, use the following equation: $V_{IN(MIN)}$ = $V_{OUT(MAX)}$ + $V_{DO(MAX)}$.
3. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.

Typical Characteristics

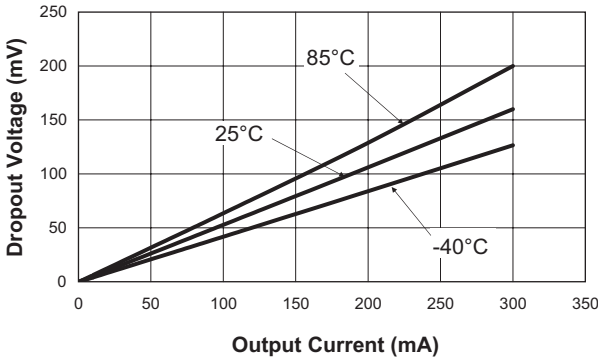
LDO Dropout Voltage vs. Temperature



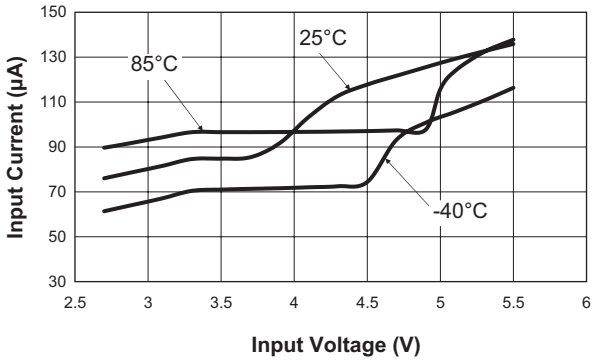
LDO Dropout Characteristics
(V_{OUT} = 3.3V)



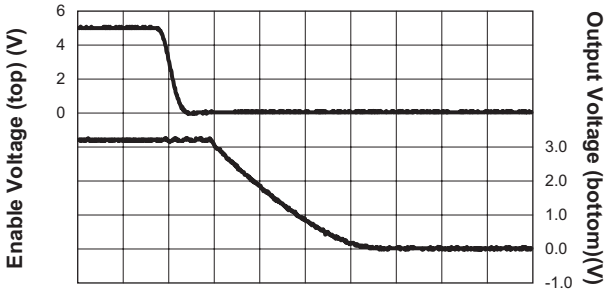
LDO Dropout Voltage vs. Output Current



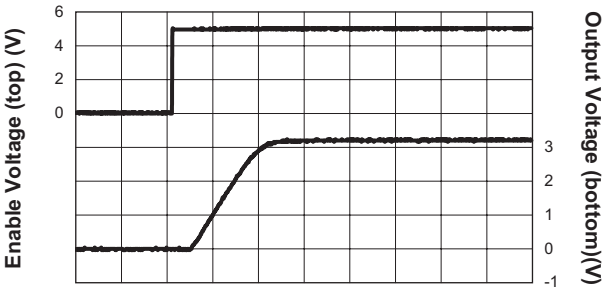
No Load Quiescent Current vs. Input Voltage
(EN_BUCK = EN_LDO = V_{IN})



LDO Turn-Off Response Time
(V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 300mA)

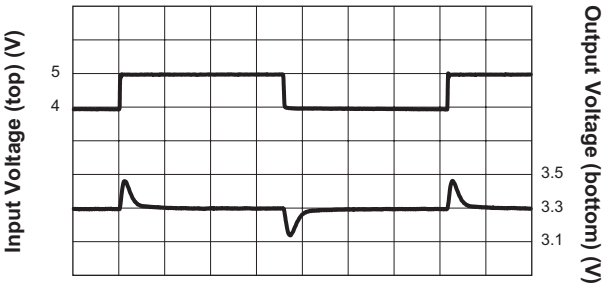


LDO Turn-On Time From Enable
(V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 300mA)



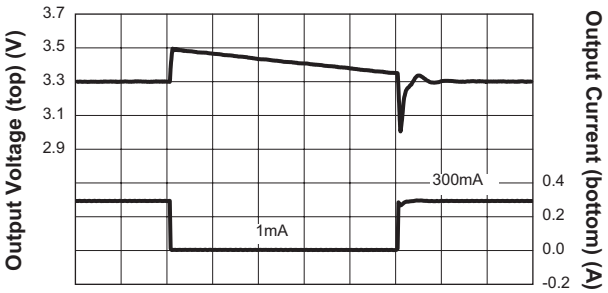
Typical Characteristics

LDO Line Transient Response
(V_{IN} = 4V to 5V; V_{OUT} = 3.3V; I_{OUT} = 300mA; C_{OUT} = 4.7µF)



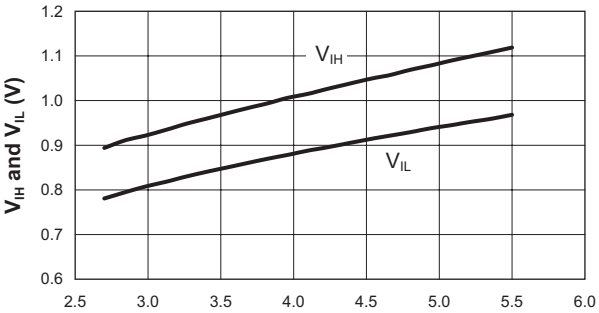
Time (40µs/div)

LDO Load Transient Response
(1mA to 300mA; V_{IN} = 5V; V_{OUT} = 3.3V; C_{OUT} = 4.7µF)

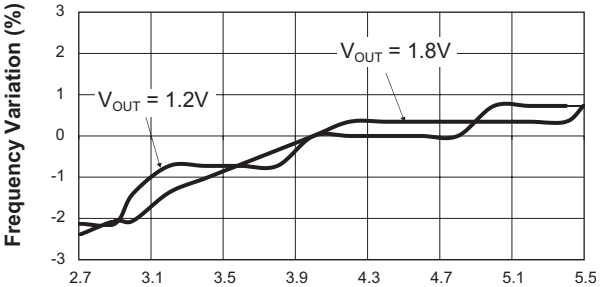


Time (100µs/div)

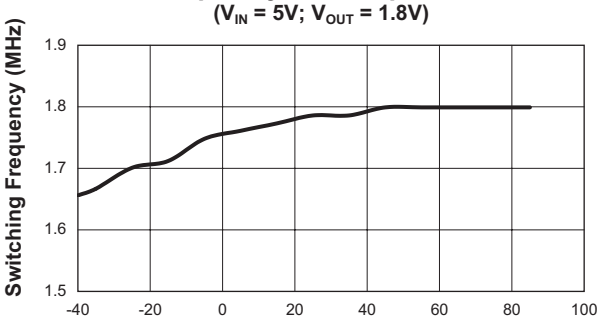
LDO V_{IH} and V_{IL} vs. Input Voltage



Step-Down Converter Switching Frequency vs. Input Voltage
(I_{OUT} = 400mA)

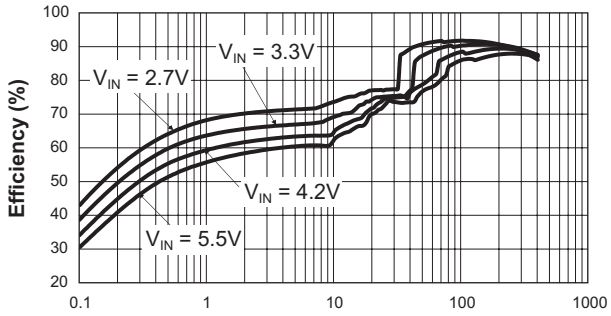


Step-Down Converter Switching Frequency vs. Temperature
(V_{IN} = 5V; V_{OUT} = 1.8V)

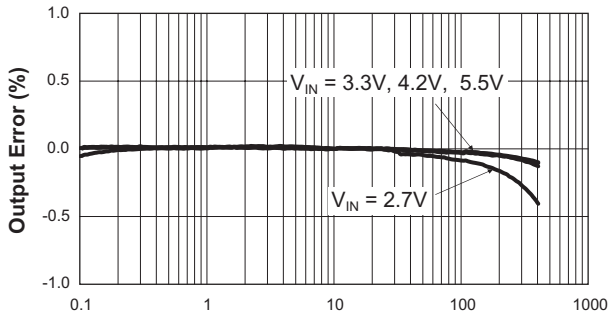


Typical Characteristics

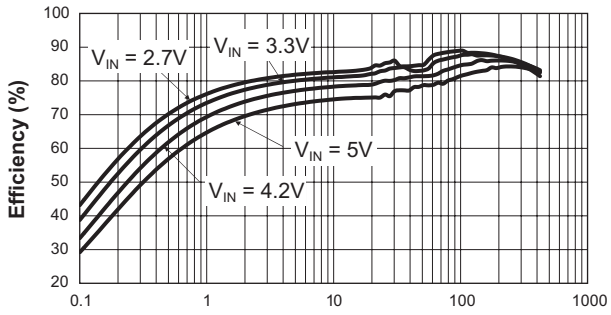
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.8V; L = 2.2µH)



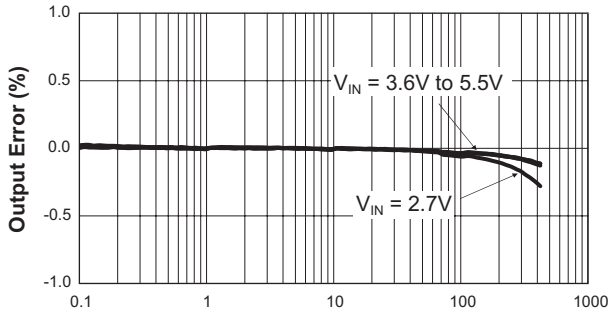
Step-Down Converter DC Regulation
(V_{OUT} = 1.8V; L = 2.2µH)



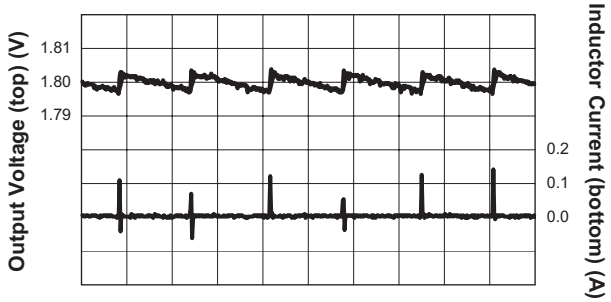
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.2V; L = 2.2µH)



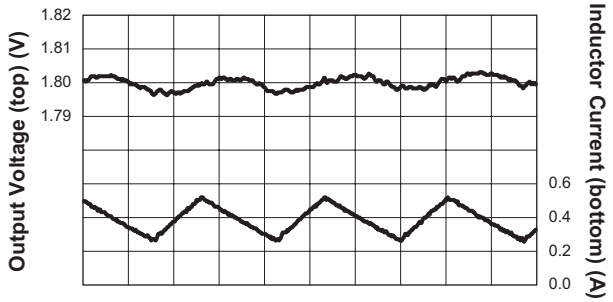
Step-Down Converter DC Regulation
(V_{OUT} = 1.2V; L = 2.2µH)



Step-Down Converter Output Ripple
(V_{OUT} = 1.8V; V_{IN} = 5V; I_{OUT} = 1mA)

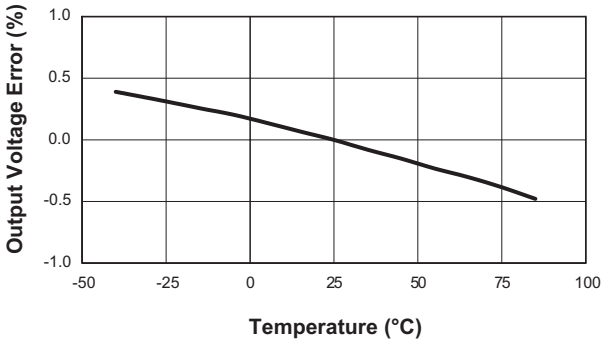


Step-Down Converter Output Ripple
(V_{OUT} = 1.8V; V_{IN} = 5V; I_{OUT} = 400mA)

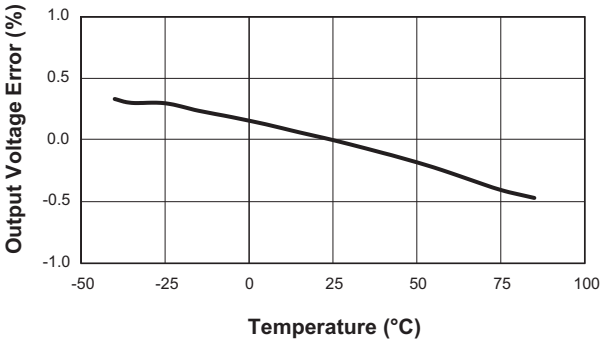


Typical Characteristics

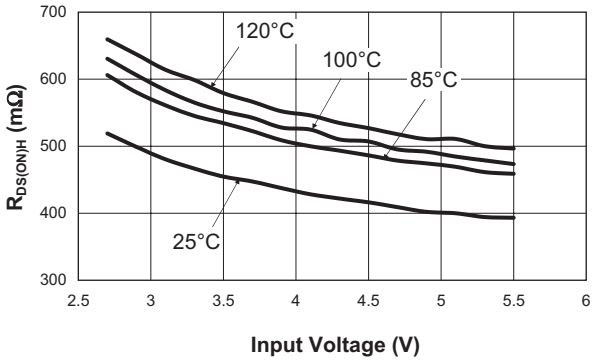
Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 5V; V_{OUT} = 1.8V; I_{OUT} = 400mA)



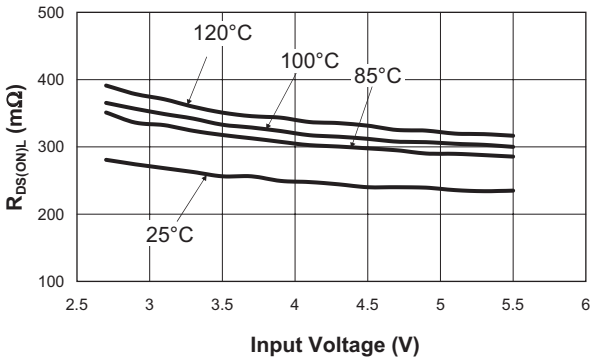
Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 5V; V_{OUT} = 1.2V; I_{OUT} = 400mA)



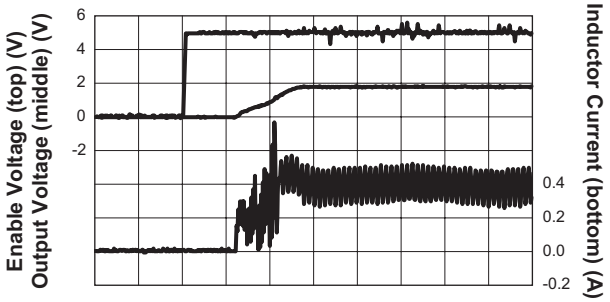
Step-Down Converter P-Channel $R_{DS(ON)H}$ vs. Input Voltage



Step-Down Converter N-Channel $R_{DS(ON)L}$ vs. Input Voltage

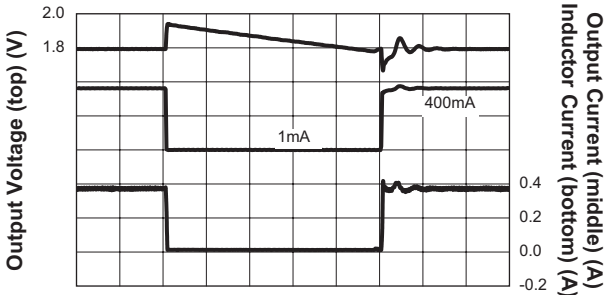


Step-Down Converter Soft Start
(V_{IN} = 5V; V_{OUT} = 1.8V; I_{OUT} = 400mA; C_{FF} = Open)



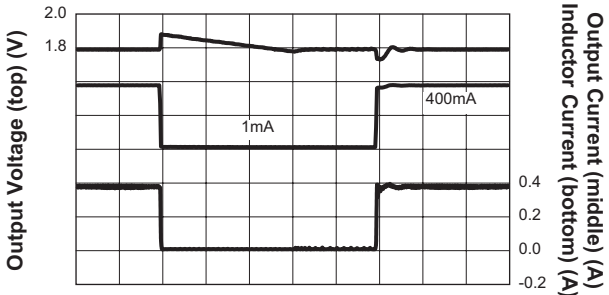
Typical Characteristics

Step-Down Converter Load Transient Response
(1mA to 400mA; V_{IN} = 5V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF)



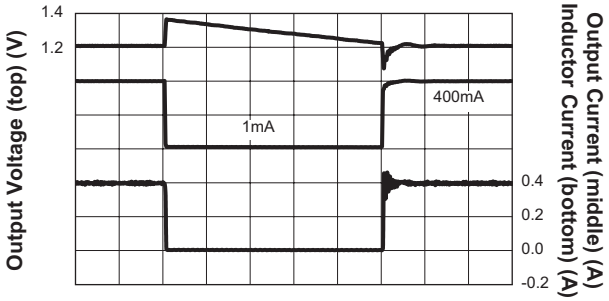
Time (100µs/div)

Step-Down Converter Load Transient Response
(1mA to 400mA; V_{IN} = 5V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF; C_{FF} = 100pF)



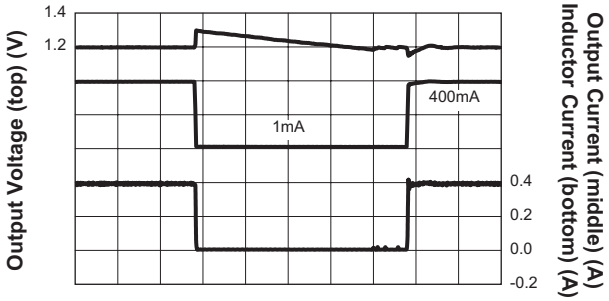
Time (100µs/div)

Step-Down Converter Load Transient Response
(1mA to 400mA; V_{IN} = 5V; V_{OUT} = 1.2V; C_{OUT} = 4.7µF)



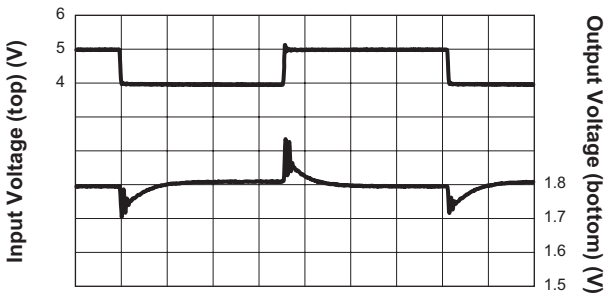
Time (100µs/div)

Step-Down Converter Load Transient Response
(1mA to 400mA; V_{IN} = 5V; V_{OUT} = 1.2V; C_{OUT} = 4.7µF; C_{FF} = 100pF)



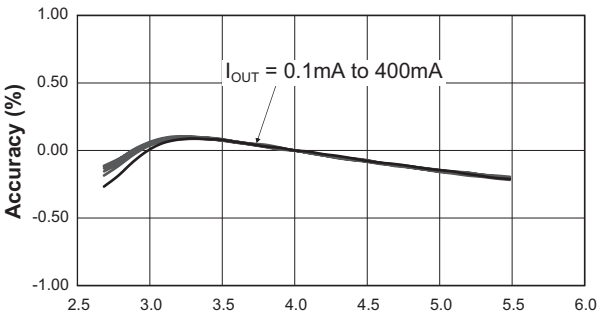
Time (100µs/div)

Step-Down Converter Line Transient Response
(V_{IN} = 4V to 5V; V_{OUT} = 1.8V; I_{OUT} = 400mA; C_{OUT} = 4.7µF)



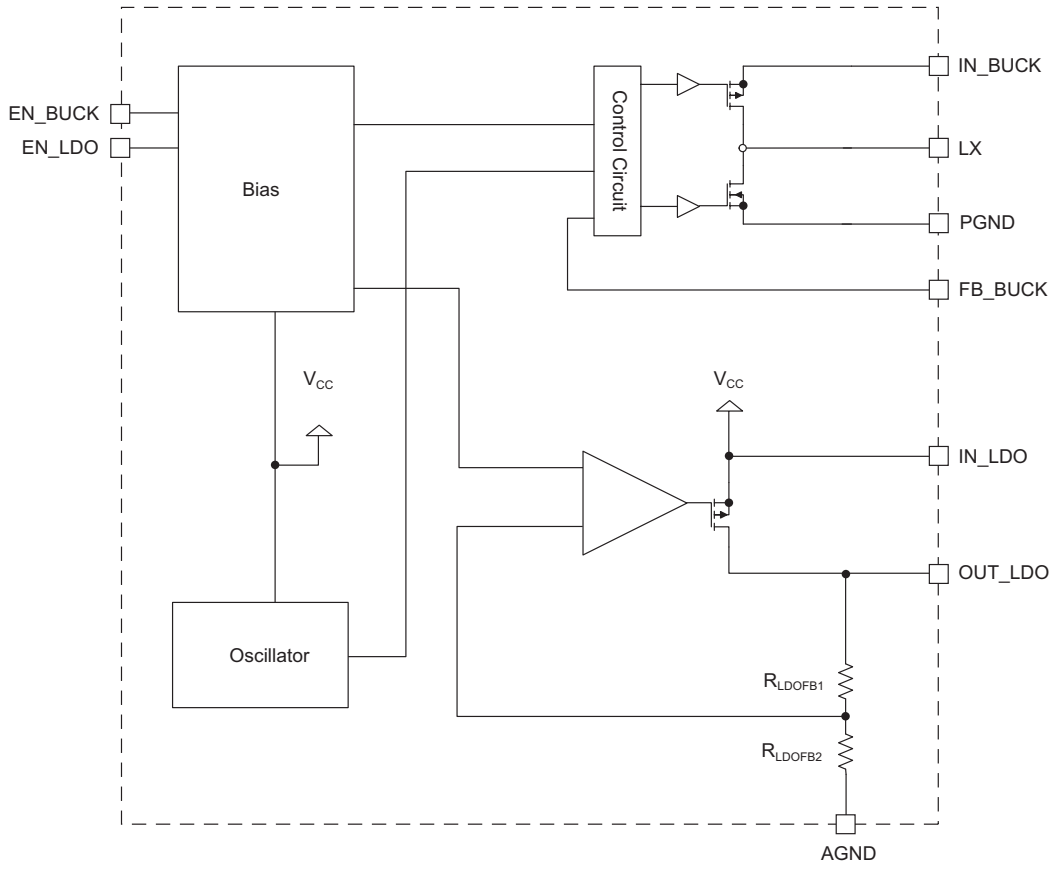
Time (40µs/div)

Step-Down Converter Line Regulation
(V_{OUT} = 1.2V; L = 2.2µH)



Input Voltage (V)

Functional Block Diagram



Functional Description

The AAT2500M is a high performance power management IC comprised of a buck converter and a linear regulator. The buck converter is a high efficiency converter capable of delivering up to 400mA. Operating at 1.8MHz, the converter requires only three external power components (C_{IN}, C_{OUT}, and L_X) and is stable with a ceramic output capacitor. The linear regulator delivers 300mA and is also stable with ceramic capacitors.

Linear Regulator

The advanced circuit design of the linear regulator has been specifically optimized for very fast start-up and shutdown timing. This proprietary LDO has also been tailored for superior transient response characteristics. These traits are particularly important for applications that require fast power supply timing.

The high-speed turn-on capability is enabled through implementation of a fast-start control cir-

cuit, which accelerates the power-up behavior of fundamental control and feedback circuits within the LDO regulator. Fast turn-off time response is achieved by an active output pull-down circuit, which is enabled when the LDO regulator is placed in shutdown mode. This active fast shut-down circuit has no adverse effect on normal device operation. The LDO regulator output has been specifically optimized to function with low-cost, low-ESR ceramic capacitors; however, the design will allow for operation over a wide range of capacitor types.

The regulator comes with complete short-circuit and thermal protection. The combination of these two internal protection circuits gives a comprehensive safety system to guard against extreme adverse operating conditions.

The regulator features an enable/disable function. This pin (EN_LDO) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN_LDO turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN_LDO pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN_LDO} to keep the LDO regulator in a continuously on state.

The IN_LDO input powers the internal reference, oscillator, and bias control blocks. For this reason, the IN_LDO input must be connected to the input power source to provide power to both the LDO and step-down converter functions.

When the regulator is in shutdown mode, an internal 1.5kΩ resistor is connected between OUT and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5KΩ resistor has no adverse impact on device turn-on time.

Step-Down Converter

The AAT2500M buck is a constant frequency peak current mode PWM converter with internal compensation. It is designed to operate with an input voltage range of 2.7V to 5.5V. The output voltage ranges from 0.6V to the input voltage. The 0.6V fixed model shown in Figure 1 is also the adjustable version and is externally programmable with a resistive divider, as shown in Figure 2. The converter MOSFET power stage is sized for 400mA load capability with up to 92% efficiency. Light load efficiency is close to 80% at a 500µA load.

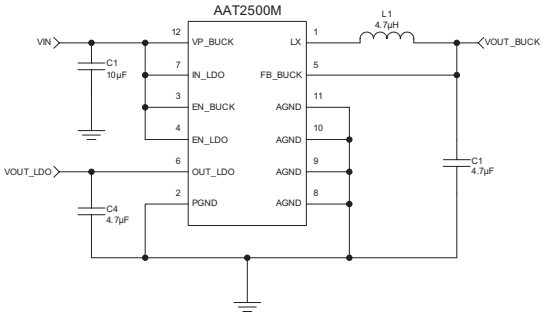


Figure 1: AAT2500M Fixed Output.

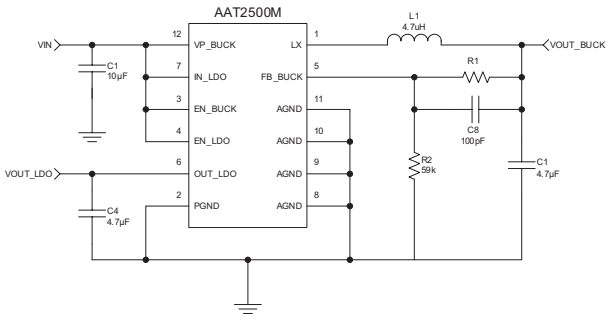


Figure 2: AAT2500M with Adjustable Step-Down Output and Enhanced Transient Response.

Soft Start

The AAT2500M soft-start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. When pulled low, the enable input forces the converter into a low-power, non-switching state with a bias current of less than 1µA.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As 100% duty cycle is approached, the minimum off-time initially forces the high side on-time to exceed the 1.8MHz clock cycle and reduce the effective switching frequency. Once the input drops below the level where the output can be regulated, the high side P-channel MOSFET is turned on continuously for 100% duty cycle. At 100% duty cycle, the output voltage tracks the input voltage minus the IR drop of the high side P-channel MOSFET $R_{DS(ON)}$.

Low Supply

The under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Fault Protection

For overload conditions, the peak inductor current is limited. Thermal protection disables switching when the internal dissipation or ambient temperature becomes excessive. The junction over-temperature threshold is 150°C with 15°C of hysteresis.

Applications Information

LDO Regulator

Input and Output Capacitors: An input capacitor is not required for basic operation of the linear regulator. However, if the AAT2500M is physically located at a reasonable distance from an input power source, an input capacitor (C3) will be needed for stable operation. Typically, a 1µF or larger capacitor is recommended for C3 in most applications. C3 should be located as closely to the input voltage (IN_LDO) pin as practically possible.

An input capacitor greater than 1µF will offer superior input line transient response and maximize power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C3. There is no specific capacitor ESR requirement for C3. However, for 300mA LDO regulator output operation, ceramic capacitors are recommended for C3 due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

For proper load voltage regulation and operational stability, a capacitor is required between the OUT_LDO and AGND pins. The output capacitor (C4) connection to the LDO regulator ground pin should be made as directly as practically possible for maximum device performance. Since the regulator has been designed to function with very low ESR capacitors, ceramic capacitors in the 1.0µF to 10µF range are recommended for best performance. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection should use 2.2µF or greater for C4. In low output current applications, where output load is less than 10mA, the minimum value for C4 can be as low as 0.47µF.

Equivalent Series Resistance: ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Step-Down Converter

Inductor Selection: The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low-voltage fixed versions of the AAT2500M is 0.24A/µsec. This equates to a slope compensation that is 35% of the inductor current down slope for a 1.5V output and 2.2µH inductor.

$$m = \frac{0.35 \cdot V_O}{L} = \frac{0.35 \cdot 1.5V}{2.2\mu H} = 0.24 \frac{A}{\mu sec}$$

This is the internal slope compensation for the adjustable (V_O = 0.6V) version or low output voltage fixed versions. When externally programming the 0.6V version to 2.5V, the calculated inductance is 3.75µH.

$$L = \frac{0.35 \cdot V_O}{m} = \frac{0.35 \cdot V_O}{0.24A \frac{A}{\mu sec}} \approx 1.5 \frac{\mu sec}{A} \cdot V_O$$

$$= 1.5 \frac{\mu sec}{A} \cdot 2.5V = 3.75\mu H$$

In this case, a standard 4.7µH value is selected.

For high output voltage fixed versions (2.5V and above), m = 0.48A/µsec. Table 1 displays inductor values for the AAT2500M fixed and adjustable options.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 2.2µH CDRH3D16 series inductor selected from Sumida has a 59mΩ DCR and a 1.3A DC current rating. At full load, the inductor DC loss is 9.4mW which gives a 1.5% loss in efficiency for a 400mA, 1.5V output.

Configuration	Output Voltage	Inductor	Slope Compensation
0.6V Adjustable With External Resistive Divider	0.6V to 2.0V	2.2µH	0.24A/µsec
	2.5V	4.7µH	0.24A/µsec
Fixed Output	0.6V to 2.0V	2.2µH	0.24A/µsec
	2.5V to 3.3V	2.2µH	0.48A/µsec

Table 1: Inductor Values.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C2. The calculated value varies with input voltage and is a maximum when V_{IN_BUCK} is double the output voltage (V_O).

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_{OSC}}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_{OSC}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load (output) current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_{IN_BUCK} is twice V_{OUT_BUCK}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2500M. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C2) can be seen in the evaluation board layout in Figure 3.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

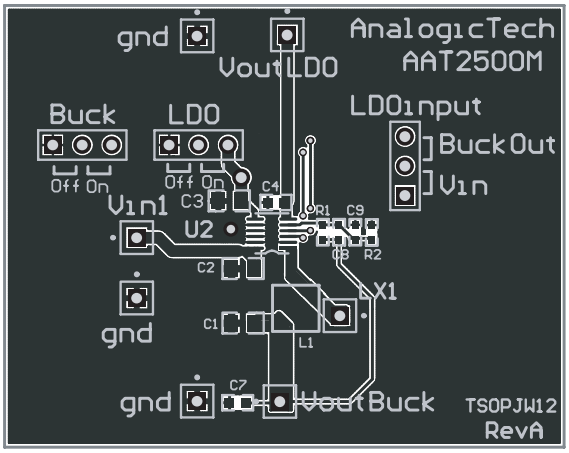


Figure 3: AAT2500M Evaluation Board Top Side.

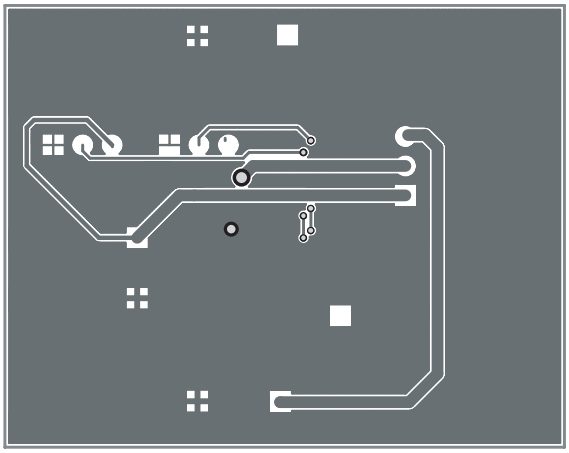


Figure 4: AAT2500M Evaluation Board Bottom Side.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The step-down converter output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_{OSC}}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_{OSC} \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Adjustable Output Voltage Resistor Selection

For applications requiring an adjustable output voltage (V_O or V_{OUT}), the 0.6V version can be externally programmed. Resistors R1 and R2 of Figure 5 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2

is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

The adjustable version of the AAT2500M, combined with an external feedforward capacitor (C8 in Figures 2 and 5), delivers enhanced transient response for extreme pulsed load applications. The addition of the feedforward capacitor typically requires a larger output capacitor C1 for stability.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 221kΩ R1 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715

Table 2: Adjustable Resistor Values For Use With 0.6V Step-Down Converter.

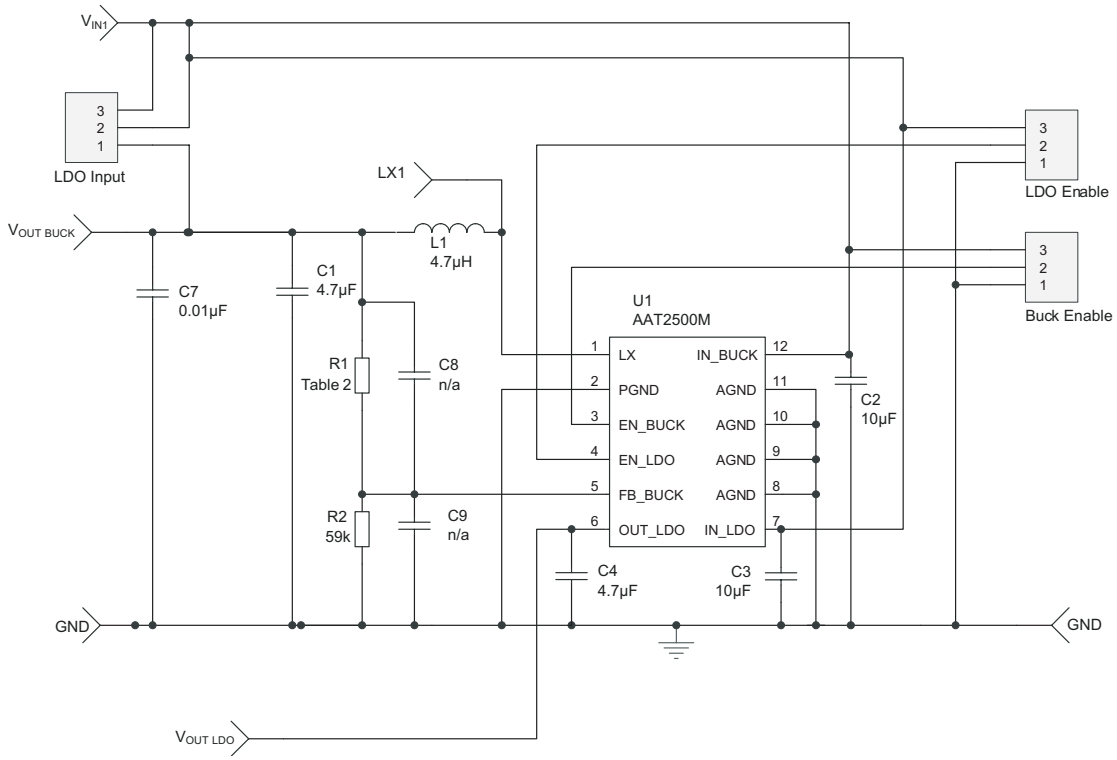


Figure 5: AAT2500M Evaluation Board Schematic.

Thermal Calculations

There are three types of losses associated with the AAT2500M step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the step-down converter and LDO losses is given by:

$$P_{TOTAL} = \frac{I_{OBUCK}^2 \cdot (R_{DSON(HS)} \cdot V_{OBUCK} + R_{DSON(LS)} \cdot [V_{IN} - V_{OBUCK}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_{OSC} \cdot I_{OBUCK} + I_{QBUCK} + I_{QLDO}) \cdot V_{IN} + I_{OLDO} \cdot (V_{IN} - V_{OLDO})$$

I_{QBUCK} is the step-down converter quiescent current and I_{QLDO} is the LDO quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the buck converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{OBUCK}^2 \cdot R_{DSON(HS)} + I_{OLDO} \cdot (V_{IN} - V_{OLDO})$$

$$+ (I_{QBUCK} + I_{QLDO}) \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TSOPJW-12 package which is 110°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

PCB Layout

The following guidelines should be used to ensure a proper layout.

1. The input capacitor C2 should connect as closely as possible to IN_BUCK and PGND, as shown in Figure 5.
2. The output capacitor and inductor should be connected as closely as possible. The connection of the inductor to the LX pin should also be as short as possible.
3. The feedback trace should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB_BUCK pin. This prevents noise from being coupled into the high impedance feedback node.
4. The resistance of the trace from the load return to GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Step-Down Converter Design Example

Specifications

V_{OBUCK} = 1.8V @ 400mA (adjustable using 0.6V version), Pulsed Load ΔI_{LOAD} = 300mA

V_{OLDO} = 3.3V @ 300mA

V_{IN} = 2.7V to 4.2V (3.6V nominal)

F_{OSC} = 1.8MHz

T_{AMB} = 85°C

1.8V Buck Output Inductor

$$L1 = 1.5\,\frac{\mu sec}{A} \cdot V_{OBUCK} = 1.5\,\frac{\mu sec}{A} \cdot 1.8V = 2.7\mu H \quad \text{(see Table 1)}$$

For Sumida inductor CDRH3D16, 2.2µH, DCR = 59mΩ.

$$\Delta I_{L1} = \frac{V_{OBUCK}}{L1 \cdot F} \cdot \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right) = \frac{1.8V}{2.2\mu H \cdot 1.8MHz} \cdot \left(1 - \frac{1.8V}{4.2V}\right) = 260mA$$

$$I_{PKL1} = I_{OBUCK} + \frac{\Delta I_{L1}}{2} = 0.4A + 0.130A = 0.53A$$

$$P_{L1} = I_{OBUCK}^2 \cdot DCR = (0.4A)^2 \cdot 59m\Omega = 9.4mW$$

1.8V Output Capacitor

V_{DROOP} = 0.2V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_{OSC}} = \frac{3 \cdot 0.3A}{0.2V \cdot 1.8MHz} = 2.5\mu F$$

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OBUCK}) \cdot (V_{IN(MAX)} - V_{OBUCK})}{L1 \cdot F_{OSC} \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{2.2\mu H \cdot 1.8MHz \cdot 4.2V} = 75mA_{RMS}$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (75mA)^2 = 28.1\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{OBUCK}} - ESR\right) \cdot 4 \cdot F_{OSC}} = \frac{1}{\left(\frac{25mV}{0.4A} - 5m\Omega\right) \cdot 4 \cdot 1.8MHz} = 2.42\mu F$$

$$I_{RMS} = \frac{I_{OBUCK}}{2} = 0.2A_{RMS}$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.2A)^2 = 0.2mW$$

AAT2500M Losses

$$P_{TOTAL} = \frac{I_{OBUCK}^2 \cdot (R_{DSON(HS)} \cdot V_{OBUCK} + R_{DSON(LS)} \cdot [V_{IN} - V_{OBUCK}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_{OSC} \cdot I_{OBUCK} + I_{QBUCK} + I_{QLDO}) \cdot V_{IN} + (V_{IN} - V_{LDO}) \cdot I_{LDO}$$

$$= \frac{(0.4A)^2 \cdot (0.725\Omega \cdot 1.8V + 0.7\Omega \cdot [4.2V - 1.8V])}{4.2V}$$

$$+ (5ns \cdot 1.8MHz \cdot 0.4A + 50\mu A + 125\mu A) \cdot 4.2V + (4.2V - 3.3V) \cdot 0.3A = 399mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (110°C/W) \cdot 399mW = 129°C$$

V_{OUT} (V)	R1 (kΩ)	R1 (kΩ)	L1 (µH)
Adjustable Version (0.6V device)	**R2 = 59kΩ**	**R2 = 221kΩ[1]**	
0.8	19.6	75.0	2.2
0.9	29.4	113	2.2
1.0	39.2	150	2.2
1.1	49.9	187	2.2
1.2	59.0	221	2.2
1.3	68.1	261	2.2
1.4	78.7	301	2.2
1.5	88.7	332	2.2
1.8	118	442	2.2
1.85	124	464	2.2
2.0	137	523	2.2 or 3.3
2.5	187	715	4.7
V_{OUT} (V)	R1 (kΩ)		L1 (µH)
Fixed Version	**R2 Not Used**		
0.6-3.3V	0		2.2

Table 3: Evaluation Board Component Values.

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH3D16-4R7	4.7	0.90	0.11	3.8x3.8x1.8	Shielded
Sumida	CDRH3D161HP-2R2	2.2	1.30	0.059	4.0x4.0x1.8	Shielded
MuRata	LQH32CN4R7M23	4.7	0.45	0.20	2.5x3.2x2.0	Non-Shielded
MuRata	LQH32CN2R2M23	2.2	0.60	0.13	2.5x3.2x2.0	Non-Shielded
Coilcraft	LPO3310-222	2.2	1.10	0.15	3.3x3.3x1.0	Non-Shielded
Coilcraft	LPO3310-472	4.7	0.80	0.27	3.3x3.3x1.0	Non-Shielded
Coiltronics	SD3118-4R7	4.7	0.98	0.122	3.1x3.1x1.85	Shielded

Table 4: Typical Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
MuRata	GRM21BR61A475KA73L	4.7µF	10V	X5R	0805
MuRata	GRM18BR60J475KE19D	4.7µF	6.3V	X5R	0603
MuRata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805
MuRata	GRM21BR60J226ME39	22µF	6.3V	X5R	0805

Table 5: Surface Mount Capacitors.

1. For reduced quiescent current R2 = 221kΩ.

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	Buck Converter	LDO		
TSOPJW-12	Adj ≥ 0.6V	3.3V	XLXYY	AAT2500MITP-AW-T1

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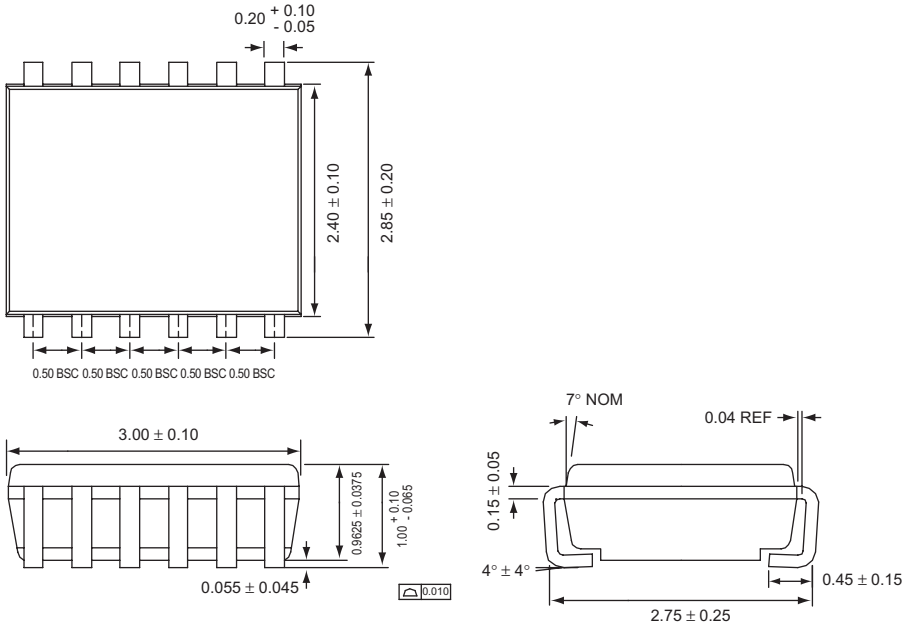
Legend	
Voltage	Code
Adjustable (0.6V)	A
0.9	B
1.2	E
1.5	G
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W
4.2	C

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. Contact Sales for availability.

Package Information

TSOPJW-12



All dimensions in millimeters.

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