DC to 1000 MHz IF Gain Block

ADL5530

FEATURES

Fixed gain of 16.5 dB
Operation up to 1000 MHz
37 dBm Output Third-Order Intercept (OIP3)
3 dB noise figure
Input/output internally matched to 50 Ω
Stable temperature and power supply
3 V or 5 V power supply
110 mA power supply current

APPLICATIONS

VCO buffers
General purpose Tx/Rx amplification

FUNCTIONAL BLOCK DIAGRAM

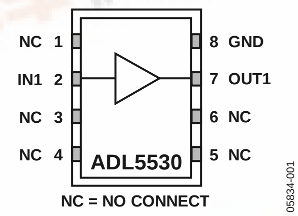

Figure 1.

GENERAL DESCRIPTION

The ADL5530 is a broadband, fixed-gain, linear amplifier that operates at frequencies up to 1000 MHz. The device can be used in a wide variety of wired and wireless devices, including cellular, broadband, CATV, and LMDS/MMDS applications.

The ADL5530 provides a gain of 16.5 dB, which is stable over frequency, temperature, power supply, and from device to device. It achieves an OIP3 of 37 dBm with an output compression point of 21.8 dB and a noise figure of 3 dB.

This amplifier is single-ended and internally matched to 50 Ω with an input return loss of 11 dB. Only input/output ac-coupling capacitors, a power supply decoupling capacitor, and an external inductor are required for operation.

The ADL5530 operates with supply voltages of 3 V or 5 V with a supply current of 110 mA.

The ADL5530 is fabricated on a GaAs pHEMPT process. The device is packaged in a 3 mm × 2 mm LFCSP that uses an exposed paddle for excellent thermal impedance. It operates from −40°C to +85°C. A fully populated evaluation board is also available.

Rev. 0

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REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION (See Table 2)					
Frequency Range[1]		10		1000	MHz
Gain (S21)			16.5		dB
Input Return Loss (S11)			−11		dB
Output Return Loss (S22)			−20		dB
Reverse Isolation (S12)			−21.5		dB
FREQUENCY = 70 MHz					
Gain		15	16.7	18	dB
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±0.1		dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point			21.7		dBm
Output Third-Order Intercept	Δf = 10 MHz , Output Power (P_{OUT}) = 10 dBm per tone		37		dBm
Noise Figure			5		dB
	VPOS = 3 V		3.2		dB
FREQUENCY = 190 MHz					
Gain		15	16.8	18.5	dB
vs. Frequency	± 50 MHz		±0.1		dB
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±0.2		dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point			21.8		dBm
Output Third-Order Intercept	Δf = 10 MHz , P_{OUT} = 10 dBm per tone		37		dBm
Noise Figure			3	4.5	dB
	VPOS = 3 V		2.3		dB
FREQUENCY = 380 MHz					
Gain		14.8	16	17.3	dB
vs. Frequency	± 50 MHz		±0.1		dB
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±0.3	±0.8	dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point		19.5	21.6		dBm
Output Third-Order Intercept	Δf = 10 MHz , P_{OUT} = 10 dBm per tone		36		dBm
Noise Figure			2.5	3.5	dB
	VPOS = 3 V		2		dB
FREQUENCY = 900 MHz					
Gain		13	14.5	16	dB
vs. Frequency	± 50 MHz		±0.2		dB
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±0.5	±1	dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point			21.4		dBm
Output Third-Order Intercept	Δf = 10 MHz , P_{OUT} = 10 dBm per tone		37		dBm
Noise Figure			2.7	3.5	dB
	VPOS = 3 V		2.3		dB
POWER INTERFACE	Pin VPOS				
Supply Voltage (VPOS)		3	5	5.5	V
Supply Current			110	135	mA
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±5		mA
Power Dissipation	VPOS = 5 V		0.55		W
	VPOS = 3 V		0.33		W

[1] For operation at lower frequencies, see the Theory of Operation section.

TYPICAL SCATTERING PARAMETERS

VPOS = 5 V and T_A = 25°C.

Table 2.

Freq. (MHz)	S11			S21			S12			S22			K Factor
	dB	Magnitude	Angle	dB	Magnitude	Angle	dB	Magnitude	Angle	dB	Magnitude	Angle	
10	−7.1	0.44	−34	17.2	7.23	172	−22.5	0.08	22	−17.7	0.13	−69	0.94
20	−9.7	0.33	−26	16.7	6.81	174	−21.9	0.08	12	−24.4	0.06	−73	1.07
50	−11.2	0.28	−16	16.6	6.73	174	−21.7	0.08	4	−31.4	0.03	−42	1.10
100	−11.5	0.27	−13	16.5	6.70	171	−21.6	0.08	1	−30.4	0.03	−23	1.10
150	−11.4	0.27	−14	16.5	6.67	167	−21.6	0.08	−1	−29.3	0.03	−24	1.10
200	−11.5	0.27	−16	16.4	6.59	162	−21.6	0.08	−3	−27.7	0.04	−25	1.11
250	−11.4	0.27	−19	16.3	6.52	157	−21.6	0.08	−4	−26.6	0.05	−25	1.11
300	−11.4	0.27	−23	16.2	6.45	153	−21.6	0.08	−5	−25.1	0.06	−27	1.12
350	−11.3	0.27	−26	16.1	6.36	149	−21.6	0.08	−6	−23.7	0.07	−29	1.12
400	−11.2	0.27	−29	16.0	6.29	144	−21.6	0.08	−7	−22.2	0.08	−32	1.12
450	−11.1	0.28	−32	15.9	6.21	140	−21.6	0.08	−8	−20.7	0.09	−33	1.12
500	−11.1	0.28	−36	15.7	6.11	136	−21.6	0.08	−9	−19.6	0.10	−35	1.12
550	−11.0	0.28	−39	15.6	6.02	132	−21.7	0.08	−10	−18.4	0.12	−37	1.13
600	−10.9	0.29	−42	15.5	5.94	128	−21.7	0.08	−11	−17.3	0.14	−38	1.13
650	−10.8	0.29	−45	15.3	5.84	124	−21.6	0.08	−12	−16.4	0.15	−40	1.12
700	−10.7	0.29	−49	15.2	5.73	119	−21.6	0.08	−13	−15.5	0.17	−41	1.13
750	−10.6	0.29	−52	15.0	5.62	115	−21.6	0.08	−13	−14.6	0.19	−44	1.13
800	−10.6	0.30	−55	14.8	5.51	111	−21.6	0.08	−14	−13.8	0.20	−45	1.12
850	−10.4	0.30	−58	14.6	5.39	107	−21.6	0.08	−15	−13.1	0.22	−47	1.12
900	−10.3	0.30	−61	14.4	5.28	104	−21.6	0.08	−16	−12.4	0.24	−49	1.12
950	−10.2	0.31	−64	14.3	5.17	100	−21.6	0.08	−17	−11.7	0.26	−51	1.12
1000	−10.1	0.31	−66	14.1	5.06	96	−21.6	0.08	−18	−11.2	0.28	−52	1.11

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VPOS	6 V
Input Power (re: 50 Ω)	10 dBm
Internal Power Dissipation (Paddle Soldered)	600 mW
θ_{JC} (Junction to Paddle)	154 °C/W
Maximum Junction Temperature	180 °C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulates on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

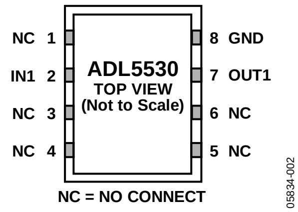

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 5, 6	NC	No Connect.
2	IN1	RF Input. Requires a DC blocking capacitor.
7	OUT1/ VPOS	RF Output and VPOS (Supply Voltage). DC bias is provided to this pin through an inductor. RF path requires a DC blocking capacitor.
8	GND	Ground. Connect this pin to a low impedance ground plane.
Exposed Paddle		Internally connected to GND. Solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

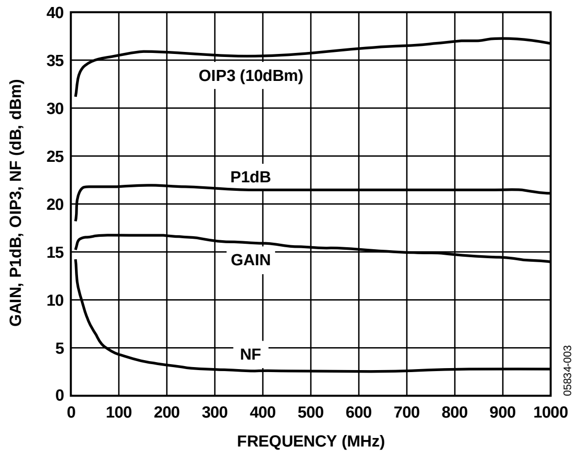

Figure 3. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, VPOS = 5 V

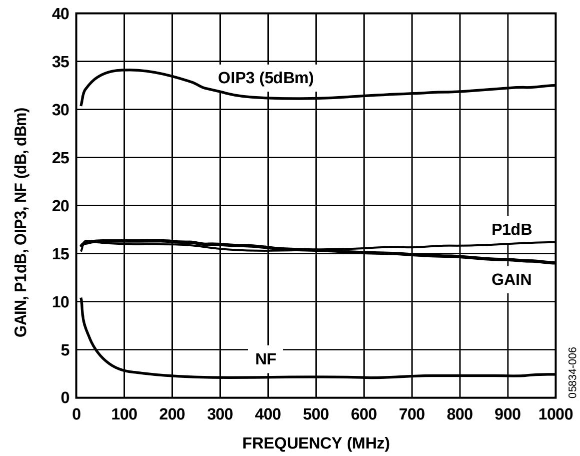

Figure 6. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, VPOS = 3 V

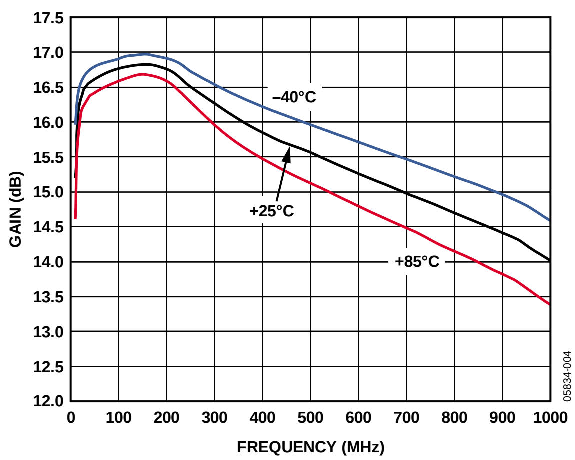

Figure 4. Gain vs. Frequency and Temperature, VPOS = 5 V

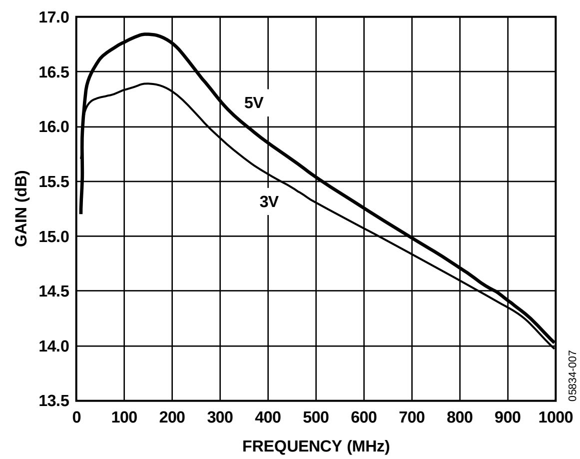

Figure 7. Gain vs. Frequency and Supply, VPOS = 5 V and 3 V

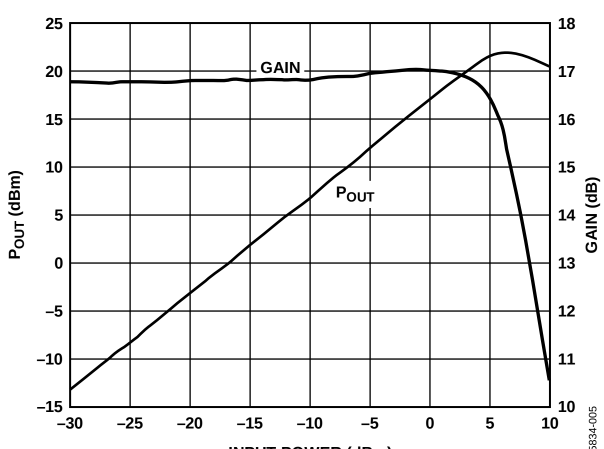

Figure 5. Output Power and Gain vs. Input Power, f = 190 MHz, VPOS = 5 V

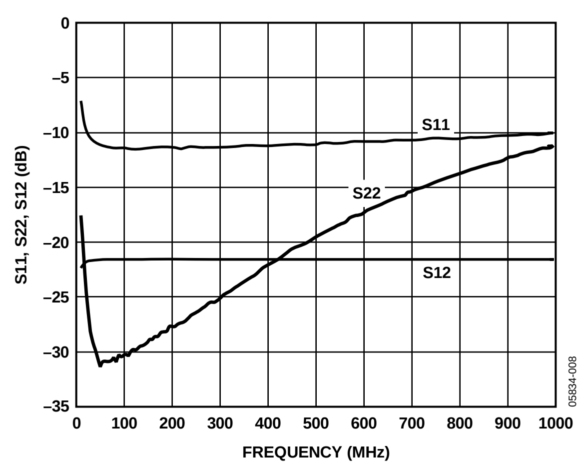

Figure 8. Input Return Loss, Output Return Loss, and Reverse Isolation vs. Frequency, VPOS = 5 V

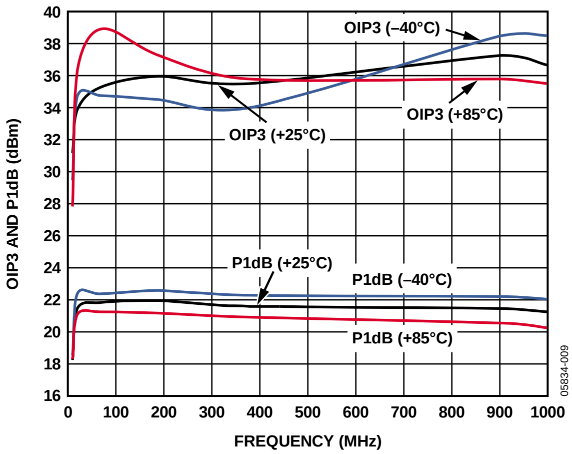

Figure 9. OIP3 and P1dB vs. Frequency and Temperature, VPOS = 5 V

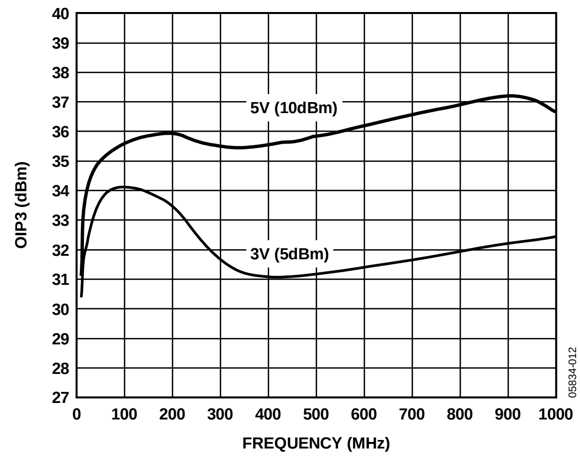

Figure 12. OIP3 vs. Frequency and Supply, VPOS = 5 V and 3 V

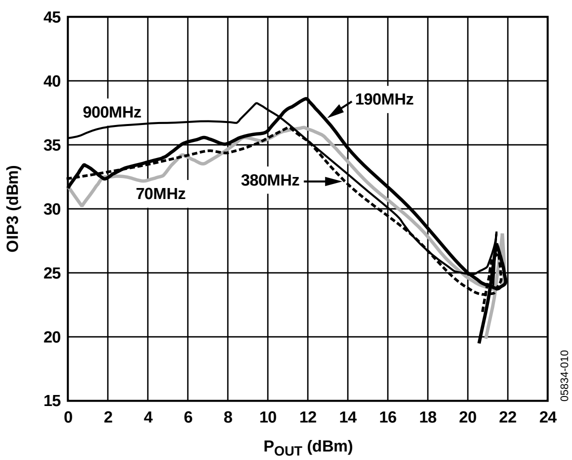

Figure 10. OIP3 vs. Output Power and Frequency, VPOS = 5 V

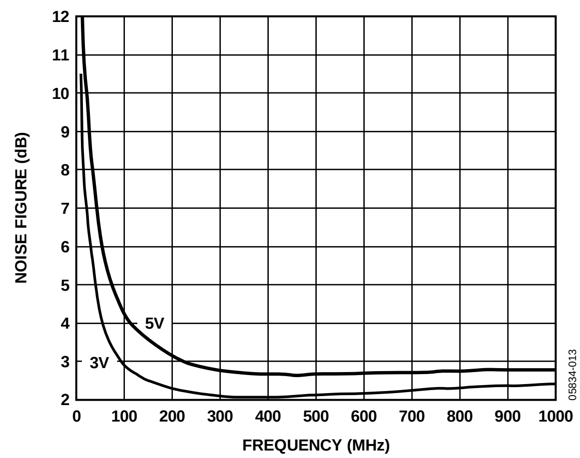

Figure 13. Noise Figure vs. Frequency and Supply, VPOS = 5 V and 3 V

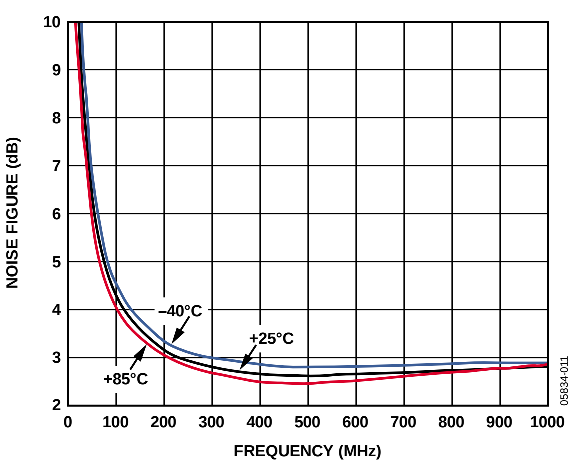

Figure 11. Noise Figure vs. Frequency and Temperature, VPOS = 5 V

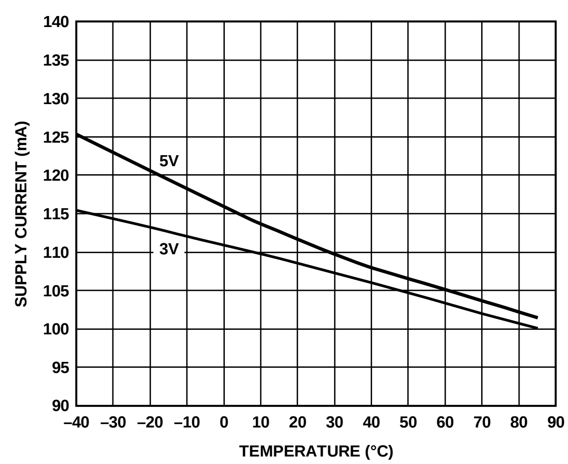

Figure 14. Supply Current vs. Temperature and Supply, VPOS = 5 V and 3 V

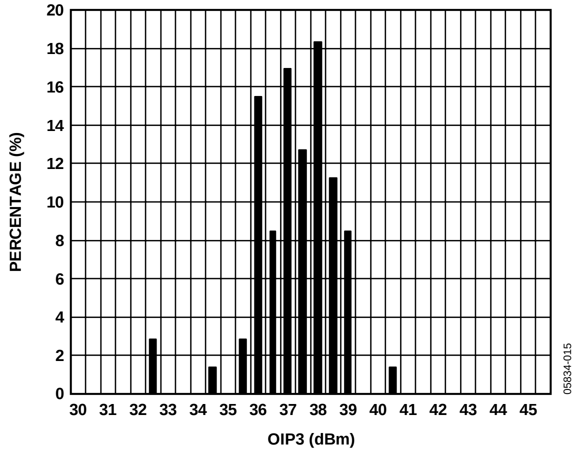

Figure 15. OIP3 Distribution at 190 MHz, 5 V

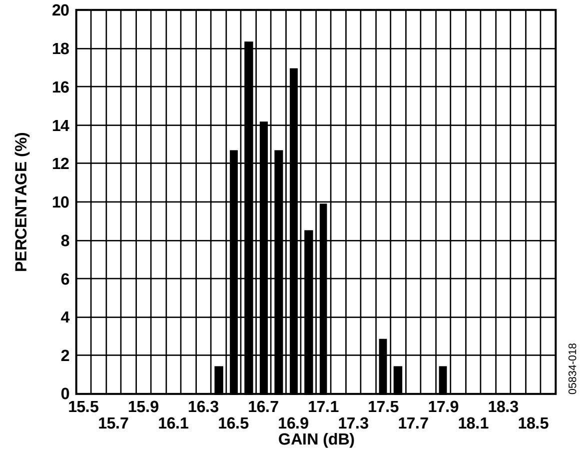

Figure 18. Gain Distribution at 190 MHz, VPOS = 5 V

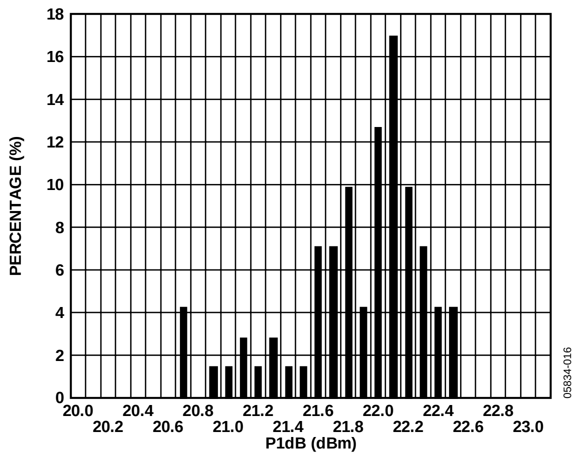

Figure 16. P1dB Distribution at 190 MHz, VPOS = 5 V

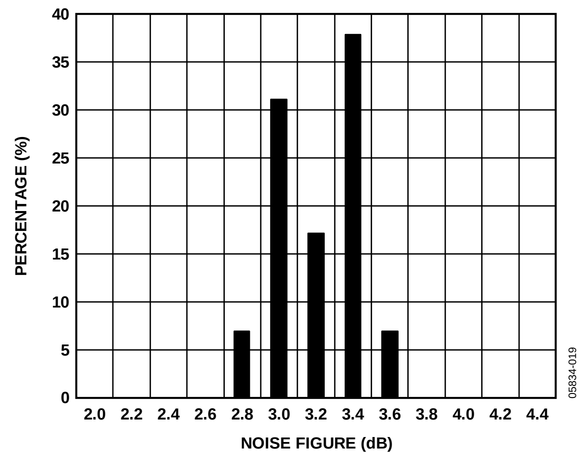

Figure 19. Noise Figure Distribution at 190 MHz, VPOS = 5 V

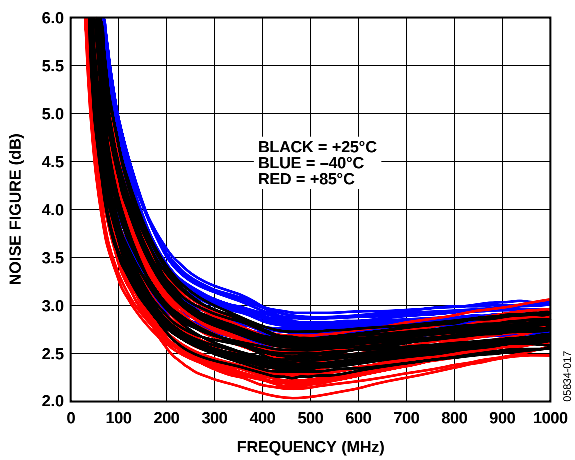

Figure 17. Noise Figure Temperature Distribution, VPOS = 5 V

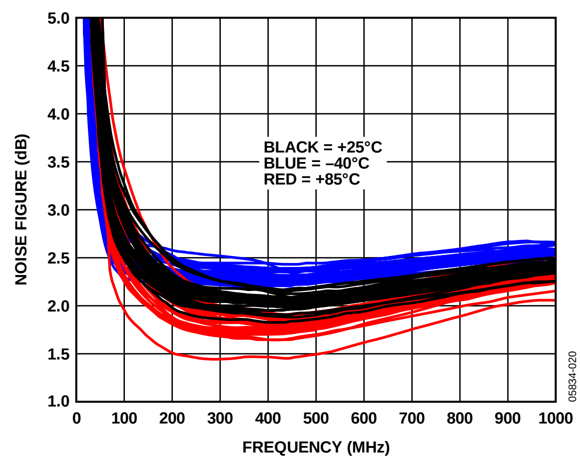

Figure 20. Noise Figure Temperature Distribution, VPOS = 3 V

THEORY OF OPERATION

The basic connections for operating the ADL5530 are shown in Figure 21. Recommended components are listed in Table 5. The inputs and outputs should be ac coupled with appropriately sized capacitors (device characterization was performed with 10 nF capacitors). DC bias is provided to the amplifier via an inductor connected to the RF output pin. The bias voltage should be decoupled using a 10 nF capacitor.

A bias voltage of 5 V is recommended. However, the device is specified to operate down to 3 V with a slightly reduced compression point and a reduced noise figure.

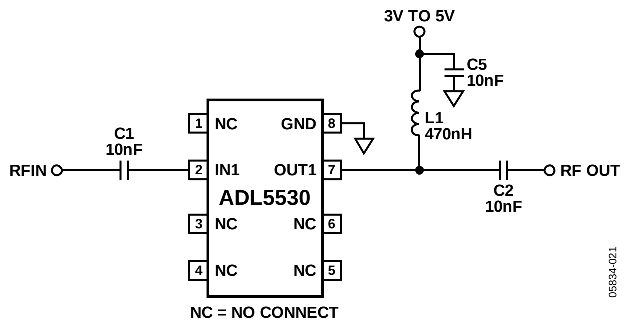

Figure 21. Basic Connections

For operation down to 10 MHz, a larger biasing choke is recommended (see Table 5) along with larger ac-coupling capacitors. Figure 22 shows a plot of input return loss and gain with the recommended components.

Table 5. Recommended Components for Basic Connections

Frequency	C1	C2	L1	C5
10 MHz to 50 MHz	0.1 µF	0.1 µF	3.3 µH	0.1 µF
50 MHz to 1000 MHz	10 nF	10 nF	470 nH	10 nF

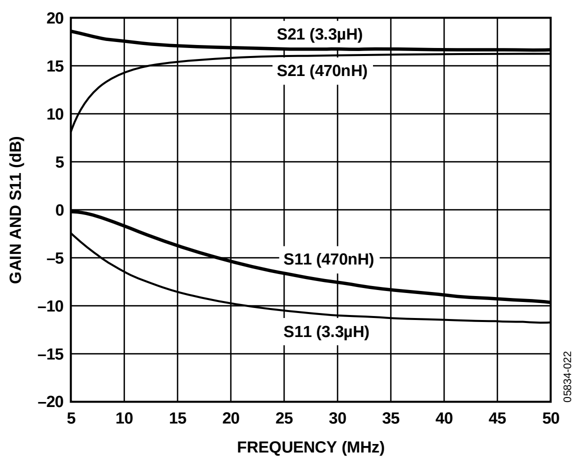

Figure 22. Performance at 10 MHz

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 23 shows the recommended land pattern for ADL5530. To minimize thermal impedance, the exposed paddle on the package underside should be soldered down to a ground plane along with Pin 8. If multiple ground layers exist, they should be stitched together using vias. Pin 1, Pin 3, Pin 4, Pin 5 and Pin 6 can be left unconnected, or can be connected to ground. Connecting these pins to ground slightly enhances thermal impedance.

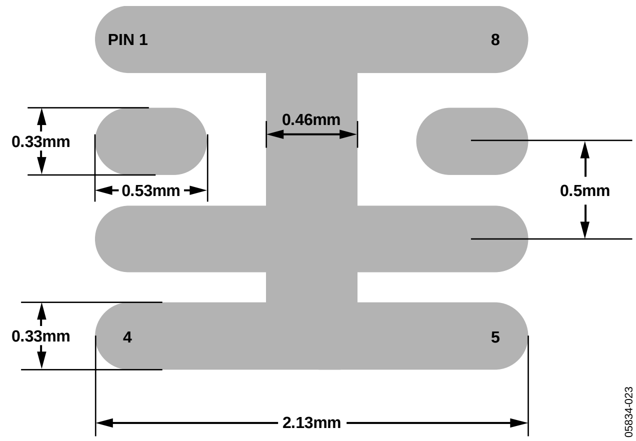

Figure 23. Recommended Land Pattern

EVALUATION BOARD

Figure 24 shows the schematic for the ADL5530 evaluation board. The board is powered by a single supply (between 3 V and 5 V).

The components used on the board are listed in Table 6. Power can be applied to the board through clip-on leads (J5, J6), through an edge connector (P1), or through Jumper W1. Note that IN2, OUT2, T1, T2, C6, C7 and C10 have no function. Because Pin 1, Pin 3 and Pin 6 of ADL5530 are No Connects, these pins are grounded on this PCB (this has no effect on electrical performance).

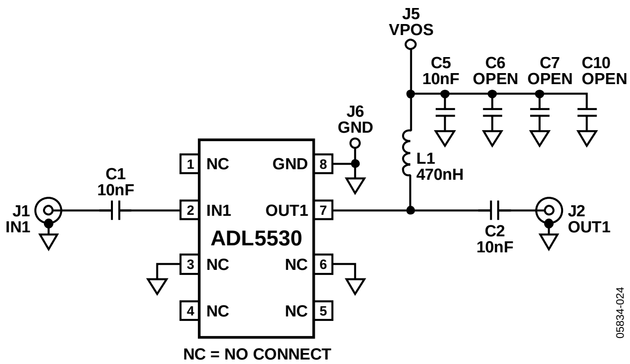

Figure 24. Evaluation Board Schematic

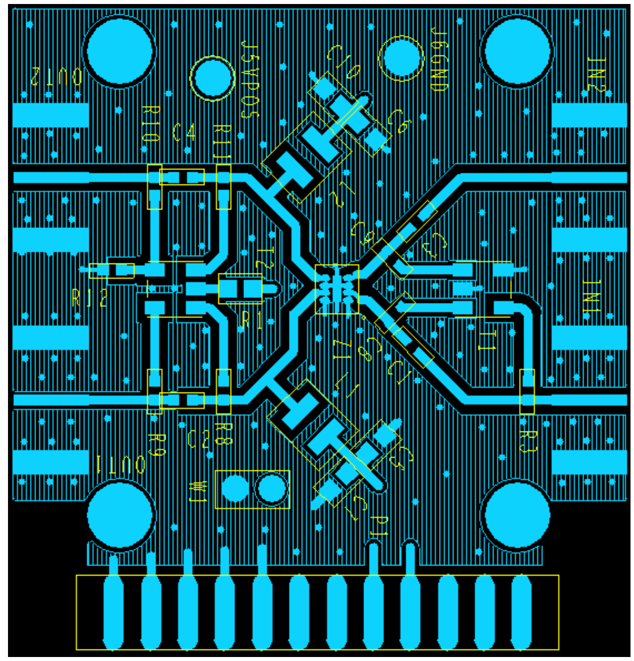

Figure 25. Evaluation Board Layout

Table 6. Evaluation Board Configuration Options

Component	Function	Default Value
C1, C2	AC-coupling capacitors.	10 nF 0402
C5	Power supply decoupling capacitor.	10 nF 0603
L1	DC bias inductor.	470 nH 1008
J5, J6	Clip-on terminals for power supply.	J5 = VPOS J6 = GND
W1	2-pin jumper for connection of ground and supply via cable.	
P1	Edge connector.	P1: A1 to A5 = GND P1: B1 to B5 = GND P1: A8 to A9 = VPOS P1: B8 to B9 = VPOS

OUTLINE DIMENSIONS

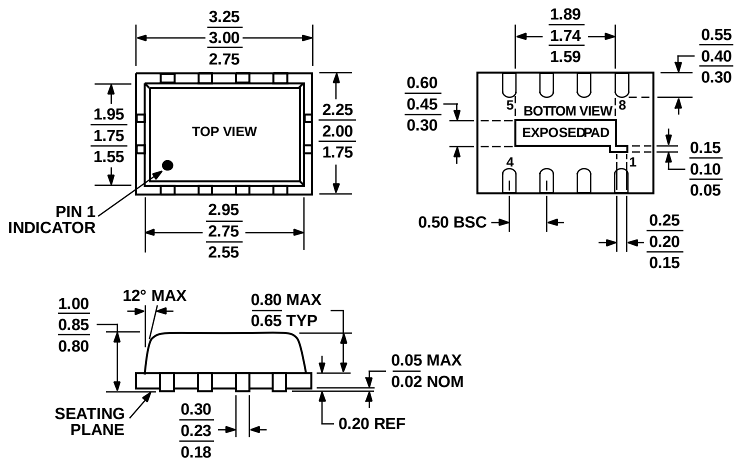

Figure 26. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
2 mm × 3 mm Body, Very Thin, Dual Lead
CP-8-1
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5530ACPZ-R7[1]	−40°C to +85°C	8-Lead LFCSP_VD, 7" Tape and Reel	CP-8-1	OT	1500
ADL5530ACPZ-WP[1]	−40°C to +85°C	8-Lead LFCSP_VD, Waffle Pack	CP-8-1	OT	50
ADL5530-EVAL		Evaluation Board			1

[1] Z = Pb-free part.