



# 4 ADC/8 DAC with PLL, 192 kHz, 24-Bit CODEC

## AD1939

### FEATURES

- PLL generated or direct master clock
- Low EMI design
- 112 dB DAC/107 dB ADC dynamic range and SNR
- 94 dB THD + N
- Single 3.3 V supply
- Tolerance for 5 V logic inputs
- Supports 24-bits and 8 kHz to 192 kHz sample rates
- Differential ADC input
- Differential DAC output
- Log volume control with autoramp function
- SPI® controllable for flexibility
- Software controllable clickless mute
- Software power-down
- Right-justified, left-justified, I<sup>2</sup>S, and TDM modes
- Master and slave modes up to 16-channel in/out
- 64-lead LQFP package

### APPLICATIONS

- Automotive audio systems
- Home Theater Systems
- Set-top boxes
- Digital audio effects processors

### GENERAL DESCRIPTION

The AD1939 is a high performance, single-chip codec that provides four analog-to-digital converters (ADCs) with differential input and eight digital-to-analog converters (DACs) with differential output using the Analog Devices, Inc. patented multibit sigma-delta ( $\Sigma$ - $\Delta$ ) architecture. An SPI port is included, allowing a microcontroller to adjust volume and many other parameters. The AD1939 operates from 3.3 V digital and analog supplies. The AD1939 is available in a 64-lead (differential output) LQFP package.

The AD1939 is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive the master clock from the LR clock or from an external crystal, the AD1939 eliminates the need for a separate high frequency master clock and can also be used with a suppressed bit clock. The digital-to-analog and analog-to-digital converters are designed using the latest ADI continuous time architectures to further minimize EMI. By using 3.3 V supplies, power consumption is minimized, further reducing emissions.

### FUNCTIONAL BLOCK DIAGRAM

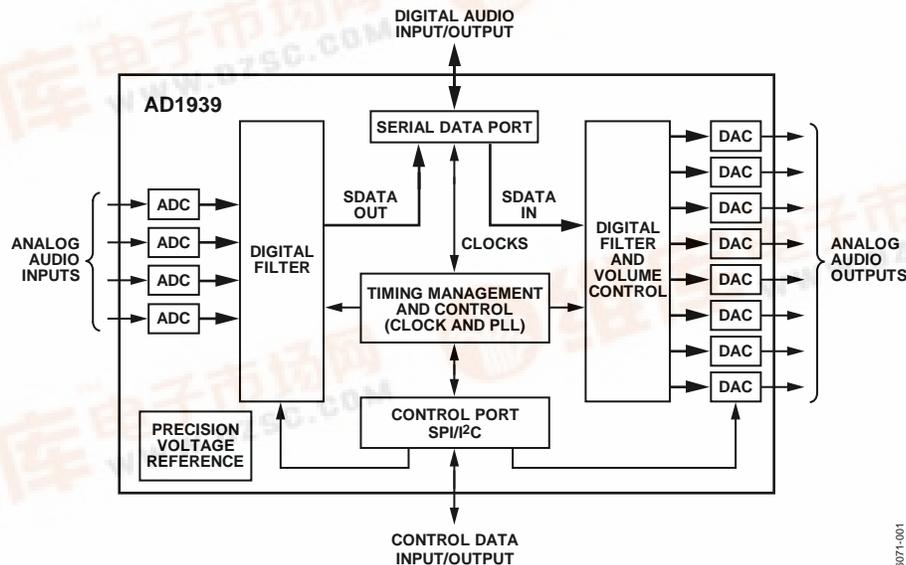


Figure 1.

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**REVISION HISTORY****7/06—Revision 0: Initial Version**

## SPECIFICATIONS

### TEST CONDITIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications.

Supply voltages (AVDD, DVDD)	3.3 V
Temperature range <sup>1</sup>	as specified in Table 1 and Table 2
Master clock	12.288 MHz (48 kHz $f_s$ , $256 \times f_s$ mode)
Input sample rate	48 kHz
Measurement bandwidth	20 Hz to 20 kHz
Word width	24 bits
Load capacitance (digital output)	20 pF
Load current (digital output)	$\pm 1$ mA or $1.5$ k $\Omega$ to $\frac{1}{2}$ DVDD supply
Input voltage HI	2.0 V
Input voltage LO	0.8 V

<sup>1</sup> Functionally guaranteed at  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  case temperature.

### ANALOG PERFORMANCE SPECIFICATIONS

Specifications guaranteed at  $25^\circ\text{C}$  (ambient).

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
<b>ANALOG-TO-DIGITAL CONVERTERS</b>					
ADC Resolution	All ADCs		24		Bits
Dynamic Range	20 Hz to 20 kHz, $-60$ dB input				
No Filter (RMS)		96	102		dB
With A-Weighted Filter (RMS)		98	105		dB
Total Harmonic Distortion + Noise	$-1$ dBFS		$-96$	$-87$	dB
Gain Error		$-10$		$+10$	%
Interchannel Gain Mismatch		$-0.25$		$+0.25$	dB
Offset Error		$-10$	0	$+10$	mV
Gain Drift			100		ppm/ $^\circ\text{C}$
Interchannel Isolation			$-110$		dB
CMRR	100 mV rms, 1 kHz		55		dB
	100 mV rms, 20 kHz		55		dB
Input Resistance			14		k $\Omega$
Input Capacitance			10		pF
Input Common-Mode Bias Voltage			1.5		V
<b>DIGITAL-TO-ANALOG CONVERTERS</b>					
Dynamic Range	20 Hz to 20 kHz, $-60$ dB input				
No Filter (RMS)		102	107		dB
With A-Weighted Filter (RMS)		105	110		dB
With A-Weighted Filter (Avg)			112		dB
Total Harmonic Distortion + Noise	0 dBFS				
	Two channels running		$-94$		dB
	Eight channels running		$-86$	$-76$	dB
Full-Scale Output Voltage			1.76 (4.96)		V rms (V p-p)
Gain Error		$-10$		$+10$	%
Interchannel Gain Mismatch		$-0.2$		$+0.2$	dB
Offset Error		$-25$	$-6$	$+25$	mV
Gain Drift		$-30$		$+30$	ppm/ $^\circ\text{C}$
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees

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Parameter	Conditions/Comments	Min	Typ	Max	Unit
Volume Control Step			0.375		dB
Volume Control Range			95		dB
De-emphasis Gain Error				±0.6	dB
Output Resistance at Each Pin			100		Ω
REFERENCE					
Internal Reference Voltage	FILTR pin		1.50		V
External Reference Voltage	FILTR pin	1.32	1.50	1.68	V
Common-Mode Reference Output	CM pin		1.50		V
REGULATOR					
Input Supply Voltage	VSUPPLY pin	4.5	5	5.5	V
Regulated Output Voltage	VSENSE pin	3.19	3.37	3.55	V

Specifications measured at 130°C (case).

**Table 2.**

Parameter	Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS					
ADC Resolution	All ADCs		24		Bits
Dynamic Range	20 Hz to 20 kHz, –60 dB input				
No Filter (RMS)		93	102		dB
With A-Weighted Filter (RMS)		96	104		dB
Total Harmonic Distortion + Noise	–1 dBFS		–96	–87	dB
Gain Error		–10		+10	%
Interchannel Gain Mismatch		–0.25		+0.25	dB
Offset Error		–10	0	+10	mV
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range	20 Hz to 20 kHz, –60 dB input				
No Filter (RMS)		101	107		dB
With A-Weighted Filter (RMS)		104	110		dB
With A-Weighted Filter (Average)			112		dB
Total Harmonic Distortion + Noise	0 dBFS				
	Two channels running		–94		dB
	Eight channels running		–86	–70	dB
Full-Scale Output Voltage			1.76 (4.96)		V rms (V p-p)
Gain Error		–10		+10	%
Interchannel Gain Mismatch		–0.2		+0.2	dB
Offset Error		–25	–6	+25	mV
Gain Drift		–30		+30	ppm/°C
REFERENCE					
Internal Reference Voltage	FILTR pin		1.50		V
External Reference Voltage	FILTR pin	1.32	1.50	1.68	V
Common-Mode Reference Output	CM pin		1.50		V
REGULATOR					
Input Supply Voltage	VSUPPLY pin	4.5	5	5.5	V
Regulated Output Voltage	VSENSE pin	3.2	3.43	3.65	V

## CRYSTAL OSCILLATOR SPECIFICATIONS

**Table 3.**

Parameter	Min	Typ	Max	Unit
Transconductance		3.5		mmhos

**DIGITAL INPUT/OUTPUT SPECIFICATIONS**

$-40^{\circ}\text{C} < T_A < +130^{\circ}\text{C}$ , DVDD = 3.3 V  $\pm$  10%.

**Table 4.**

Parameter	Conditions/Comments	Min	Typ	Max	Unit
Input Voltage HI ( $V_{IH}$ )		2.0			V
Input Voltage HI ( $V_{IH}$ )	MCLKI/XI pin	2.2			V
Input Voltage LO ( $V_{IL}$ )				0.8	V
Input Leakage	$I_{IH}$ @ $V_{IH} = 2.4$ V			10	$\mu\text{A}$
	$I_{IL}$ @ $V_{IL} = 0.8$ V			10	$\mu\text{A}$
High Level Output Voltage ( $V_{OH}$ )	$I_{OH} = 1$ mA	DVDD – 0.60			V
Low Level Output Voltage ( $V_{OL}$ )	$I_{OL} = 1$ mA			0.4	V
Input Capacitance				5	pF

**POWER SUPPLY SPECIFICATIONS****Table 5.**

Parameter	Conditions/Comments	Min	Typ	Max	Unit
<b>SUPPLIES</b>					
Voltage	DVDD	3.0	3.3	3.6	V
	AVDD	3.0	3.3	3.6	V
Digital Current	MCLK = 256 $f_s$				
Normal Operation	$f_s = 48$ kHz		56		mA
	$f_s = 96$ kHz		65		mA
	$f_s = 192$ kHz		95		mA
Power-Down	$f_s = 48$ kHz to 192 kHz		2.0		mA
Analog Current					
Normal Operation			74		mA
Power-Down			23		mA
<b>DISSIPATION</b>					
Operation	MCLK = 256 $f_s$ , 48 kHz				
All Supplies			429		mW
Digital Supply			185		mW
Analog Supply			244		mW
Power-Down, All Supplies			83		mW
<b>POWER SUPPLY REJECTION RATIO</b>					
Signal at Analog Supply Pins	1 kHz 200 mV p-p		50		dB
	20 kHz 200 mV p-p		50		dB

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## DIGITAL FILTERS

Table 6.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typ @ 48 kHz					
Pass Band		0.4375 $f_s$		21		kHz
Pass-Band Ripple				$\pm 0.015$		dB
Transition Band		0.5 $f_s$		24		kHz
Stop Band		0.5625 $f_s$		27		kHz
Stop-Band Attenuation			79			dB
Group Delay		22.9844/ $f_s$		479		$\mu$ s
DAC INTERPOLATION FILTER						
Pass Band	48 kHz mode, typ @ 48 kHz	0.4535 $f_s$		22		kHz
	96 kHz mode, typ @ 96 kHz	0.3646 $f_s$	35			kHz
	192 kHz mode, typ @ 192 kHz	0.3646 $f_s$		70		kHz
Pass-Band Ripple	48 kHz mode, typ @ 48 kHz				$\pm 0.01$	dB
	96 kHz mode, typ @ 96 kHz				$\pm 0.05$	dB
	192 kHz mode, typ @ 192 kHz				$\pm 0.1$	dB
Transition Band	48 kHz mode, typ @ 48 kHz	0.5 $f_s$		24		kHz
	96 kHz mode, typ @ 96 kHz	0.5 $f_s$		48		kHz
	192 kHz mode, typ @ 192 kHz	0.5 $f_s$		96		kHz
Stop Band	48 kHz mode, typ @ 48 kHz	0.5465 $f_s$		26		kHz
	96 kHz mode, typ @ 96 kHz	0.6354 $f_s$		61		kHz
	192 kHz mode, typ @ 192 kHz	0.6354 $f_s$		122		kHz
Stop-Band Attenuation	48 kHz mode, typ @ 48 kHz		70			dB
	96 kHz mode, typ @ 96 kHz		70			dB
	192 kHz mode, typ @ 192 kHz		70			dB
Group Delay	48 kHz mode, typ @ 48 kHz	25/ $f_s$		521		$\mu$ s
	96 kHz mode, typ @ 96 kHz	11/ $f_s$		115		$\mu$ s
	192 kHz mode, typ @ 192 kHz	8/ $f_s$		42		$\mu$ s

## TIMING SPECIFICATIONS

$-40^{\circ}\text{C} < T_A < +130^{\circ}\text{C}$ , DVDD = 3.3 V  $\pm$  10%.

Table 7.

Parameter	Condition	Comments	Min	Max	Unit
INPUT MASTER CLOCK (MCLK) AND RESET					
$t_{MH}$	MCLK duty cycle	DAC/ADC clock source = PLL clock @ 256 $f_s$ , 384 $f_s$ , 512 $f_s$ , 768 $f_s$	40	60	%
$t_{MH}$		DAC/ADC clock source = direct MCLK @ 512 $f_s$ (bypass on-chip PLL)	40	60	%
$f_{MCLK}$	MCLK frequency	PLL mode, 256 $f_s$ reference	6.9	13.8	MHz
$f_{MCLK}$		Direct 512 $f_s$ mode		27.6	MHz
$t_{PDR}$	Low		15		ns
$t_{PDRR}$	Recovery	Reset to active output	4096		$t_{MCLK}$
PLL					
Lock time	MCLK and LRCLK input			10	ms
256 $f_s$ VCO Clock Output Duty Cycle MCLKO/XO pin			40	60	%

Parameter	Condition	Comments	Min	Max	Unit
<b>SPI PORT</b>					
		See Figure 11			
t <sub>CCH</sub>	CCLK high		35		ns
t <sub>CCL</sub>	CCLK low		35		ns
f <sub>CCLK</sub>	CCLK frequency	f <sub>CCLK</sub> = 1/t <sub>CCP</sub> ; only t <sub>CCP</sub> shown in Figure 11		10	MHz
t <sub>CDS</sub>	CDATA setup	To CCLK rising	10		ns
t <sub>CDH</sub>	CDATA hold	From CCLK rising	10		ns
t <sub>CLS</sub>	CLATCH setup	To CCLK rising	10		ns
t <sub>CLH</sub>	CLATCH hold	From CCLK falling	10		ns
t <sub>CLHIGH</sub>	CLATCH high	Not shown in Figure 11	10		ns
t <sub>COE</sub>	COOUT enable	From CCLK falling		30	ns
t <sub>COD</sub>	COOUT delay	From CCLK falling		30	ns
t <sub>COH</sub>	COOUT hold	From CCLK falling, not shown in Figure 11	30		ns
t <sub>COTS</sub>	COOUT tri-state	From CCLK falling		30	ns
<b>DAC SERIAL PORT</b>					
		See Figure 24			
t <sub>DBH</sub>	DBCLK high	Slave mode	10		ns
t <sub>DBL</sub>	DBCLK low	Slave mode	10		ns
t <sub>DLS</sub>	DLRCLK setup	To DBCLK rising, slave mode	10		ns
t <sub>DLH</sub>	DLRCLK hold	From DBCLK rising, slave mode	5		ns
t <sub>DLS</sub>	DLRCLK skew	From DBCLK falling, master mode	-8	+8	ns
t <sub>DDS</sub>	DSDATA setup	To DBCLK rising	10		ns
t <sub>DDH</sub>	DSDATA hold	From DBCLK rising	5		ns
<b>ADC SERIAL PORT</b>					
		See Figure 25			
t <sub>ABH</sub>	ABCLK high	Slave mode	10		ns
t <sub>ABL</sub>	ABCLK low	Slave mode	10		ns
t <sub>ALS</sub>	ALRCLK setup	To ABCLK rising, slave mode	10		ns
t <sub>ALH</sub>	ALRCLK hold	From ABCLK rising, slave mode	5		ns
t <sub>ALS</sub>	ALRCLK skew	From ABCLK falling, master mode	-8	+8	ns
t <sub>ABDD</sub>	ASDATA delay	From ABCLK falling		18	ns
<b>AUXILIARY INTERFACE</b>					
t <sub>AXDS</sub>	AAUXDATA setup	To AUXBCLK rising	10		ns
t <sub>AXDH</sub>	AAUXDATA hold	From AUXBCLK rising	5		ns
t <sub>DXDD</sub>	DAUXDATA delay	From AUXBCLK falling		18	ns
t <sub>XBH</sub>	AUXBCLK high		10		ns
t <sub>XBL</sub>	AUXBCLK low		10		ns
t <sub>DLS</sub>	AUXLRCLK setup	To AUXBCLK rising	10		ns
t <sub>DLH</sub>	AUXLRCLK hold	From AUXBCLK rising	5		ns

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## ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Analog (AVDD)	-0.3 V to +3.6 V
Digital (DVDD)	-0.3 V to +3.6 V
VSUPPLY	-0.3 V to +6.0 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	-0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	-0.3 V to DVDD + 0.3 V
Operating Temperature Range (Case)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## THERMAL RESISTANCE

$\theta_{JA}$  represents thermal resistance, junction-to-ambient;

$\theta_{JC}$  represents the thermal resistance, junction-to-case.

All characteristics are for a 4-layer board.

Table 9. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
64-lead LQFP	47	11.1	°C/W



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

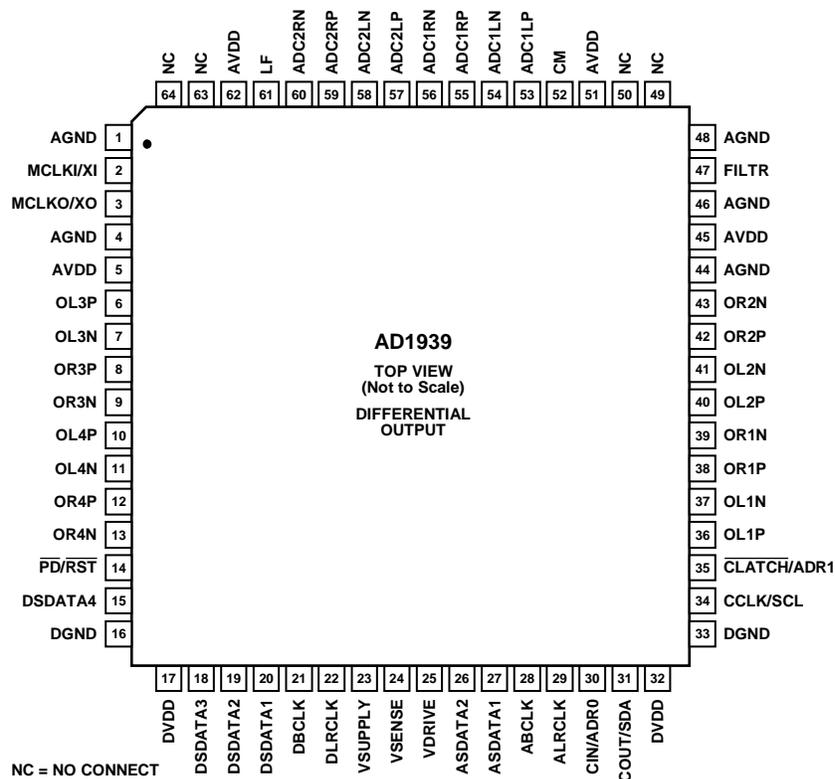


Figure 2. 64-Lead LQFP, Differential Output, Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	In/Out	Mnemonic	Description
1	I	AGND	Analog Ground.
2	I	MCLKI/XI	Master Clock Input/Crystal Oscillator Input.
3	O	MCLKO/XO	Master Clock Output/Crystal Oscillator Output.
4	I	AGND	Analog Ground.
5	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
6	O	OL3P	DAC 3 Left Positive Output.
7	O	OL3N	DAC 3 Left Negative Output.
8	O	OR3P	DAC 3 Right Positive Output.
9	O	OR3N	DAC 3 Right Negative Output.
10	O	OL4P	DAC 4 Left Positive Output.
11	O	OL4N	DAC 4 Left Negative Output.
12	O	OR4P	DAC 4 Right Positive Output.
13	O	OR4N	DAC 4 Right Negative Output
14	I	PD/RST	Power-Down Reset (Active Low).
15	I/O	DSDATA4	DAC Input 4 (Input to DAC 4 L and R)/DAC TDM Data Out 2/AUX ADC 1 Data In.
16	I	DGND	Digital Ground.
17	I	DVDD	Digital Power Supply. Connect to digital 3.3 V supply.
18	I/O	DSDATA3	DAC Input 3 (Input to DAC 3 L and R)/DAC TDM Data In 2/Aux DAC 2 Data Output.
19	I/O	DSDATA2	DAC Input 2 (Input to DAC 2 L and R)/DAC TDM Data Out 1/AUX ADC 1 Data In.
20	I	DSDATA1	DAC Input 1 (Input to DAC 1 L and R)/DAC TDM Data In 1/AUX ADC 2 Data In.
21	I/O	DBCLK	Bit Clock for DACs.
22	I/O	DLRCLK	LR Clock for DACs.
23	I	VSUPPLY	+5 V Input to Regulator, Emitter of Pass Transistor.
24	I	VSENSE	+3.3 V Output of Regulator, Collector of Pass Transistor.

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Pin No.	In/Out	Mnemonic	Description
25	O	VDRIVE	Drive for Base of Pass Transistor.
26	I/O	ASDATA2	ADC Serial Data Output 2 (ADC 2 L and R)/ADC TDM Data Input/Aux DAC 1 Data Output.
27	O	ASDATA1	ADC Serial Data Output 1 (ADC 1 L and R)/ADC TDM Data Output.
28	I/O	ABCLK	Bit Clock for ADCs.
29	I/O	ALRCLK	LR Clock for ADCs.
30	I	CIN/ADR0	Control Data Input (SPI).
31	I/O	COUT/SDA	Control Data Output (SPI).
32	I	DVDD	Digital Power Supply. Connect to digital 3.3 V supply.
33	I	DGND	Digital Ground.
34	I	CCLK/SCL	Control Clock Input (SPI).
35	I	CLATCH/ADR1	Latch Input for Control Data (SPI).
36	O	OL1P	DAC 1 Left Positive Output.
37	O	OL1N	DAC 1 Left Negative Output.
38	O	OR1P	DAC 1 Right Positive Output.
39	O	OR1N	DAC 1 Right Negative Output.
40	O	OL2P	DAC 2 Left Positive Output.
41	O	OL2N	DAC 2 Left Negative Output.
42	O	OR2P	DAC 2 Right Positive Output.
43	O	OR2N	DAC 2 Right Negative Output
44	I	AGND	Analog Ground.
45	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
46	I	AGND	Analog Ground.
47	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass with 10 $\mu$ F  100 nF to AGND.
48	I	AGND	Analog Ground.
49		NC	No Connect.
50		NC	No Connect.
51	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
52	O	CM	Common-Mode Reference Filter Capacitor Connection. Bypass with 47 $\mu$ F  100 nF to AGND.
53	I	ADC1LP	ADC1 Left Positive Input.
54	I	ADC1LN	ADC1 Left Negative Input.
55	I	ADC1RP	ADC1 Right Positive Input.
56	I	ADC1RN	ADC1 Right Negative Input.
57	I	ADC2LP	ADC2 Left Positive Input.
58	I	ADC2LN	ADC2 Left Negative Input.
59	I	ADC2RP	ADC2 Right Positive Input.
60	I	ADC2RN	ADC2 Right Negative Input.
61	O	LF	PLL Loop Filter, Return to AVDD.
62	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
63		NC	No Connect.
64		NC	No Connect.

# TYPICAL PERFORMANCE CHARACTERISTICS

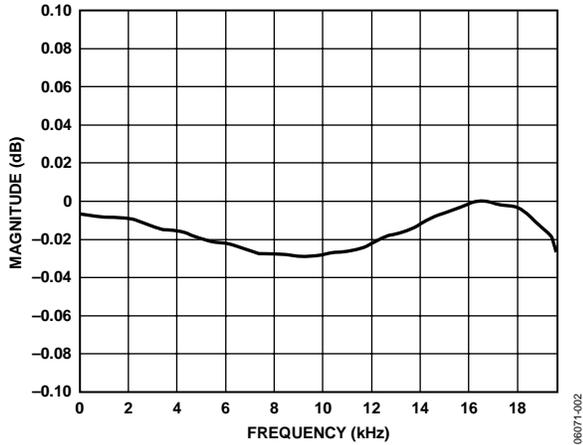


Figure 3. ADC Pass-Band Filter Response, 48 kHz

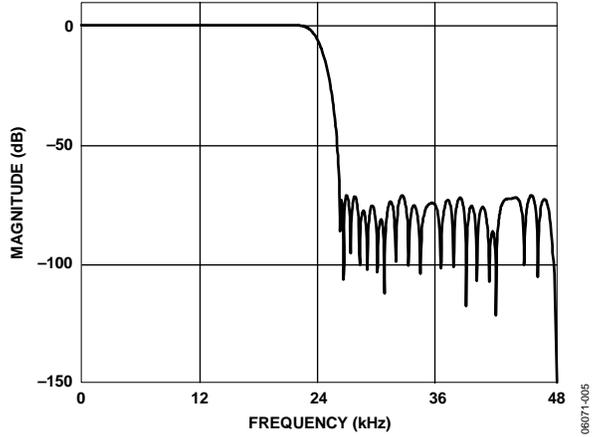


Figure 6. DAC Stop-Band Filter Response, 48 kHz

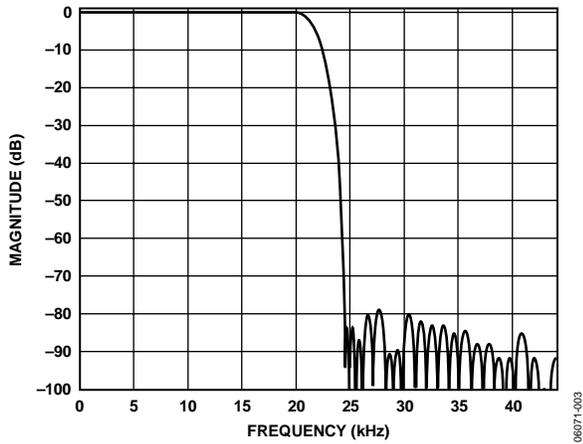


Figure 4. ADC Stop-Band Filter Response, 48 kHz

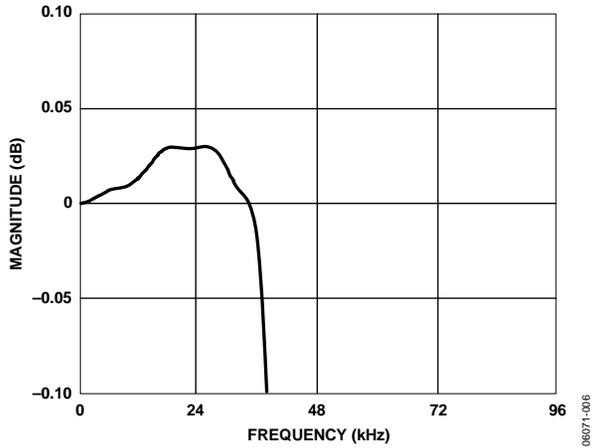


Figure 7. DAC Pass-Band Filter Response, 96 kHz

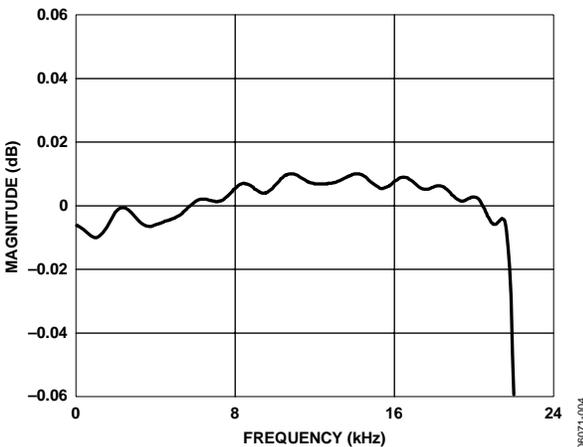


Figure 5. DAC Pass-Band Filter Response, 48 kHz

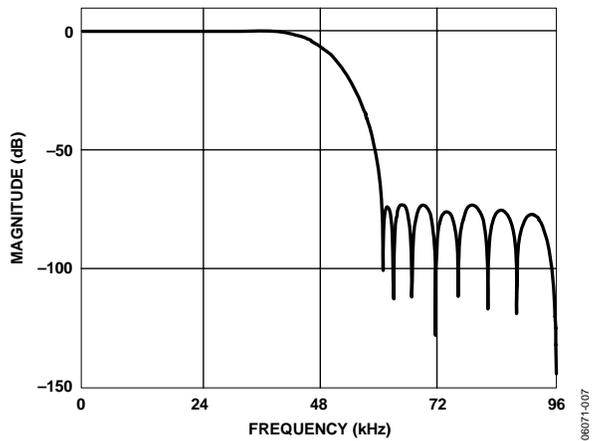


Figure 8. DAC Stop-Band Filter Response, 96 kHz

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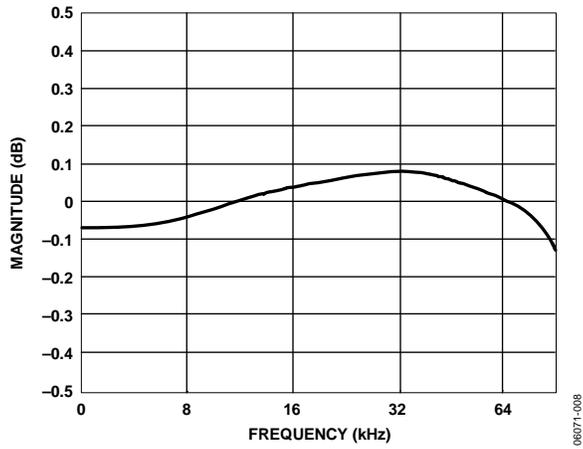


Figure 9. DAC Pass-Band Filter Response, 192 kHz

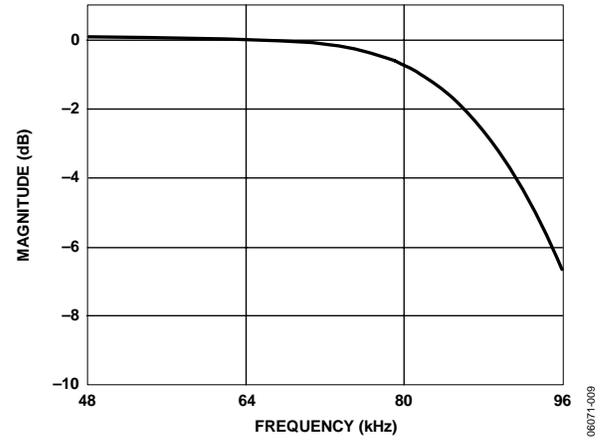


Figure 10. DAC Stop-Band Filter Response, 192 kHz

## THEORY OF OPERATION

### ANALOG-TO-DIGITAL CONVERTERS (ADCS)

There are four analog-to-digital converter (ADC) channels in the AD1939 configured as two stereo pairs with differential inputs. The ADCs can operate at a nominal sample rate of 48 kHz, 96 kHz, or 192 kHz. The ADCs include on-board digital anti-aliasing filters with 79 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 128 (48 kHz, 96 kHz, and 192 kHz modes). Digital outputs are supplied through two serial data output pins (one for each stereo pair) and a common frame clock (ALRCLK) and bit clock (ABCLK). Alternatively, one of the TDM modes can be used to access up to 16 channels on a single TDM data line.

The ADCs must be driven from a differential signal source for best performance. The input pins of the ADCs connect to internal switched capacitors. To isolate the external driving op amp from the glitches caused by the internal switched capacitors, each input pin should be isolated by using a series-connected external 100  $\Omega$  resistor together with a 1 nF capacitor connected from each input to ground. This capacitor must be of high quality, for example, ceramic NPO or polypropylene film.

The differential inputs have a nominal common-mode voltage of 1.5 V. The voltage at the common-mode reference pin (CM) can be used to bias external op amps to buffer the input signals (see the Power Supply and Voltage Reference section). The inputs can also be ac-coupled and do not need an external dc bias to CM.

A digital high-pass filter can be switched in line with the ADCs under serial control to remove residual dc offsets. It has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency scales directly with sample frequency.

### DIGITAL-TO-ANALOG CONVERTERS (DACs)

The AD1939 digital-to-analog converter (DAC) channels are arranged as differential, four stereo pairs giving eight analog outputs for improved noise and distortion performance. The DACs include on-board digital reconstruction filters with 70 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 4 (48 kHz or 96 kHz modes) or 2 (192 kHz mode). Each channel has its own independently programmable attenuator, adjustable in 255 steps in increments of 0.375 dB. Digital inputs are supplied through four serial data input pins (one for each stereo pair) and a common frame clock (DLRCLK) and bit clock (DBCLK). Alternatively, one of the TDM modes can be used to access up to 16 channels on a single TDM data line.

Each output pin has a nominal common-mode dc level of 1.5 V and swings  $\pm 1.27$  V for a 0 dBFS digital input signal. A single op amp, third-order, external, low-pass filter is recommended to remove high frequency noise present on the output pins, as well as to provide differential-to-single-ended conversion in the case of the differential output. Note that the use of op amps with low

slew rate or low bandwidth can cause high frequency noise and tones to fold down into the audio band; exercise care in selecting these components.

The voltage at CM, the common-mode reference pin, can be used to bias the external op amps that buffer the output signals (see the Power Supply and Voltage Reference section).

### CLOCK SIGNALS

The on-chip phase locked loop (PLL) can be selected to reference the input sample rate from either of the LRCLK pins or 256, 384, 512, or 768 times the sample rate, referenced to the 48 kHz mode from the MCLKI/XI pin. The default at power-up is  $256 \times f_s$  from MCLKI/XI. In 96 kHz mode, the master clock frequency stays at the same absolute frequency; therefore, the actual multiplication rate is divided by 2. In 192 kHz mode, the actual multiplication rate is divided by 4. For example, if a device in the AD1939 family is programmed in  $256 \times f_s$  mode, the frequency of the master clock input is  $256 \times 48$  kHz = 12.288 MHz. If the AD1939 is then switched to 96 kHz operation (by writing to the SPI or I<sup>2</sup>C<sup>®</sup> port), the frequency of the master clock should remain at 12.288 MHz, which is  $128 \times f_s$  in this example. In 192 kHz mode, this becomes  $64 \times f_s$ .

The internal clock for the ADCs is  $256 \times f_s$  for all clock modes. The internal clock for the DACs varies by mode:  $512 \times f_s$  (48 kHz mode),  $256 \times f_s$  (96 kHz mode), or  $128 \times f_s$  (192 kHz mode). By default, the on-board PLL generates this internal master clock from an external clock. A direct  $512 \times f_s$  (referenced to 48 kHz mode) master clock can be used for either the ADCs or DACs if selected in PLL and Clock Control 1 register.

Note that it is not possible to use a direct clock for the ADCs set to the 192 kHz mode. It is required that the on-chip PLL be used in this mode.

The PLL can be powered down in the PLL and Clock Control 0 register. To ensure reliable locking when changing PLL modes, or if the reference clock is unstable at power-on, power down the PLL and then power it back up when the reference clock has stabilized.

The internal master clock (MCLK) can be disabled in the PLL and Clock Control 0 register to reduce power dissipation when the AD1939 is idle. The clock should be stable before it is enabled. Unless a standalone mode is selected (see the Serial Control Port section), the clock is disabled by reset and must be enabled by writing to the SPI or I<sup>2</sup>C port for normal operation.

To maintain the highest performance possible, it is recommended that the clock jitter of the internal master clock signal be limited to less than 300 ps rms TIE (time interval error). Even at these levels, extra noise or tones can appear in the DAC outputs if the jitter spectrum contains large spectral peaks. If the internal PLL is not being used, it is best to use an independent crystal oscillator

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to generate the master clock. In addition, it is especially important that the clock signal should not be passed through an FPGA, CPLD, or other large digital chip (such as a DSP) before being applied to the AD1939. In most cases, this induces clock jitter due to the sharing of common power and ground connections with other unrelated digital output signals. When the PLL is used, jitter in the reference clock is attenuated above a certain frequency depending on the loop filter.

## RESET AND POWER-DOWN

Reset sets all the control registers to their default settings. To avoid pops, reset does not power down the analog outputs. After reset is deasserted and the PLL acquires lock condition, an initialization routine runs inside the AD1939. This initialization lasts for approximately 256 MCLKs.

The power-down bits in the PLL and Clock Control 0, DAC Control 1, and ADC Control 1 registers power down the respective sections. All other register settings are retained. The reset pin should be pulled low by an external resistor to guarantee proper startup.

## SERIAL CONTROL PORT

The AD1939 has an SPI control port that permits programming and reading back of the internal control registers for the ADCs, DACs, and clock system. A standalone mode is also available for operation without serial control; it is configured at reset using the serial control pins. All registers are set to default, except the internal MCLK enable is set to 1 and ADC BCLK and LRCLK master/slave is set by the COUT/SDA pin. Standalone mode only supports stereo mode with an I<sup>2</sup>S data format and 256 f<sub>s</sub> MCLK rate. Refer to Table 11 for details. It is recommended to use a weak pull-up resistor on CLATCH in applications that have a microcontroller. This pull-up resistor ensures that the AD1939 recognizes the presence of a microcontroller.

The SPI control port of the AD1939 is a 4-wire serial control port. The format is similar to the Motorola SPI format except the input data-word is 24 bits wide. The serial bit clock and latch can be completely asynchronous to the sample rate of the ADCs and DACs. Figure 11 shows the format of the SPI signal. The first byte is a global address with a read/write bit. For the AD1939 the address is 0x04, shifted left one bit due to the R/W bit. The second byte is the AD1939 register address and the third byte is the data.

Table 11. Standalone Mode Selection

ADC Clocks	CIN/ADRO	COUT/SDA	CCLK/SCL	CLATCH/ADR1
Slave	0	0	0	0
Master	0	1	0	0

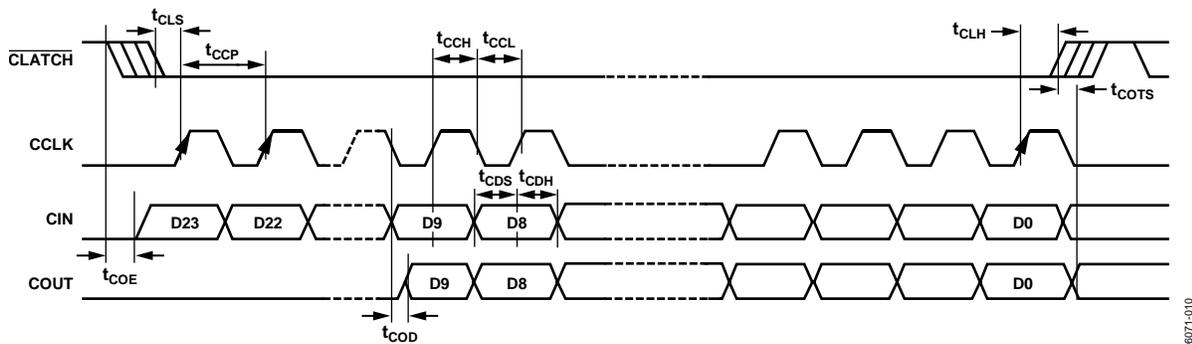


Figure 11. Format of SPI Signal

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## POWER SUPPLY AND VOLTAGE REFERENCE

The AD1939 is designed for 3.3 V supplies. Separate power supply pins are provided for the analog and digital sections. To minimize noise pickup, these pins should be bypassed with 100 nF ceramic chip capacitors placed as close to the pins as possible. A bulk aluminum electrolytic capacitor of at least 22  $\mu$ F should also be provided on the same PC board as the codec. For critical applications, improved performance is obtained with separate supplies for the analog and digital sections. If this is not possible, it is recommended that the analog and digital supplies be isolated by means of a ferrite bead in series with each supply. It is important that the analog supply be as clean as possible.

The AD1939 includes a 3.3 V regulator driver that only requires an external pass transistor and bypass capacitors to make a 5 V to 3.3 V regulator. If the regulator driver is not used, connect VSUPPLY, VDRIVE, and VSENSE to DGND.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the 3.3 V DVDD supply and are compatible with TTL and 3.3 V CMOS levels.

The ADC and DAC internal voltage reference ( $V_{REF}$ ) is brought out on FILTR and should be bypassed as close as possible to the chip with a parallel combination of 10  $\mu$ F and 100 nF. Any external current drawn should be limited to less than 50  $\mu$ A.

The internal reference can be disabled in the PLL and Clock Control 1 register and FILTR can be driven from an external source. This can be used to scale the DAC output to the clipping level of a power amplifier based on its power supply voltage. The ADC input gain varies by the inverse ratio. The total gain from ADC input to DAC output remains constant.

The CM pin is the internal common-mode reference. It should be bypassed as close as possible to the chip, with a parallel combination of 47  $\mu$ F and 100 nF. This voltage can be used to bias external op amps to the common-mode voltage of the input and output signal pins. The output current should be limited to less than 0.5 mA source and 2 mA sink.

## SERIAL DATA PORTS—DATA FORMAT

The eight DAC channels use a common serial bit clock (DBCLK) and a common left-right framing clock (DLRCLK) in the serial data port. The four ADC channels use a common serial bit clock (ABCLK) and left-right framing clock (ALRCLK) in the serial data port. The clock signals are all synchronous with the sample rate. The normal stereo serial modes are shown in Figure 23.

The ADC and DAC serial data modes default to I<sup>2</sup>S. The ports can also be programmed for left-justified, right-justified, and TDM modes. The word width is 24 bits by default and can be programmed for 16 or 20 bits. The DAC serial formats are programmable according to the DAC Control 0 register. The

polarity of DBCLK and DLRCLK is programmable according to the DAC Control 1 register. The ADC serial formats and serial clock polarity are programmable according to the ADC Control 1 register. Both DAC and ADC serial ports are programmable to become the bus masters according to DAC Control 1 register and ADC Control 2 register. By default, both ADC and DAC serial ports are in the slave mode.

## TIME-DIVISION MULTIPLEXED (TDM) MODES

The AD1939 serial ports also have several different TDM serial data modes. The first and most commonly used configurations are shown in Figure 12 and Figure 13. In Figure 12, the ADC serial port outputs one data stream consisting of four on-chip ADCs followed by four unused slots. In Figure 13, the eight on-chip DAC data slots are packed into one TDM stream. In this mode, both DBCLK and ABCLK are 256 fs.

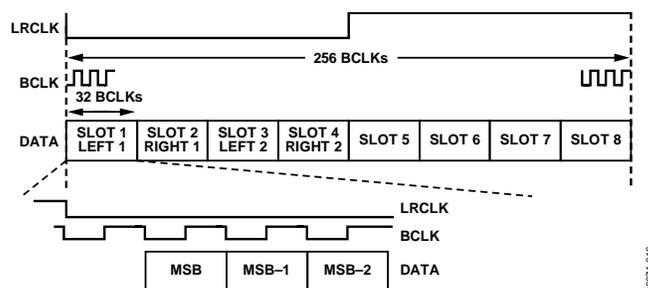


Figure 12. ADC TDM (8-Channel I<sup>2</sup>S Mode)

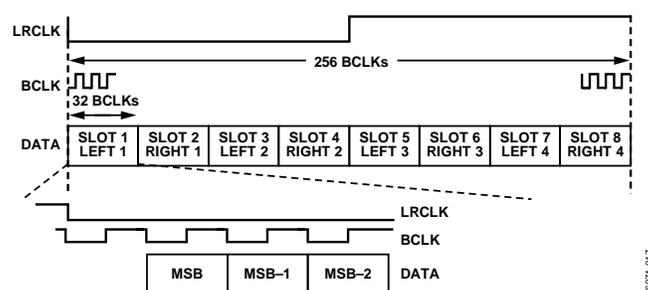


Figure 13. DAC TDM (8-Channel I<sup>2</sup>S Mode)

The I/O pins of the serial ports are defined according to the serial mode that is selected. For a detailed description of the function of each pin in TDM and AUX modes, see Table 12.

The AD1939 allows systems with more than eight DAC channels to be easily configured by the use of an auxiliary serial data port. The DAC TDM-AUX mode is shown in Figure 14. In this mode, the AUX channels are the last four slots of the TDM data stream. These slots are extracted and output to the AUX serial port. It should be noted that due to the high DBCLK frequency, this mode is available only in the 48 kHz/44.1 kHz/32 kHz sample rate.

The AD1939 also allows system configurations with more than four ADC channels as shown in Figure 15 (using 8 ADCs) and Figure 16 (using 16 ADCs). Again, due to the high ABCLK frequency, this mode is available only in the 48 kHz/44.1 kHz/32 kHz sample rate.

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Combining the AUX ADC and DAC modes results in a system configuration of 8 ADCs and 12 DACs. The system, then, consists of two external stereo ADCs, two external stereo DACs,

and one AD1939. This mode is shown in Figure 17 (combined AUX DAC and ADC modes).

**Table 12. Pin Function Changes in TDM and AUX Modes**

Mnemonic	Stereo Modes	TDM Modes	AUX Modes
ASDATA1	ADC1 Data Out	ADC TDM Data Out	TDM Data Out
ASDATA2	ADC2 Data Out	ADC TDM Data In	AUX Data Out 1 (to Ext. DAC 1)
DSDATA1	DAC1 Data In	DAC TDM Data In	TDM Data In
DSDATA2	DAC2 Data In	DAC TDM Data Out	AUX Data In 1 (from Ext. ADC 1)
DSDATA3	DAC3 Data In	DAC TDM Data In 2 (Dual-Line Mode)	AUX Data In 2 (from Ext. ADC 2)
DSDATA4	DAC4 Data In	DAC TDM Data Out 2 (Dual-Line Mode)	AUX Data Out 2 (to Ext. DAC 2)
ALRCLK	ADC LRCLK In/Out	ADC TDM Frame Sync In/Out	TDM Frame Sync In/Out
ABCLK	ADC BCLK In/Out	ADC TDM BCLK In/Out	TDM BCLK In/Out
DLRCLK	DAC LRCLK In/Out	DAC TDM Frame Sync In/Out	AUX LRCLK In/Out
DBCLK	DAC BCLK In/Out	DAC TDM BCLK In/Out	AUX BCLK In/Out

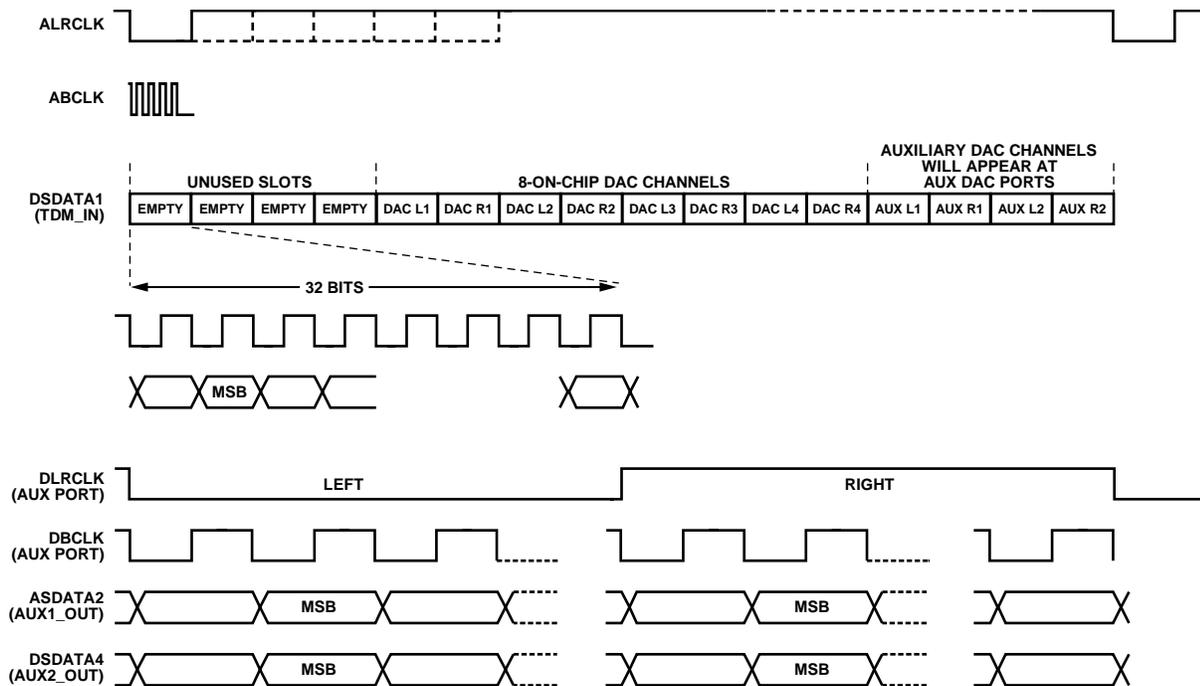


Figure 14. 16-Channel DAC TDM-AUX Mode

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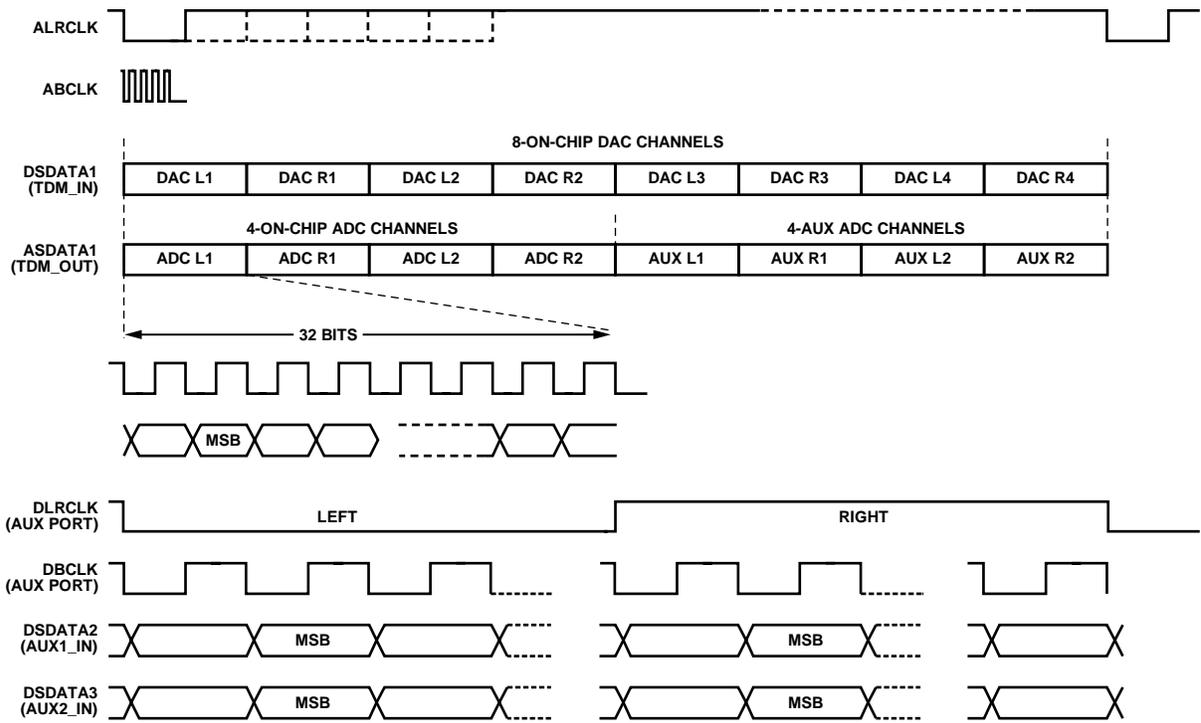


Figure 15. 8-Channel AUX ADC Mode

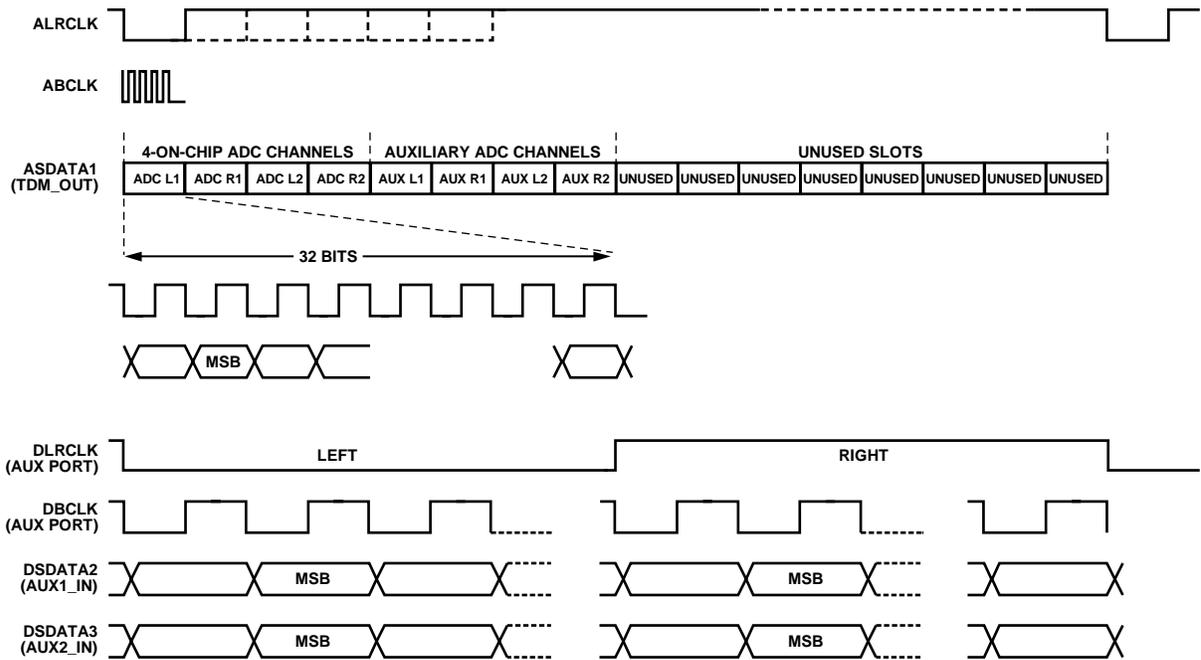


Figure 16. 16-Channel AUX ADC Mode

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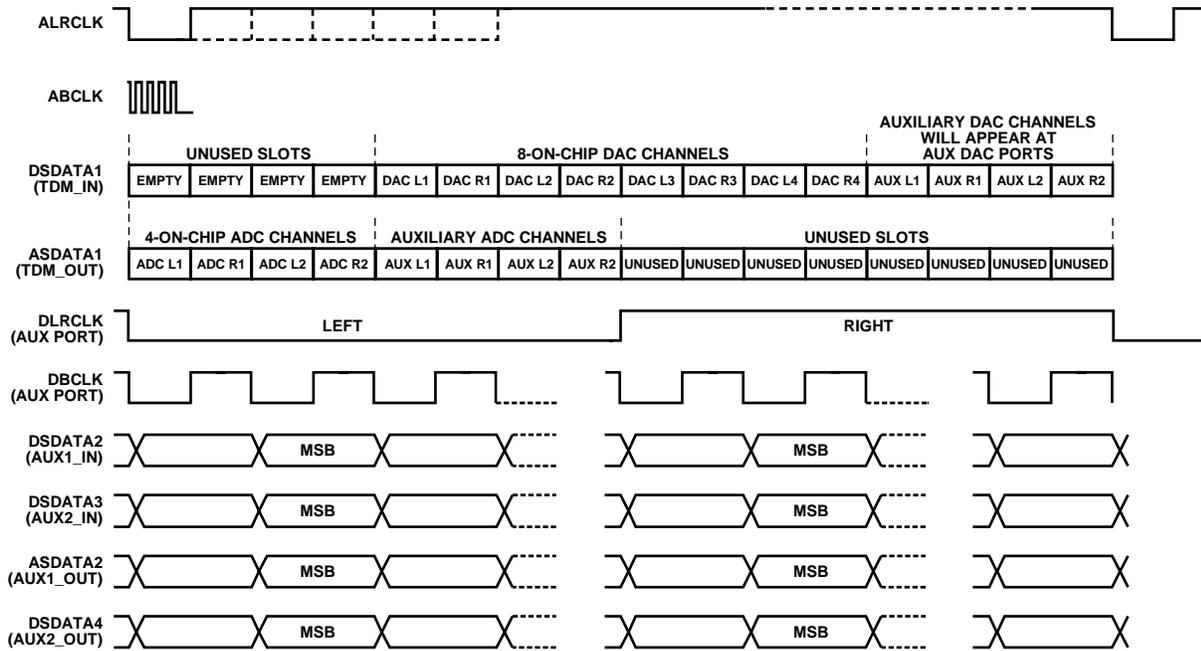


Figure 17. Combined AUX DAC and ADC Mode

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### DAISY-CHAIN MODE

The AD1939 also allows a daisy-chain configuration to expand the system to 8 ADCs and 16 DACs (see Figure 18). In this mode, the DBCLK frequency is 512 f<sub>s</sub>. The first eight slots of the DAC TDM data stream belong to the first AD1939 in the chain and the last eight slots belong to the second AD1939. The second AD1939 is the device attached to the DSP TDM port.

To accommodate 16 channels at a 96 kHz sample rate, the AD1939 can be configured into a dual-line, TDM mode as shown in Figure 19. This mode allows a slower DBCLK than normally required by the one-line TDM mode.

Again, the first four channels of each TDM input belong to the first AD1939 in the chain and the last four channels belong to the second AD1939.

The dual-line TDM mode can also be used to send data at a 192 kHz sample rate into the AD1939 as shown in Figure 20.

There are two configurations for the ADC port to work in daisy-chain mode. The first one is with an ABCLK at 256 f<sub>s</sub> shown in Figure 21. The second configuration is shown in Figure 22. Note that in the 512 f<sub>s</sub> ABCLK mode, the ADC channels occupy the first eight slots; the second eight slots are empty. The TDM\_IN of the first AD1939 must be grounded in all modes of operation.

The I/O pins of the serial ports are defined according to the serial mode selected. See Table 13 for a detailed description of the function of each pin. See Figure 26 for a typical AD1939 configuration with two external stereo DACs and two external stereo ADCs.

Figure 23 through Figure 25 show the serial mode formats. For maximum flexibility, the polarity of LRCLK and BCLK are programmable. In these figures, all of the clocks are shown with their normal polarity. The default mode is I<sup>2</sup>S.

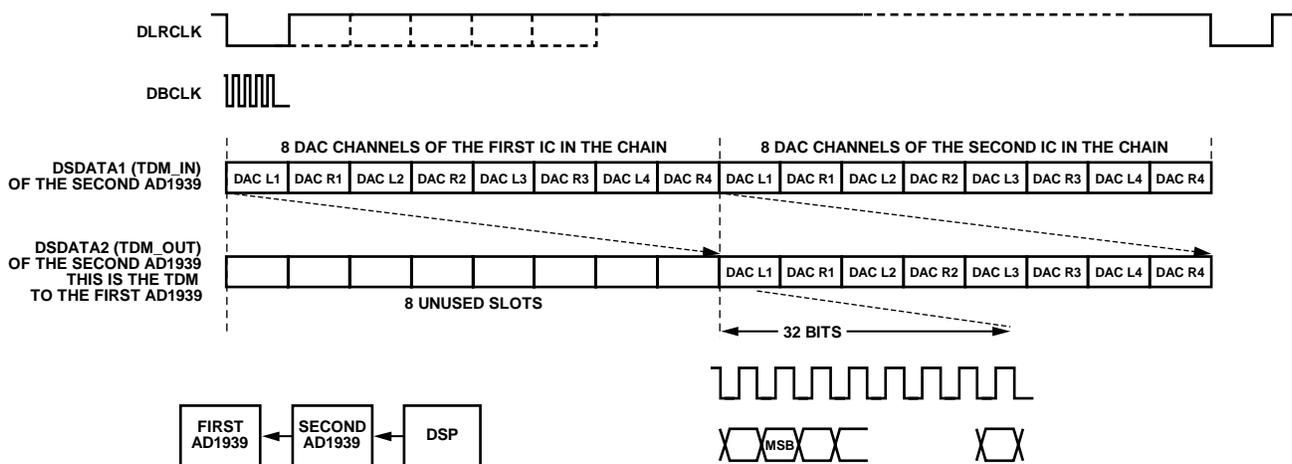
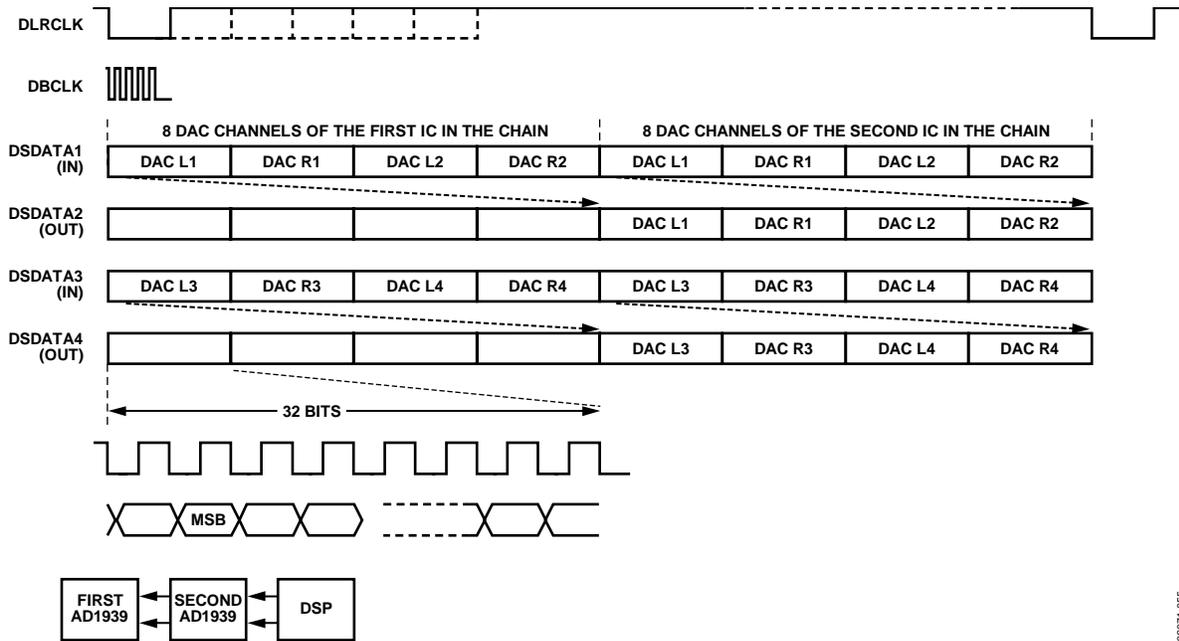


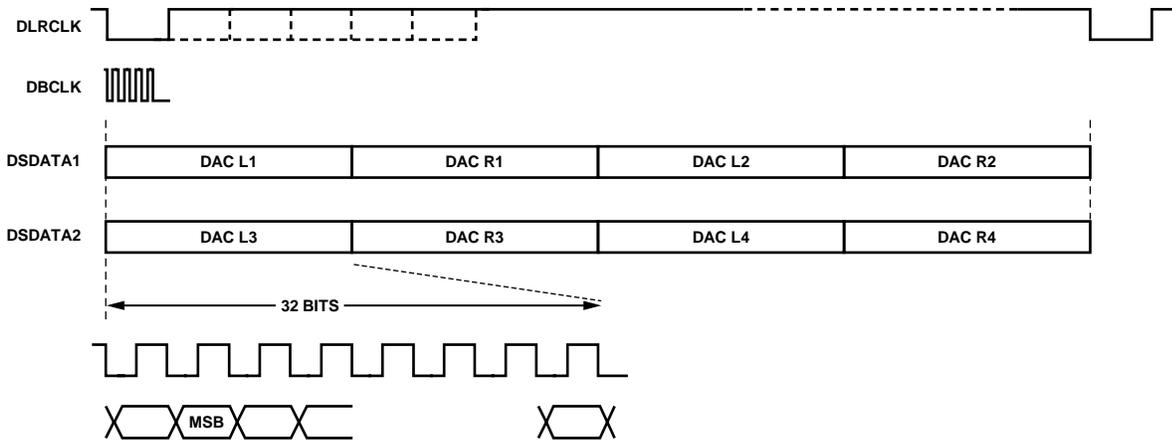
Figure 18. Single-Line DAC TDM Daisy-Chain Mode (Applicable to 48 kHz Sample Rate, 16-Channel, Two-AD1939 Daisy Chain)

# AD1939



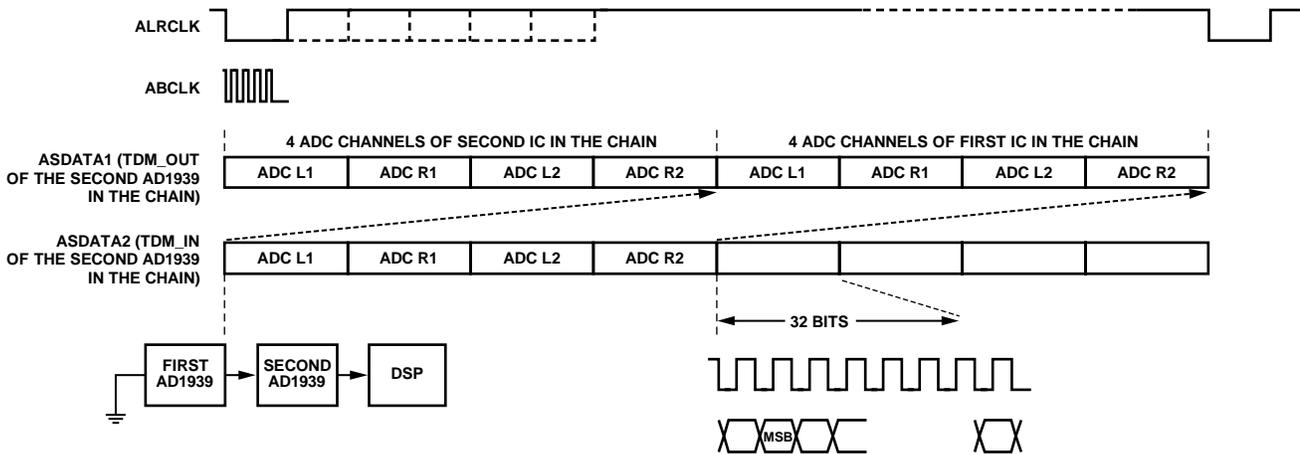
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Figure 19. Dual-Line DAC TDM Mode (Applicable to 96 kHz Sample Rate, 16-Channel, Two-AD1939 Daisy Chain); DSDATA3 and DSDATA4 Are the Daisy Chain



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Figure 20. Dual-Line DAC TDM Mode (Applicable to 192 kHz Sample Rate, 8-Channel Mode)



06071-056

Figure 21. ADC TDM Daisy-Chain Mode (256 fs ABCLK, Two-AD1939 Daisy Chain)

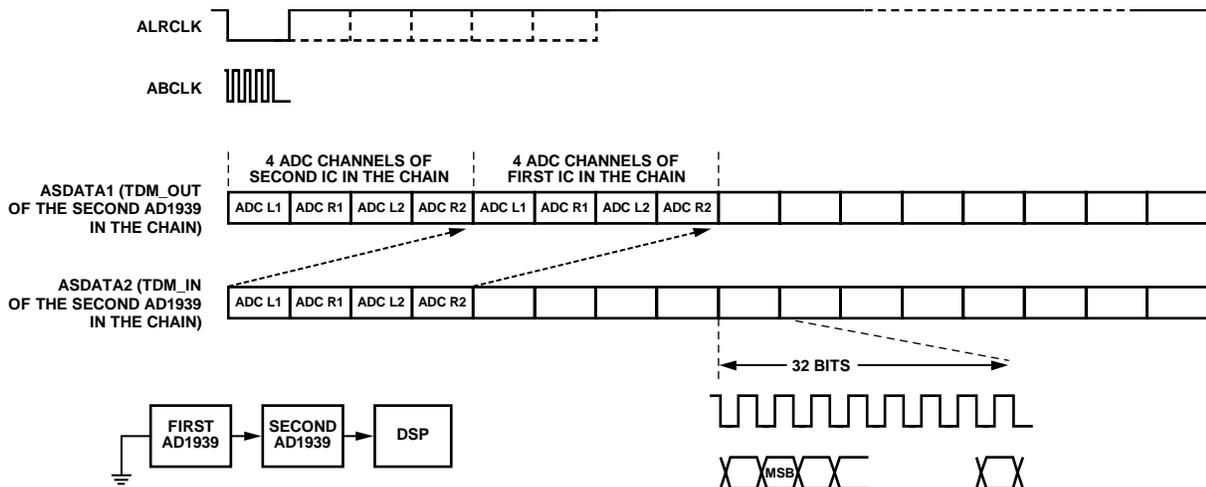
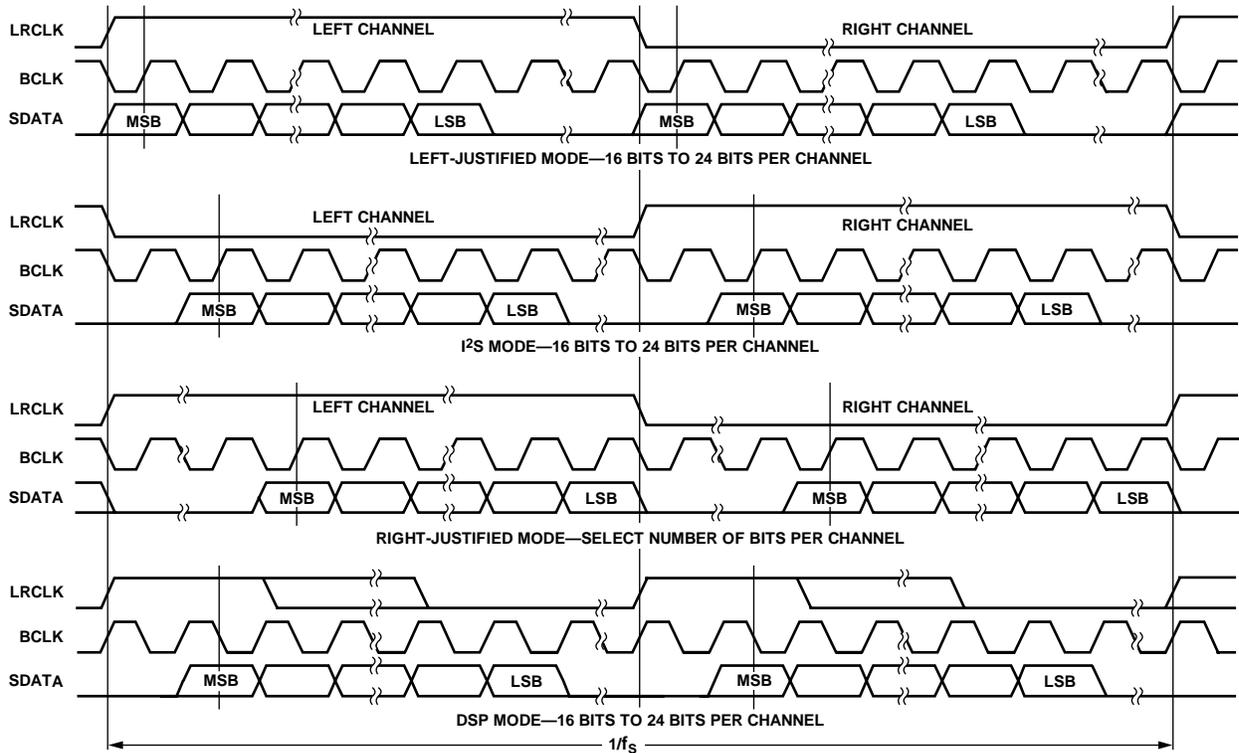


Figure 22. ADC TDM Daisy-Chain Mode (512 fs ABCLK, Two-AD1939 Daisy Chain)



NOTES

1. DSP MODE DOES NOT IDENTIFY CHANNEL.
2. LRCLK NORMALLY OPERATES AT  $f_s$  EXCEPT FOR DSP MODE, WHICH IS  $2 \times f_s$ .
3. BCLK FREQUENCY IS NORMALLY  $64 \times$  LRCLK BUT MAY BE OPERATED IN BURST MODE.

Figure 23. Stereo Serial Modes

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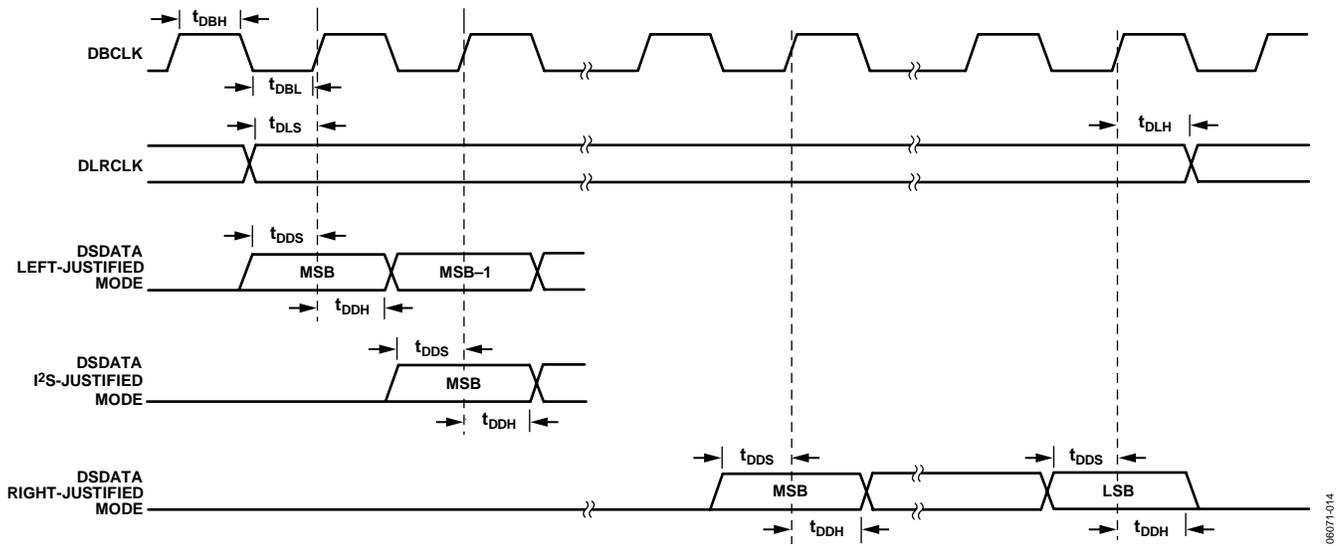


Figure 24. DAC Serial Timing

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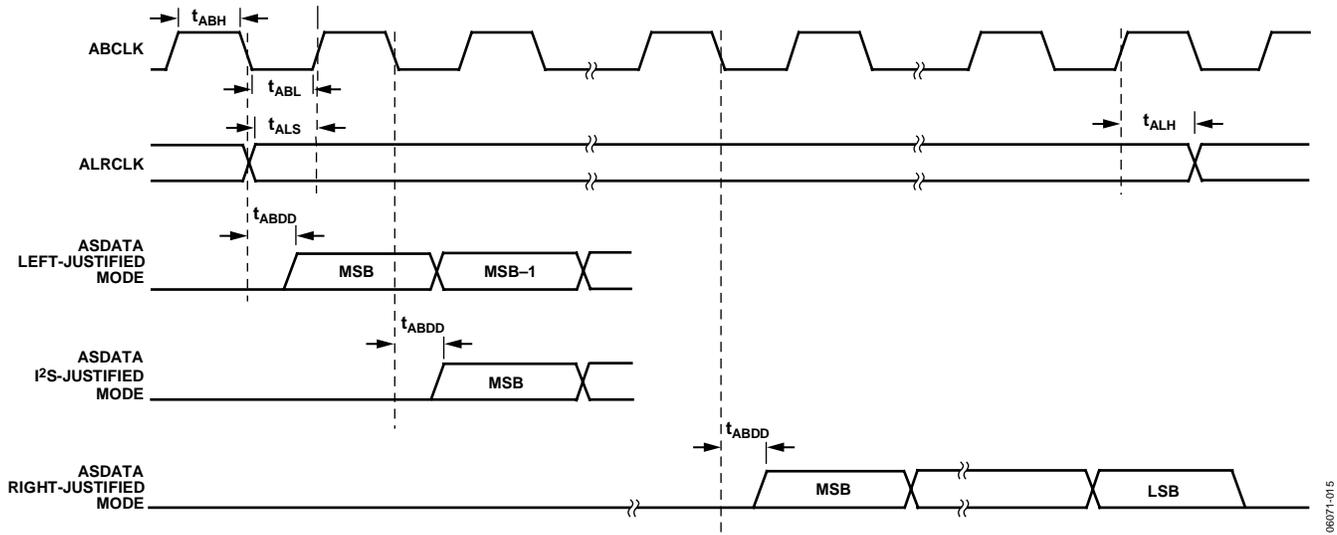


Figure 25. ADC Serial Timing

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Table 13. Pin Function Changes in TDM and AUX Modes (Replication of Table 12)

Mnemonic	Stereo Modes	TDM Modes	AUX Modes
ASDATA1	ADC1 Data Out	ADC TDM Data Out	TDM Data Out
ASDATA2	ADC2 Data Out	ADC TDM Data In	AUX Data Out 1 (to Ext. DAC 1)
DSDATA1	DAC1 Data In	DAC TDM Data In	TDM Data In
DSDATA2	DAC2 Data In	DAC TDM Data Out	AUX Data In 1 (from Ext. ADC 1)
DSDATA3	DAC3 Data In	DAC TDM Data In 2 (Dual-Line Mode)	AUX Data In 2 (from Ext. ADC 2)
DSDATA4	DAC4 Data In	DAC TDM Data Out 2 (Dual-Line Mode)	AUX Data Out 2 (to Ext. DAC 2)
ALRCLK	ADC LRCLK In/Out	ADC TDM Frame Sync In/Out	TDM Frame Sync In/Out
ABCLK	ADC BCLK In/Out	ADC TDM BCLK In/Out	TDM BCLK In/Out
DLRCLK	DAC LRCLK In/Out	DAC TDM Frame Sync In/Out	AUX LRCLK In/Out
DBCLK	DAC BCLK In/Out	DAC TDM BCLK In/Out	AUX BCLK In/Out

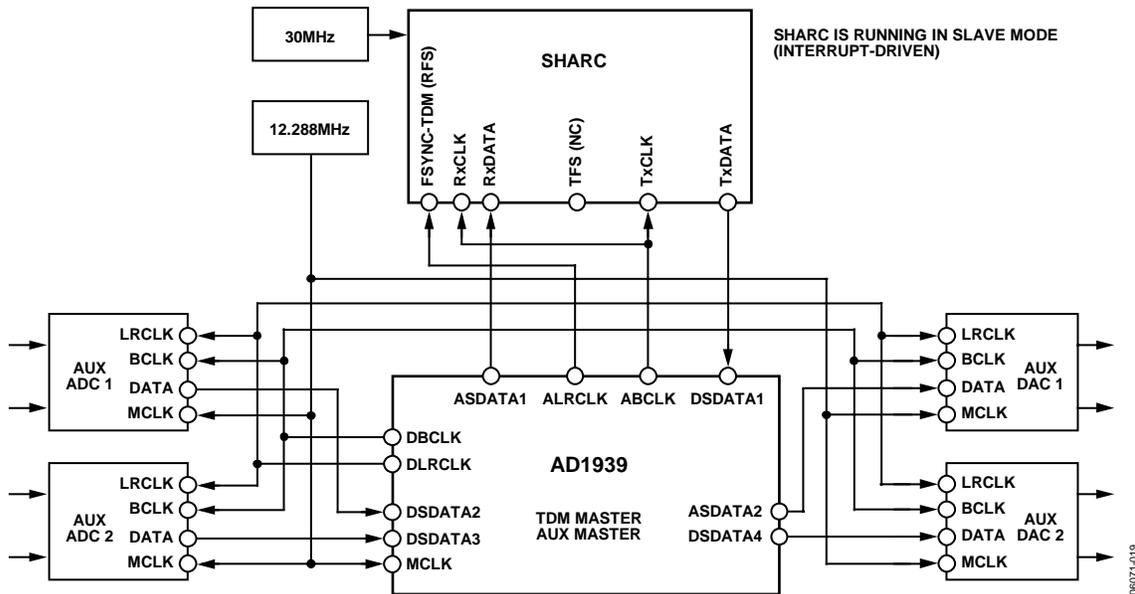


Figure 26. Example of AUX Mode Connection to SHARC (AD1939 as TDM Master/AUX Master Shown)

# AD1939

## CONTROL REGISTERS

### DEFINITIONS

The format is the same for I<sup>2</sup>C and SPI ports. The global address for the AD1939 is 0x04, shifted left one bit due to the R/W bit. However, in I<sup>2</sup>C, ADR0 and ADR1 are ORed into Bit 17 and Bit 8 to provide multiple chip addressing. All registers are reset to 0, except for the DAC volume registers that are set to full volume.

Note that the first setting in each control register parameter is the default setting.

**Table 14. Register Format**

	Global Address	R/W	Register Address	Data
Bit	23:17	16	15:8	7:0

**Table 15. Register Addresses and Functions**

Address	Function
0	PLL and Clock Control 0
1	PLL and Clock Control 1
2	DAC Control 0
3	DAC Control 1
4	DAC Control 2
5	DAC individual channel mutes
6	DAC 1L volume control
7	DAC 1R volume control
8	DAC 2L volume control
9	DAC 2R volume control
10	DAC 3L volume control
11	DAC 3R volume control
12	DAC 4L volume control
13	DAC 4R volume control
14	ADC Control 0
15	ADC Control 1
16	ADC Control 2

### PLL AND CLOCK CONTROL REGISTERS

**Table 16. PLL and Clock Control 0 Register**

Bit	Value	Function	Description
0	0	Normal operation	PLL power-down
	1	Power-down	
2:1	00	INPUT 256 (×44.1 kHz or 48 kHz)	MCLKI/XI
	01	INPUT 384 (×44.1 kHz or 48 kHz)	
	10	INPUT 512 (×44.1 kHz or 48 kHz)	
	11	INPUT 768 (×44.1 kHz or 48 kHz)	
4:3	00	XTAL oscillator enabled	MCLKO/XO pin
	01	256 × f <sub>s</sub> VCO output	
	10	512 × f <sub>s</sub> VCO output	
	11	Off	
6:5	00	MCLKI	PLL input
	01	DLRCLK	
	10	ALRCLK	
	11	Reserved	
7	0	Disable: ADC and DAC idle	Internal master clock enable
	1	Enable: ADC and DAC active	

Table 17. PLL and Clock Control 1 Register

Bit	Value	Function	Description
0	0 1	PLL clock MCLK	DAC clock source select
1	0 1	PLL clock MCLK	ADC clock source select
2	0 1	Enabled Disabled	On-chip voltage reference
3	0 1	Not locked Locked	PLL lock indicator (read only)
7:4	0000	Reserved	

**DAC CONTROL REGISTERS**

Table 18. DAC Control 0 Register

Bit	Value	Function	Description
0	0 1	Normal Power-down	Power-down
2:1	00 01 10 11	32 kHz/44.1 kHz/48 kHz 64 kHz/88.2 kHz/96 kHz 128 kHz/176.4 kHz/192 kHz Reserved	Sample rate
5:3	000 001 010 011 100 101 110 111	1 0 8 12 16 Reserved Reserved Reserved	SDATA delay (BCLK periods)
7:6	00 01 10 11	Stereo (normal) TDM (daisy chain) DAC AUX mode (ADC-, DAC-, TDM-coupled) Dual-line TDM	Serial format

Table 19. DAC Control 1 Register

Bit	Value	Function	Description
0	0 1	Latch in mid cycle (normal) Latch in at end of cycle (pipeline)	BCLK active edge (TDM in)
2:1	00 01 10 11	64 (2 channels) 128 (4 channels) 256 (8 channels) 512 (16 channels)	BCLKs per frame
3	0 1	Left low Left high	LRCLK polarity
4	0 1	Slave Master	LRCLK master/slave
5	0 1	Slave Master	BCLK master/slave
6	0 1	DBCLK pin Internally generated	BCLK source
7	0 1	Normal Inverted	BCLK polarity

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**Table 20. DAC Control 2 Register**

Bit	Value	Function	Description
0	0	Unmute	Master mute
	1	Mute	
2:1	00	Flat	De-emphasis (32 kHz/44.1 kHz/48 kHz mode only)
	01	48 kHz curve	
	10	44.1 kHz curve	
	11	32 kHz curve	
4:3	00	24	Word width
	01	20	
	10	Reserved	
	11	16	
5	0	Noninverted	DAC output polarity
	1	Inverted	
7:6	00	Reserved	

**Table 21. DAC Individual Channel Mutes**

Bit	Value	Function	Description
0	0	Unmute	DAC 1 left mute
	1	Mute	
1	0	Unmute	DAC 1 right mute
	1	Mute	
2	0	Unmute	DAC 2 left mute
	1	Mute	
3	0	Unmute	DAC 2 right mute
	1	Mute	
4	0	Unmute	DAC 3 left mute
	1	Mute	
5	0	Unmute	DAC 3 right mute
	1	Mute	
6	0	Unmute	DAC 4 left mute
	1	Mute	
7	0	Unmute	DAC 4 right mute
	1	Mute	

**Table 22. DAC Volume Controls**

Bit	Value	Function	Description
7:0	0	No attenuation	DAC volume control
	1 to 254	-3/8 dB per step	
	255	Full attenuation	

**ADC CONTROL REGISTERS****Table 23. ADC Control 0 Register**

Bit	Value	Function	Description
0	0	Normal	Power-down
	1	Power down	
1	0	Off	High-pass filter
	1	On	
2	0	Unmute	ADC 1L mute
	1	Mute	
3	0	Unmute	ADC 1R mute
	1	Mute	
4	0	Unmute	ADC 2L mute
	1	Mute	
5	0	Unmute	ADC 2R mute
	1	Mute	
7:6	00	32 kHz/44.1 kHz/48 kHz	Output sample rate
	01	64 kHz/88.2 kHz/96 kHz	
	10	128 kHz/176.4 kHz/192 kHz	
	11	Reserved	

**Table 24. ADC Control 1 Register**

Bit	Value	Function	Description
1:0	00	24	Word width
	01	20	
	10	Reserved	
	11	16	
4:2	000	1	SDATA delay (BCLK periods)
	001	0	
	010	8	
	011	12	
	100	16	
	101	Reserved	
	110	Reserved	
	111	Reserved	
6:5	00	Stereo	Serial format
	01	TDM (daisy chain)	
	10	ADC Aux mode (ADC-, DAC, TDM-coupled)	
	11	Reserved	
7	0	Latch in mid cycle (normal)	BCLK active edge (TDM in)
	1	Latch in at end of cycle (pipeline)	

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Table 25. ADC Control 2 Register

Bit	Value	Function	Description
0	0	50/50 (allows 32-/24-/20-/16-BCLK/channel)	LRCLK format
	1	Pulse (32-BCLK/channel)	
1	0	Drive out on falling edge (DEF)	BCLK polarity
	1	Drive out on rising edge	
2	0	Left low	LRCLK polarity
	1	Left high	
3	0	Slave	LRCLK master/slave
	1	Master	
5:4	00	64	BCLKs per frame
	01	128	
	10	256	
	11	512	
6	0	Slave	BCLK master/slave
	1	Master	
7	0	ABCLK pin	BCLK source
	1	Internally generated	

### ADDITIONAL MODES

The AD1939 offers several additional modes for board level design enhancements. To reduce the EMI in board level design, serial data can be transmitted without an explicit BCLK. See Figure 27 for an example of a DAC TDM data transmission mode that does not require high speed DBCLK. This configuration is applicable when the AD1939 master clock is generated by the PLL with the DLRCLK as the PLL reference frequency.

To relax the requirement for the setup time of the AD1939 in cases of high speed TDM data transmission, the AD1939 can latch in the data using the falling edge of DBCLK. This effectively dedicates the entire BCLK period to the setup time. This mode is useful in cases where the source has a large delay time in the serial data driver. Figure 28 shows this pipeline mode of data transmission.

Both the BCLK-less and pipeline modes are available on the ADC serial data port.

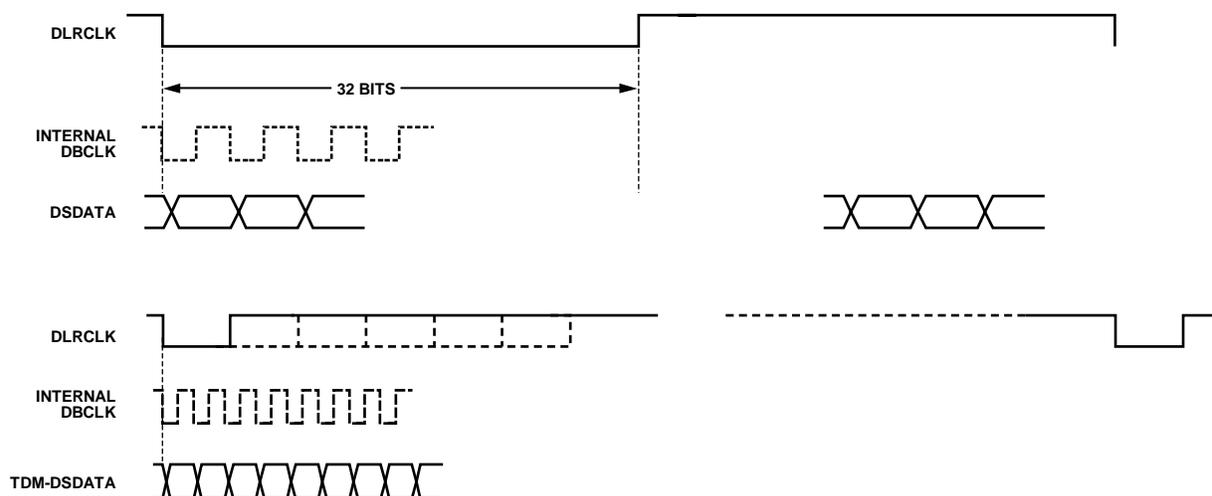


Figure 27. Serial DAC Data Transmission in TDM Format Without DBCLK  
(Applicable Only If PLL Locks to DLRCLK, This Model Is Also Available in the ADC Serial Data Port)

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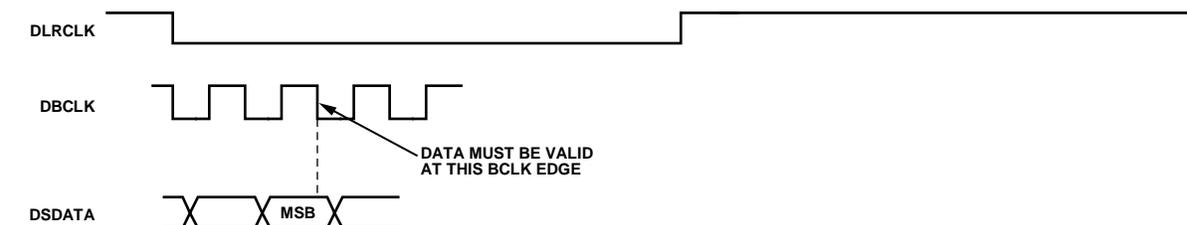


Figure 28. I<sup>2</sup>S Pipeline Mode in DAC Serial Data Transmission  
(Applicable in Stereo and TDM, Useful for High Frequency TDM Transmission, This Model Is Also Available in the ADC Serial Data Port)

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## APPLICATION CIRCUITS

Typical application circuits are shown in Figure 29 through Figure 32. Figure 29 shows a typical ADC input filter circuit. Recommended loop filters for LR clock and master clock as the PLL reference are shown in Figure 30. Output filters for the DAC outputs are shown in Figure 31 and a regulator circuit is shown in Figure 32.

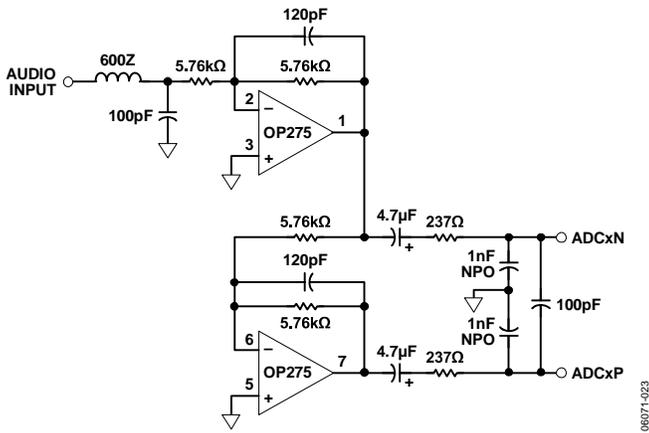


Figure 29. Typical ADC Input Filter Circuit

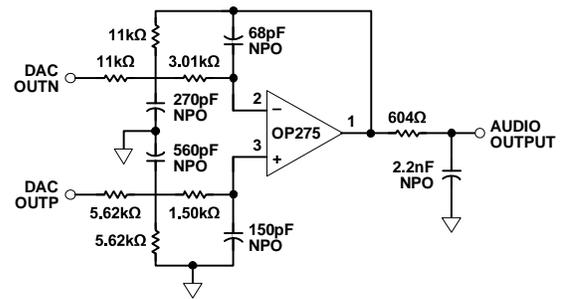


Figure 31. Typical DAC Output Filter Circuit (Differential)

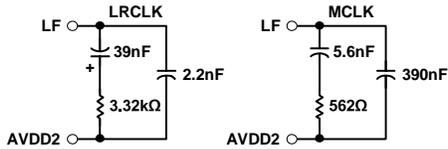


Figure 30. Recommended Loop Filters for LRCLK or MCLK PLL Reference

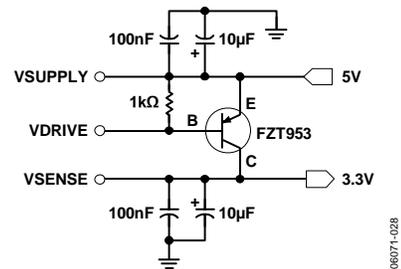
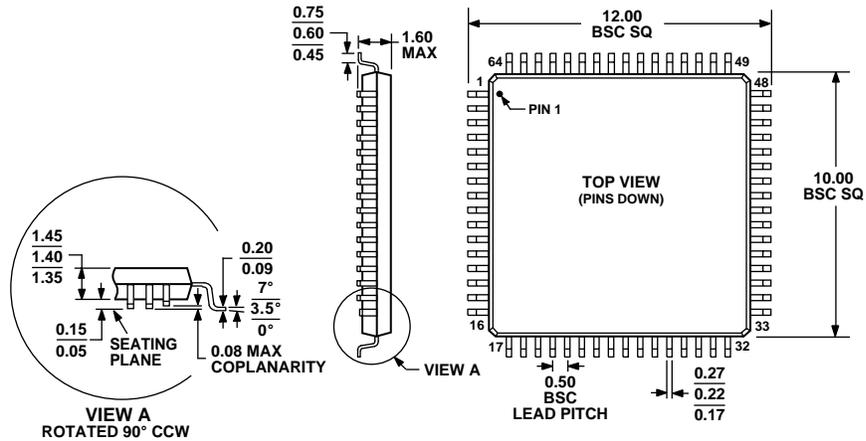


Figure 32. Recommended 3.3 V Regulator Circuit

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 33. 64-Lead Low Profile Quad Flat Package [LQFP] (ST-64-2)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1939YSTZ <sup>1,2</sup>	-40°C to +105°C	64-Lead LQFP	ST-64-2
AD1939YSTZRL	-40°C to +105°C	64-Lead LQFP, 13" Reel	ST-64-2
EVAL-AD1939EB		Evaluation Board	

<sup>1</sup> Z = Pb-free part.

<sup>2</sup> Differential output, SPI control port.

**AD1939**

**NOTES**