# 250 kSPS, 12-Bit Impedance Converter, Network Analyzer

# AD5934

## FEATURES

- Programmable output peak-to-peak excitation voltage to a max frequency of 100 kHz
- Programmable frequency sweep capability with serial I²C® interface
- Frequency resolution of 27 bits (<0.1 Hz)
- Impedance measurement range from 100 Ω to 10 MΩ
- Phase measurement capability
- System accuracy of 0.5%
- 2.7 V to 5.5 V power supply operation
- Temperature range −40°C to +125°C
- 16-lead SSOP package

## APPLICATIONS

- Electrochemical analysis
- Bioelectrical impedance analysis
- Impedance spectroscopy
- Complex impedance measurement
- Corrosion monitoring and protection equipment
- Biomedical and automotive sensors
- Proximity sensing
- Nondestructive testing
- Material property analysis
- Fuel/battery cell condition monitoring

## GENERAL DESCRIPTION

The AD5934 is a high precision impedance converter system solution which combines an on-board frequency generator with a 12-bit, 250 kSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency.

The magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep is easily calculated using the following two equations:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = Tan^{-1}(I / R)$$

**Table 1. Related Devices**

| Part No. | Description |
|---|---|
| AD5933 | 2.7 V to 5.5 V. 1 MSPS, 12-bit impedance, with internal temperature sensor, 16-lead SSOP. |

## FUNCTIONAL BLOCK DIAGRAM

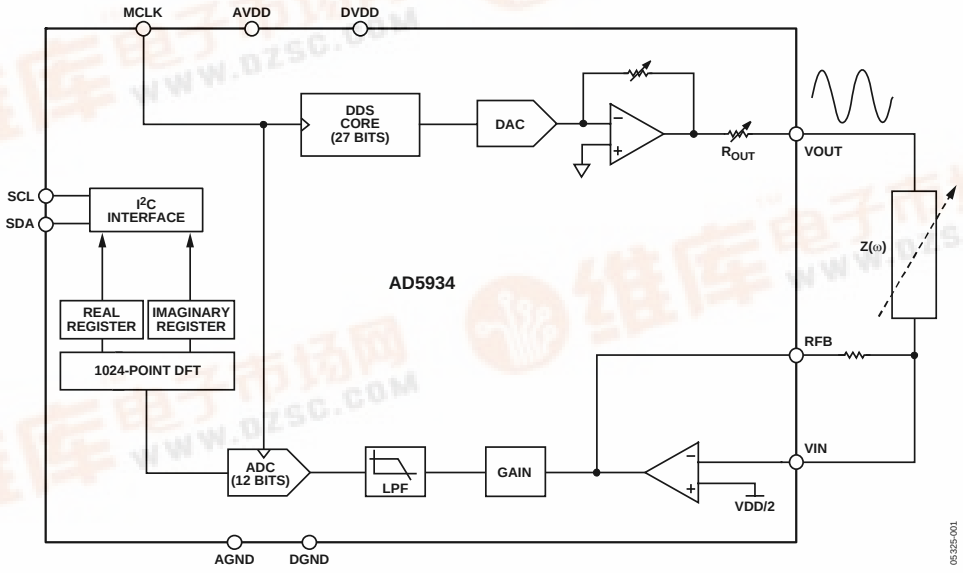


*Figure 1.*



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## REVISION HISTORY

**6/05—Revision 0: Initial Version**

# SPECIFICATIONS

Test conditions unless otherwise stated: VDD = 3.3 V, MCLK = 16.776 MHz, 2 V p-p output excitation voltage @ 30 kHz, 200 kΩ connected between Pin 5 and Pin 6. Feedback resistor = 200 kΩ connected between Pin 4 and Pin 5. PGA gain = ×1.

**Table 2.**

| | Y Version[1] | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments** |
| SYSTEM | | | | | |
| Impedance Range | 0.001 | | 10 | MΩ | |
| Total System Accuracy | | 0.5 | | % | |
| System Impedance Error Drift | | 30 | | ppm/°C | |
| TRANSMIT STAGE | | | | | |
| Output Frequency Range[2] | 1 | | 100 | kHz | |
| Output Frequency Resolution | | 0.1 | | Hz | <0.1 Hz resolution achievable using DDS techniques. |
| MCLK Frequency | | | 16.776 | MHz | Maximum system clock frequency. |
| TRANSMIT OUTPUT VOLTAGE | | | | | |
| Range 1 | | | | | |
| AC Output Excitation Voltage[3] | | 1.98 | | V p-p | Refer to Figure 4 for output voltage distribution. |
| DC Bias[4] | | 1.48 | | V | DC bias of the AC excitation signal. See Figure 5. |
| DC Output Impedance | | 200 | | Ω | $T_A$ = 25°C. |
| Short-Circuit Current to Ground at VOUT | | ±5.8 | | mA | $T_A$ = 25°C. |
| Range 2 | | | | | |
| AC Output Excitation Voltage[3] | | 0.97 | | V p-p | See Figure 6. |
| DC Bias[4] | | 0.76 | | V | DC bias of output excitation signal. See Figure 7. |
| DC Output Impedance | | 2.4 | | kΩ | |
| Short-Circuit Current to Ground at VOUT | | ±0.25 | | mA | |
| Range 3 | | | | | |
| AC Output Excitation Voltage[3] | | 0.383 | | V p-p | See Figure 8. |
| DC Bias[4] | | 0.31 | | V | DC bias of output excitation signal. See Figure 9. |
| DC Output Impedance | | 1 | | kΩ | |
| Short-Circuit Current to Ground at VOUT | | ±0.20 | | mA | |
| Range 4 | | | | | |
| AC Output Excitation Voltage[3] | | 0.198 | | V p-p | See Figure 10. |
| DC Bias[4] | | 0.173 | | V | DC bias of output excitation signal. See Figure 11. |
| DC Output Impedance | | 600 | | Ω | |
| Short-Circuit Current to Ground at VOUT | | ±0.15 | | mA | |
| Short-Circuit Current to Ground | | ±0.15 | | mA | |
| SYSTEM AC CHARACTERISTICS | | | | | |
| Signal-to-Noise Ratio | | 60 | | dB | |
| Total Harmonic Distortion | | −52 | | dB | |
| Spurious-Free Dynamic Range | | | | | |
| Wide Band (0 MHz to 1 MHz) | | −56 | | dB | |
| Narrowband (±5 kHz) | | −85 | | dB | |

| Parameter | Y Version[1] Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| RECEIVE STAGE | | | | | |
| Input Leakage Current | | 1 | | nA | To VIN pin. |
| Input Capacitance[5] | | 0.01 | | fF | Pin capacitance between VOUT and GND. |
| Feedback Capacitance $C_{FB}$ | | 3 | | pF | Feedback capacitance around current-to-voltage amplifier; appears in parallel with feedback resistor. |
| ANALOG-TO-DIGITAL CONVERTER[5] | | | | | |
| Resolution | | 12 | | bits | |
| Sampling Rate | | 250 | | kSPS | ADC throughput rate. |
| LOGIC INPUTS | | | | | |
| Input High Voltage ($V_{IH}$) | 0.7 × VDD | | | | |
| Input Low Voltage ($V_{IL}$) | | | 0.3 × VDD | | |
| Input Current[6] | | | 1 | μA | $T_A$ =25°C. |
| Input Capacitance | | | 7 | pF | $T_A$ = 25°C. |
| POWER REQUIREMENTS | | | | | |
| VDD | 2.7 | | 5.5 | V | |
| IDD (Normal Mode ) | | 10 | 15 | mA | VDD = 3.3 V. |
| | | 17 | 25 | mA | VDD = 5.5 V. |
| IDD (Standby Mode) | | 7 | | mA | VDD = 3.3 V; see the Control Register section. |
| | | 9 | | mA | VDD = 5.5 V. |
| IDD (Power-Down Mode) | | 0.7 | 5 | μA | VDD = 3.3 V. |
| | | 1 | 8 | μA | VDD = 5.5 V. |

[1] Temperature range for Y version = −40°C to +125°C, typical at 25°C.
[2] The lower limit of the output excitation frequency can be lowered by scaling the clock supplied to the AD5934.
[3] The peak-to-peak value of the AC output excitation voltage scales with supply voltage according to the formula given below. VDD is the supply voltage.

$$Output\ Excitation\ Voltage\ (\text{V p - p}) = \frac{2}{3.3} \times VDD$$

[4] The DC bias value of the Output excitation voltage scales with supply voltage according to the formula given below. VDD is the supply voltage.

$$Output\ Excitation\ Bias\ Voltage\ (\text{V}) = \frac{2}{3.3} \times VDD$$

[5] Guaranteed by design or characterization, not production tested. Input capacitance at the VOUT pin is equal to pin capacitance divided by open-loop gain of current-to-voltage amplifier.
[6] The accumulation of the currents into Pin 8, Pin 15, and Pin 16.

# I²C SERIAL INTERFACE TIMING CHARACTERISTICS

VDD = 2.7 V to 5.5 V. All specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.[1]

**Table 3.**

| Parameter[2] | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $F_{SCL}$ | 400 | kHz max | SCL clock frequency |
| $t_1$ | 2. 5 | µs min | SCL cycle time |
| $t_2$ | 0. 6 | µs min | $t_{HIGH}$, SCL high time |
| $t_3$ | 1. 3 | µs min | $t_{LOW}$, SCL low time |
| $t_4$ | 0. 6 | µs min | $t_{HD, STA}$, start/repeated start condition hold time |
| $t_5$ | 100 | ns min | $t_{SU, DAT}$, data setup time |
| $t_6$[3] | 0. 9 | µs max | $t_{HD, DAT}$, data hold time |
| | 0 | µs min | $t_{HD, DAT}$, data hold time |
| $t_7$ | 0. 6 | µs min | $t_{SU, STA}$, setup time for repeated start |
| $t_8$ | 0. 6 | µs min | $t_{SU, STO}$, stop condition setup time |
| $t_9$ | 1. 3 | µs min | $t_{BUF}$, bus free time between a stop and a start condition |
| $t_{10}$ | 300 | ns max | $t_F$, rise time of SDA when transmitting |
| | 0 | ns min | $t_R$, rise time of SCL and SDA when receiving (CMOS compatible) |
| $t_{11}$ | 300 | ns max | $t_F$, fall time of SCL and SDA when transmitting |
| | 0 | ns min | $t_F$, fall time of SDA when receiving (CMOS compatible) |
| | 250 | ns max | $t_F$, fall time of SDA when receiving |
| | 20 + 0.1 $C_B$[4] | ns min | $t_F$, fall time of SCL and SDA when transmitting |
| $C_B$ | 400 | pF max | Capacitive load for each bus line |

[1] See Figure 2.
[2] Guaranteed by design and characterization, not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined SCL's falling edge.
[4] $C_B$ is the total capacitance of one bus line in pF. Note that $t_R$ and $t_F$ are measured between 0.3 VDD and 0.7 VDD.

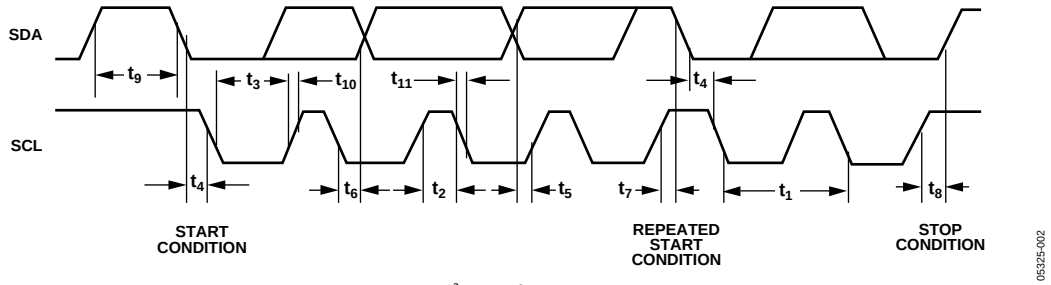


*Figure 2. I²C Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise note

**Table 4.**

| Parameter | Rating |
|---|---|
| DVDD to GND | −0.3 V to + 7. 0 V |
| AVDD1 to GND | −0.3 V to + 7. 0 V |
| AVDD2 to GND | −0.3 V to + 7. 0 V |
| SDA/SCL to GND | −0.3 V to VDD + 0.3 V |
| VOUT to GND | −0.3 V to VDD + 0.3 V |
| VIN to GND | −0.3 V to VDD + 0.3 V |
| MCLK to GND | −0.3 V to VDD + 0.3 V |
| Operating Temperature Range | |
| Extended Industrial (Y Grade) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +160°C |
| Maximum Junction Temperature | 150°C |
| SSOP Package | |
| $\theta_{JA}$ Thermal Impedance | 139°C/W |
| $\theta_{JC}$ Thermal Impedance | 136°C/W |
| Reflow Soldering (Pb-Free) | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 10 sec to 40 sec |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND DESCRIPTIONS

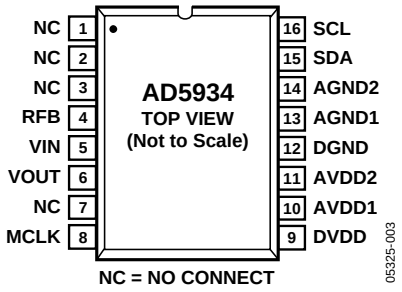


*Figure 3. Pin Configuration*

It is recommended to tie all supply connections (Pin 9, Pin 10, and Pin 11) and run from a single supply between 2.7 V and 5.5 V. It is also recommended to connect all ground signals together (Pin 12, Pin 13, and Pin 14).

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description/comment |
|---|---|---|
| 1, 2, 3, 7 | NC | No Connect. |
| 4 | RFB | External Feedback Resistor. Connected from Pin 4 to Pin 5 and used to set the gain of the current-to-voltage amplifier on the receive side. |
| 5 | VIN | Input to Receive Transimpedance Amplifier. Presents a virtual earth voltage of VDD/2. |
| 6 | VOUT | Excitation Voltage Signal Output. |
| 8 | MCLK | Master Clock for the System. Supplied by user. |
| 9 | DVDD | Digital Supply Voltage. |
| 10 | AVDD1 | Analog Supply Voltage 1. |
| 11 | AVDD2 | Analog Supply Voltage 2. |
| 12 | DGND | Digital Ground. |
| 13 | AGND1 | Analog Ground 1. |
| 14 | AGND2 | Analog Ground 2. |
| 15 | SDA | $I^2C$ Data Input. |
| 16 | SCL | $I^2C$ Clock Input. |

# TYPICAL PERFORMANCE CHARACTERISTICS

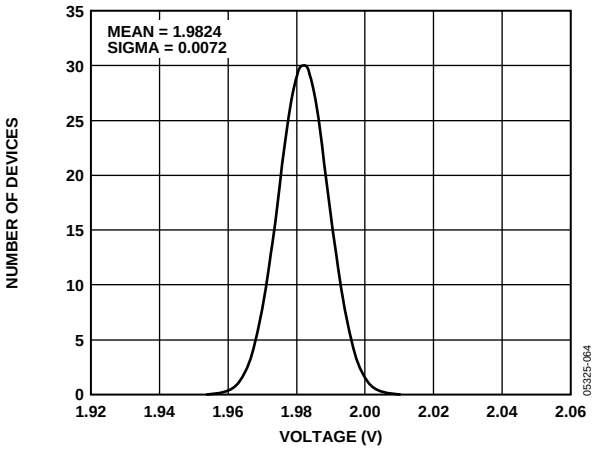


*Figure 4. Range 1: Output Excitation Voltage Distribution VDD = 3.3 V*

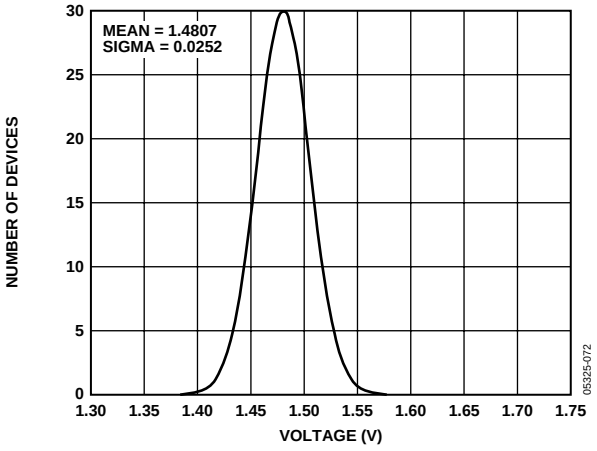


*Figure 5. Range 1: DC Bias Distribution VDD = 3.3 V*

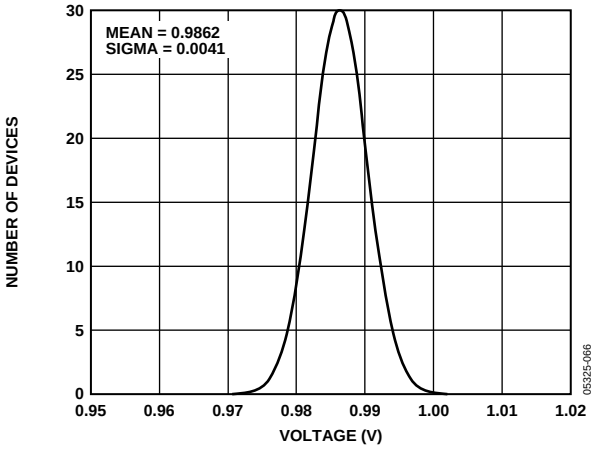


*Figure 6. Range 2: Output Excitation Voltage Distribution VDD = 3.3 V*

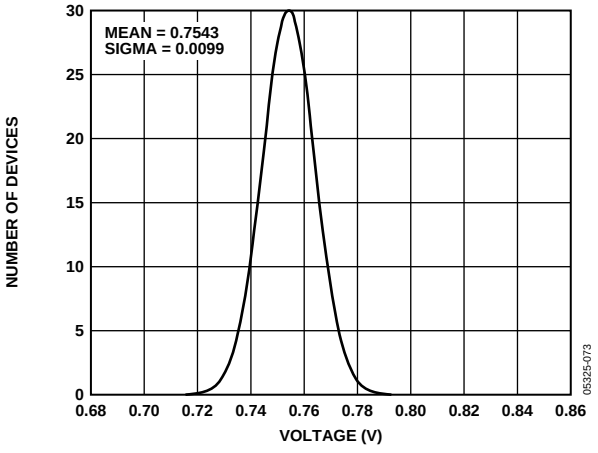


*Figure 7. Range 2: DC Bias Distribution VDD = 3.3 V*

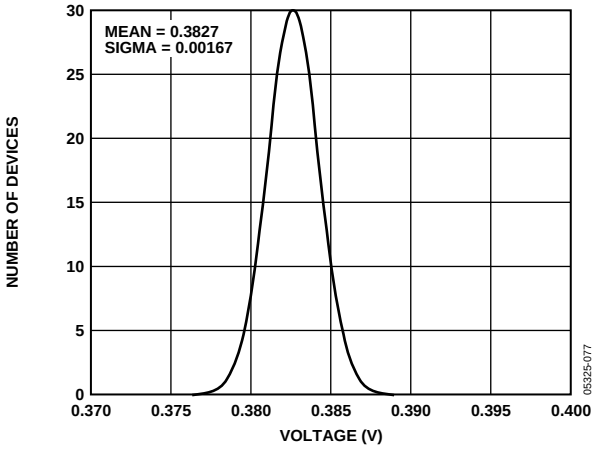


*Figure 8. Range 3: Output Excitation Voltage Distribution VDD = 3.3 V*

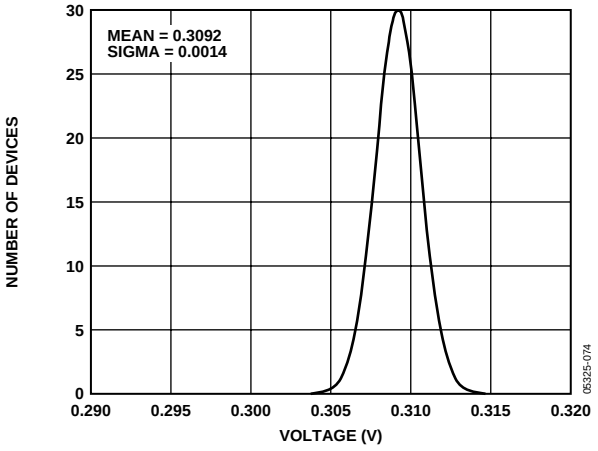


*Figure 9. Range 3: DC Bias Distribution VDD = 3.3 V*

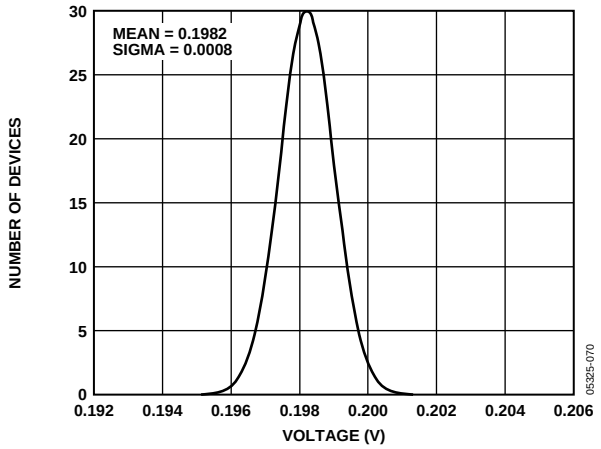


Figure 10. Range 4: Output Excitation Voltage Distribution VDD = 3.3 V

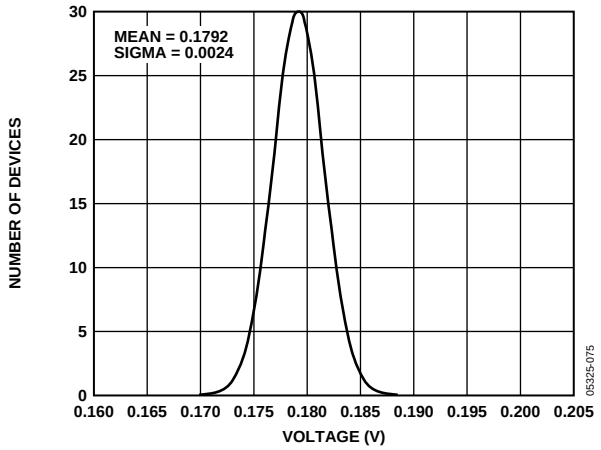


Figure 11. Range 4: DC Bias Distribution VDD = 3.3 V

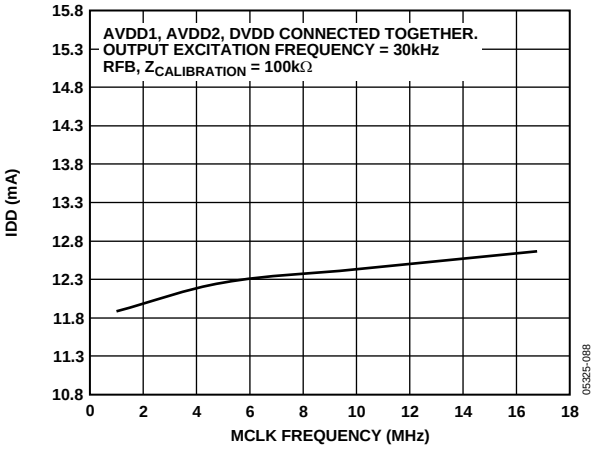


Figure 12. Typical Supply Current vs. AD5934 Clock Frequency

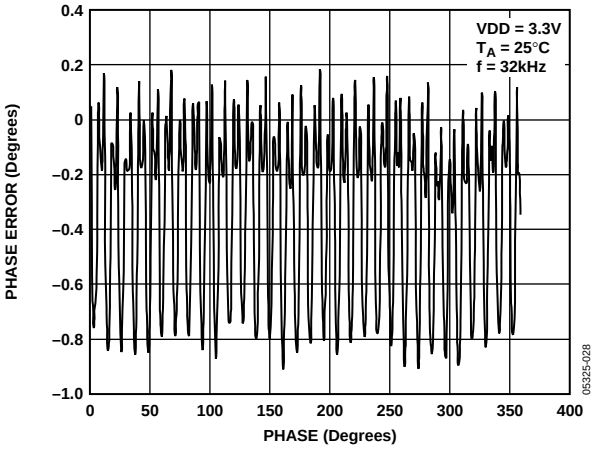


Figure 13. Typical AD5934 Phase Error

# TERMINOLOGY

**Total System Accuracy**
The AD5934 can accurately measure a range of impedance values to less than 0.5% of the correct impedance value for supply voltages between 2.7 V to 5.5 V.

**Spurious-Free Dynamic Range** (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the 0 to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz, about the fundamental frequency.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

**Total Harmonic Distortion** (THD)
THD is the ratio of the rms sum of harmonics to the fundamental, where V1 is the rms amplitude of the fundamental and V2, V3, V4, V5, and V6 are the rms amplitudes of the second through the sixth harmonics. For the AD5934, THD is defined as

$$THD(\text{db}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V^2{}_6}}{V_1}$$

# SYSTEM DESCRIPTION

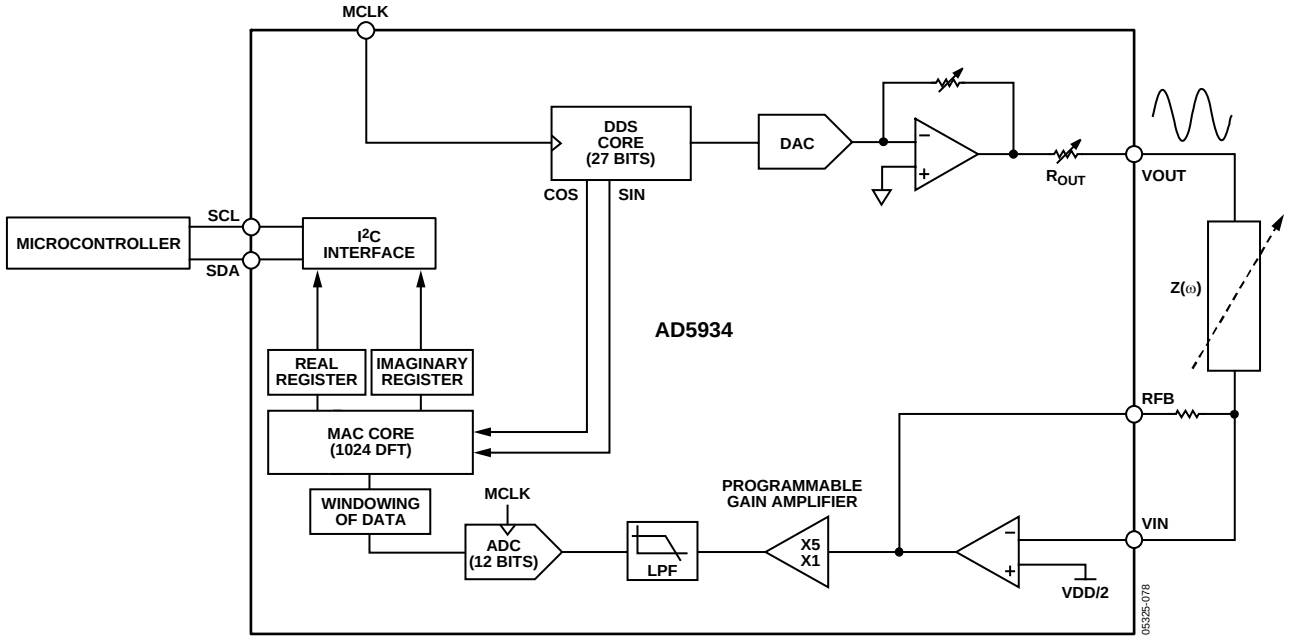


*Figure 14. AD5934 Block Overview*

The AD5934 is a high precision impedance converter system solution which combines an on-board frequency generator with a 12-bit, 250 kSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and DFT processed by an on-board DSP engine. The DFT algorithm returns both a real (R) and imaginary (I) data-word at each frequency point along the sweep. The impedance magnitude and phase is easily calculated using the following equations:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = Tan^{-1}(I/R)$$

To characterize an impedance profile Z(ω), generally a frequency sweep is required like that shown in Figure 15.

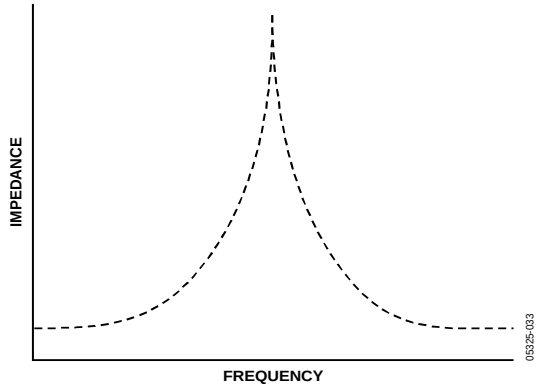


*Figure 15.*

The AD5934 permits the user to perform a frequency sweep with a user-defined start frequency, frequency resolution, and number of points in the sweep. In addition, the device allows the user to program the peak-to-peak value of the output sinusoidal signal as an excitation to the external unknown impedance connected between the VOUT and VIN pins.

Table 6 gives the four possible output peak-to-peak voltages and the corresponding dc bias levels for each range.

**Table 6.**

| Output Excitation Voltage Amplitude | Output DC Bias Level |
|---|---|
| Range 1: 1.98 V p-p | 1.48 V |
| Range 2: 0.99 V p-p | 0.74V |
| Range 3: 383 mV p-p | 0.31 V |
| Range 4: 198 mV p-p | 0.179 V |

The excitation signal for the transmit stage is provided on-chip using DDS techniques which permit subhertz resolution. The receive stage receives the input signal current from the unknown impedance, performs signal processing, and digitizes the result. The clock for the DDS is generated from an external reference clock which is provided by the user at MCLK.

## TRANSMIT STAGE

As shown in Figure 16, the transmit stage of the AD5934 is made up of a 27-bit phase accumulator DDS core which provides the output excitation signal at a particular frequency. The input to the phase accumulator is taken from the contents of the START FREQUENCY register (see RAM Locations 82h, 83h, and 84h). Although the phase accumulator offers 27 bits of resolution, the START FREQUENCY register has the 3 most significant bits (MSBs) set to 0 internally; therefore the user has the ability to program only the lower 24 bits of the START FREQUENCY register.

The AD5934 offers a frequency resolution programmable by the user down to 0.1 Hz. The frequency resolution is programmed via a 24-bit word loaded serially over the I²C interface to the FREQUENCY INCREMENT register.

The frequency sweep is fully described by the programming of three parameters: the START FREQUENCY, the FREQUENCY INCREMENT, and the NUMBER OF INCREMENTS.

### START FREQUENCY

This is a 24-bit word that is programmed to the on-board RAM at Address 82h, Address 83h, and Address 84h (see the Register Map section). The required code loaded to the START FREQUENCY register is the result of the formula shown in Equation 1, based on the master clock frequency and the required start frequency output from the DDS.

$$Start\ Frequency\ Code = \left( \frac{Required\ Output\ Start\ Frequency}{\left( \frac{MCLK}{16} \right)} \right) \times 2^{27} \quad (1)$$

For example, if the user requires the sweep to begin at 30 kHz and has a 16 MHz clock signal connected to MCLK. The code that needs to be programmed is given by

$$Start\ Frequency\ Code = \left( \frac{30\ \text{kHz}}{\left( \frac{16\ \text{MHz}}{16} \right)} \right) \times 2^{27} \equiv \text{3D70A3 hexidecimal}$$

The user programs 3D hex to Register 82 h, 70 hex to Register 83 h, and A3 hex to Register 84 h.

### FREQUENCY INCREMENT

This is a 24-bit word that is programmed to the on-board RAM at Address 85 h, Address 86 h, and Address 87 h (see the Register Map section). The required code loaded to the frequency increment register is the result of the formula shown in Equation 2, based on the master clock frequency and the required increment frequency output from the DDS.

$$Frequency\ Increment\ Code = \left( \frac{RequiredFrequencyIncrement}{\left( \frac{MCLK}{16} \right)} \right) \times 2^{27} \quad (2)$$

For example, if the user requires the sweep to have a resolution of 10 Hz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Frequency\ Increment\ Code = \left( \frac{10\ \text{Hz}}{\left( \frac{16\ \text{MHz}}{16} \right)} \right) \equiv \text{00053E hexidecimal}$$

The user programs 00 hex to Register 85 h, 05 hex to Register 86 h, and finally 3E hex to Register 87 h.

### NUMBER OF INCREMENTS

This is a 9-bit word that represents the number of frequency points in the sweep. The number is programmed to the on-board RAM at Address 88 h and Address 89 h (see the Register Map section). The maximum number of points that can be programmed is 511.

For example, if the sweep needs 150 points, the user programs 00 hex to Register 88 h and 96 hex to Register 89 h.

Once the three parameter values have been programmed, the sweep is initiated by issuing a Start Frequency Sweep command to the CONTROL register at Address 80 h and Address 81 h (see the Register Map section). Bit 2 in the STATUS register (Register 8F h) indicates the completion of the frequency measurement for each sweep point. Incrementing to the next frequency sweep point is under the control of the user. The measured result is stored in two registers (94 h, 95 h and 96 h, 97 h) which should be read before issuing an Increment Frequency command to the CONTROL register to move to the next sweep point. There is the facility to repeat the current frequency point measurement by issuing a Repeat Frequency command to the CONTROL register. This has the benefit of allowing the user to average successive readings. When the frequency sweep has completed all frequency points, Bit 3 in the STATUS register is set, indicating completion of the sweep. Once this bit is set further increments are disabled.

## FREQUENCY SWEEP COMMAND SEQUENCE

The following sequence must be followed to implement a frequency sweep.

1. Enter standby mode.
   Prior to issuing a Start Frequency Sweep command, the device must be placed in a standby mode by issuing an Enter Standby Mode command to the CONTROL register (Register 80 h). In this mode, the VOUT and VIN pins are connected internally to ground so there is no dc bias across the external impedance or between the impedance and ground.
2. Enter initialize mode.
   In general, high Q complex circuits require a long time to reach steady state. To facilitate the measurement of such impedances, this mode allows the user full control of the settling time requirement before entering start frequency sweep mode where the impedance measurement takes place.

   An Initialize with Start Frequency Command to the CONTROL register enters initialize mode. In this mode the impedance is excited with the programmed start frequency but no measurement takes place. The user times out the required settling time before issuing a Start Frequency Sweep command to the CONTROL register to enter the start frequency sweep mode.
3. Enter start frequency sweep mode.
   The user enters this mode by issuing a Start Frequency Sweep command to the control register. In this mode, the ADC starts measuring after the programmed Number of Settling Time Cycles has elapsed. The user can program an integer number of output frequency cycles (settling time cycles) to Register 8A h and Register 8B h before beginning the measurement at each frequency point (see Figure 28).

The DDS output signal is passed through a programmable gain stage in order to generate the four ranges of peak-to-peak output excitation signals listed in Table 6. The peak-to-peak output excitation voltage is selected by setting Bit D10 and Bit D9 in the CONTROL register—see the Control Register section—and is made available at the VOUT pin.

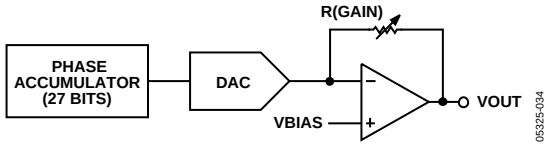


*Figure 16. AD5934 Transmit Stage*

## RECEIVE STAGE

The receive stage comprises a current–to-voltage amplifier, followed by a programmable gain amplifier (PGA), antialiasing filter, and ADC. The receive stage schematic is shown in Figure 17. The unknown impedance is connected between the VOUT and VIN pins. The first stage current-to-voltage amplifier configuration means that a voltage present at the VIN pin is a virtual ground with a dc value set at VDD/2. The signal current that is developed across the unknown impedance flows into the VIN pin and develops a voltage signal at the output of the current-to-voltage converter. The gain of the current-to voltage amplifier is determined by a user-selectable feedback resistor connected between Pins 4 (RFB) and Pin 5 (VIN). It is important for the user to choose a feedback resistance value which, in conjunction with the selected gain of the PGA stage, maintains the signal within the linear range of the ADC (0 V to VDD).

The PGA allows the user to gain the output of the current-to-voltage amplifier by a factor of 5 or 1 depending upon the status of Bit D8 in the CONTROL register (see the Register Map section Register 81h). The signal is then low-pass filtered and presented to the input of the 12-bit, 250 kSPS ADC.

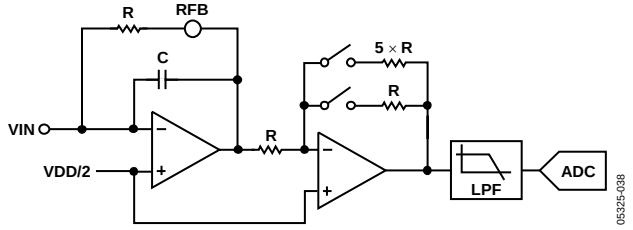


*Figure 17. AD5934 Receive Stage*

The digital data from the ADC is passed directly to the DSP core of the AD5934 which performs a DFT on the sampled data.

## DFT OPERATION

A DFT is calculated for each frequency point in the sweep. The AD5934 DFT algorithm is represented by

$$X(f) = \sum_{n=0}^{1023} \left( x(n)(\cos(n) - j\sin(n)) \right)$$

where *X(f)* is the power in the signal at the frequency point f, *x(n)* is the ADC output, with the cos(n) and sin(n) the sampled test vectors provided by the DDS core at the frequency f**.**

The multiplication is accumulated over 1024 samples for each frequency point. The result is stored in two, 16-bit registers representing the real and imaginary components of the result. The data is stored in twos complement format.

# IMPEDANCE CALCULATION

## MAGNITUDE CALCULATION

The first step in impedance calculation for each frequency point is to calculate the magnitude of the DFT at that point.

The DFT magnitude is given by

$$Magnitude = \sqrt{R^2 + I^2}$$

where R is the real number stored at Register Address 94 h and Register Address 95 h and I is the imaginary number stored at Register Address 96 h and Register Address 97 h.

For example, assume the results in the real and imaginary registers are as follows at a frequency point:

Real register: = 038B hex = 907 decimal
Imaginary register: = 0204 hex = 516 decimal

$$Magnitude = \sqrt{(907^2 + 516^2)} = 1043.506$$

To convert this number into an impedance, it must be multiplied by a scaling factor called the gain factor. The gain factor is calculated during the calibration of the system with a known impedance connected between the VOUT and VIN pins.

Once the gain factor has been calculated, it can be used in the calculation of any unknown impedance between the VOUT and VIN pins.

## GAIN FACTOR CALCULATION

An example of a gain factor calculation follows, with these assumptions:

Output excitation voltage = 2 V (p-p)
Calibration impedance value, $Z_{CALIBRATION}$ = 200 kΩ
PGA gain = ×1
Current to voltage amplifier gain resistor = 200 kΩ
Calibration frequency = 30 kHz

Then typical contents of the real and imaginary register after a frequency point conversion would be

Real register: = F9C hex = -3996 decimal
Imaginary register: = 227E hex = 8830 decimal

$$Magnitude = \sqrt{(-3996^2 + (8830)^2} = 9692.106$$

$$GAIN\ FACTOR = \left(\frac{ADMITTANCE}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

$$GAIN\ FACTOR = \left(\frac{\frac{1}{200\ \text{k}\Omega}}{9692.106}\right) = 515.819\text{E} - 12$$

## IMPEDANCE CALCULATION USING GAIN FACTOR

The next example illustrates how the calculated gain factor derived previously is used to measure an unknown impedance. For this example, assume that the unknown impedance = 510 kΩ.

After measuring the unknown impedance at a frequency of 30 kHz, assume that the real and imaginary registers contain the following data:

Real register: = 0AEB hex = −1473 decimal
Imaginary register: = 0DB3 hex = 3507 decimal

$$Magnitude = \sqrt{((-1473)^2 + (3507)^2)} = 3802.863$$

Then the measured impedance at the frequency point is given by

$$Impedance = \frac{1}{GAIN\ \ FACTOR\ \times Magnitude}$$

$$= \frac{1}{515.819273\ \ \text{E} - 12 \times 3802.863}\ \Omega$$

$$= 509.791\ \ \text{k}\Omega$$

## GAIN FACTOR VARIATION WITH FREQUENCY

Because the AD5934 has a finite frequency response, the gain factor also shows a variation with frequency. This results in an error in the impedance calculation over a frequency range. Figure 18 shows an impedance profile based on a single-point gain factor calculation. To minimize this error, the frequency sweep should be limited to as small a frequency range as possible.

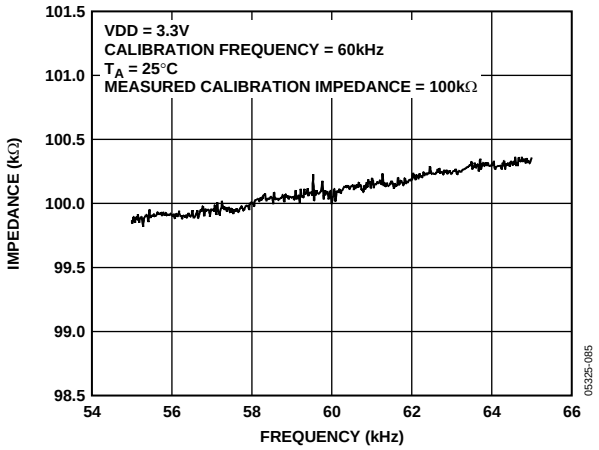


*Figure 18. Impedance Profile Using a Single-Point Gain Factor Calculation*

## TWO-POINT CALIBRATION

Alternatively it is possible to minimize this error by assuming that the frequency variation is linear and adjusting the gain factor with a 2-point calibration. Figure 19 shows an impedance profile based on a 2-point GAIN FACTOR calculation.

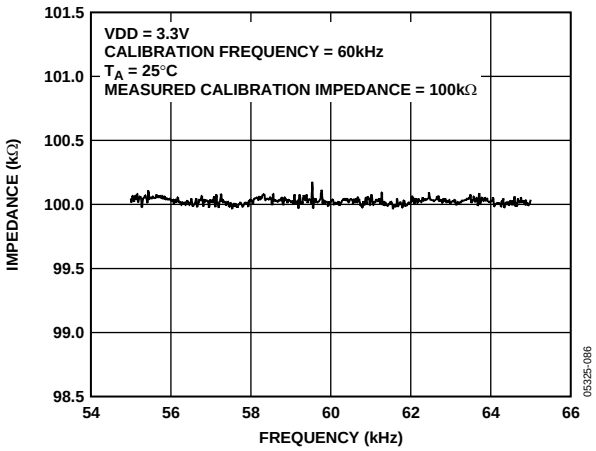


*Figure 19. Impedance Profile Using a 2-Point Gain Factor Calculation*

## TWO-POINT GAIN FACTOR CALCULATION

This is an example of a 2-point GAIN FACTOR calculation assuming the following:

Output excitation voltage = 2 V (p-p)
Calibration impedance value, $Z_{UNKNOWN}$ = 100.0 kΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current to voltage amplifier gain resistor = 100 kΩ
Calibration frequencies at = 55 kHz and 65 kHz

Typical values of the GAIN FACTOR calculated at the two calibration frequencies read

Gain factor calculated at 55 kHz = 1.031224E-09
Gain factor calculated at 65 kHz = 1.035682E-09
Difference in gain factor (ΔGF) = 1.035682E-09 – 1.031224E-09 = 4.458000E-12
Frequency span of sweep (ΔF) = 10 kHz

Therefore the GAIN FACTOR required at 60 kHz is given by

$$\left(\frac{4.458000E-12}{10\,kHz}\times 5\,kHz\right)+1.031224E-09$$

Required gain factor = 1.033453E-9

The impedance is calculated as previously described in the Impedance Calculation section.

## GAIN FACTOR SETUP CONFIGURATION

When calculating the GAIN FACTOR, it is important that the receive stage is operating in its linear region. This requires careful selection of the excitation signal range, current-to-voltage gain resistor and PGA gain. The gain through the system shown in Figure 20 is given by

$$Output\ Excitation\ Voltage\ Range\times\frac{Gain\ Setting\ Resistor}{Z_{UNKNOWN}}\times PGA\ Gain$$

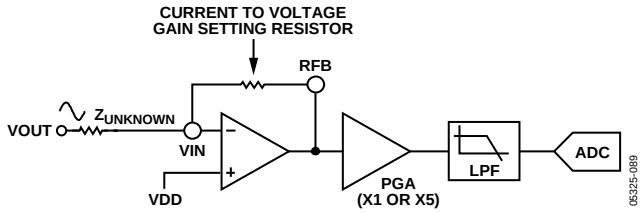


*Figure 20. AD5934 System Voltage Gain*

For this example, assume the following system settings:

VDD = 3.3 V
Gain setting resistor = 200 kΩ
$Z_{UNKNOWN}$ = 200 kΩ
PGA setting = ×1

The peak-to-peak voltage presented to the ADC input is 2 V p-p. However had the user chosen a PGA gain of ×5, the voltage would saturate the ADC.

## GAIN FACTOR RECALCULATION

The GAIN FACTOR must be recalculated for a change in any of the following parameters:

- Current-to-voltage gain setting resistor
- Output excitation voltage
- PGA gain

## GAIN FACTOR TEMPERATURE VARIATION

The typical impedance error variation with temperature is in the order of 30 ppm/°C. Figure 21 shows an impedance profile with a variation in temperature for 100 kΩ impedance using a 2-point gain factor calibration.

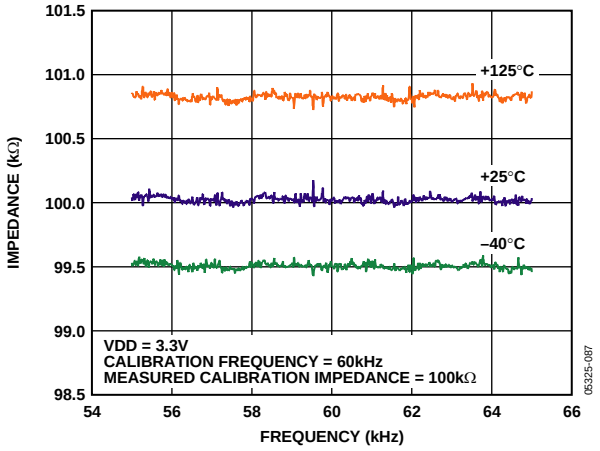


*Figure 21. Impedance Profile Variation with Temperature Using a 2-Point Gain Factor Calculation*

## IMPEDANCE ERROR

Minimizing the impedance range under test optimizes the AD5934 measurement performance. Below are examples of the AD5934 performance when operating in the six different impedance ranges. The gain factor is calculated with a precision resistor in each case.

### *Range 1 (0.1 kΩ to 1 kΩ)*

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 100 Ω
PGA gain = ×1
Supply voltage = 3.3 V
Current-to-voltage amplifier gain resistor = 100 Ω

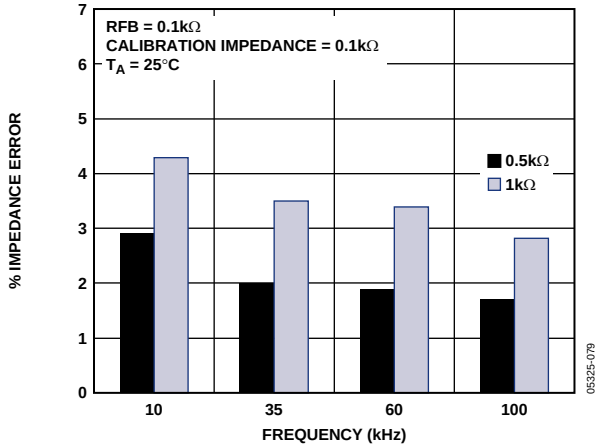


*Figure 22. Range 1: Typical % Impedance Error over Frequency*

### *Range 2 (1 kΩ to 10 kΩ)*

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 1 kΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current-to-voltage amplifier gain resistor = 1 kΩ

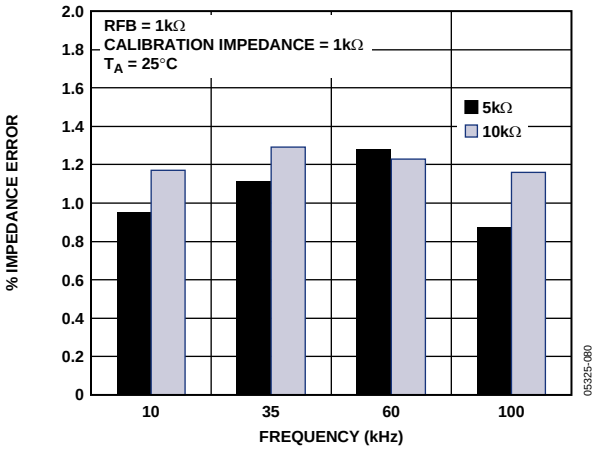


*Figure 23. Range 2: Typical % Impedance Error over Frequency*

### *Range 3 (10 kΩ to 100 kΩ)*

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 10 kΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current-to-voltage amplifier gain resistor = 10 kΩ

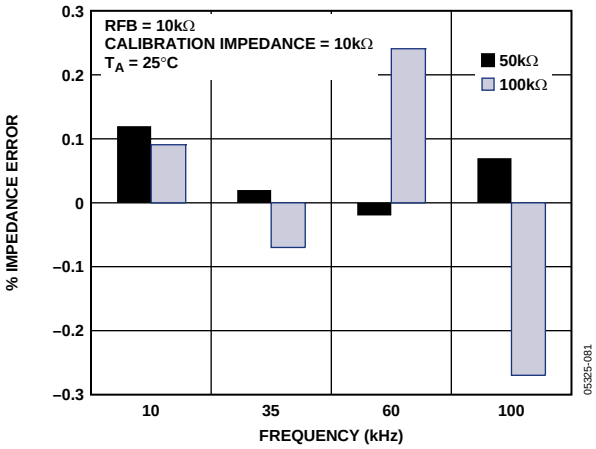


*Figure 24. Range 3: Typical % Impedance Error over Frequency*

### Range 4 (100 kΩ to 1 MΩ)

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 100 kΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current-to-voltage amplifier gain resistor = 100 kΩ

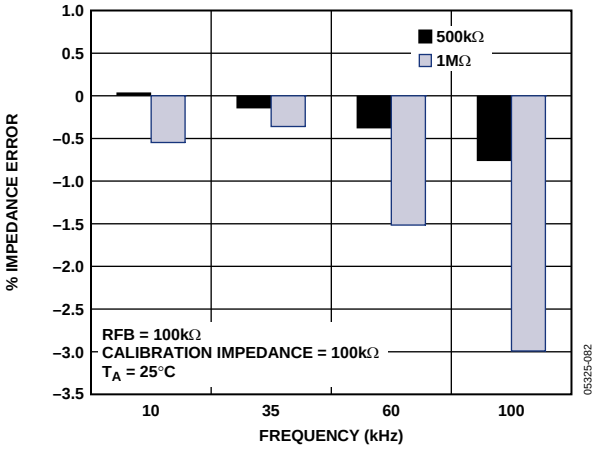


*Figure 25. Range 4: Typical % Impedance Error over Frequency*

### Range 5 (1 MΩ to 2 MΩ)

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 100 kΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current to voltage amplifier gain resistor = 100 kΩ

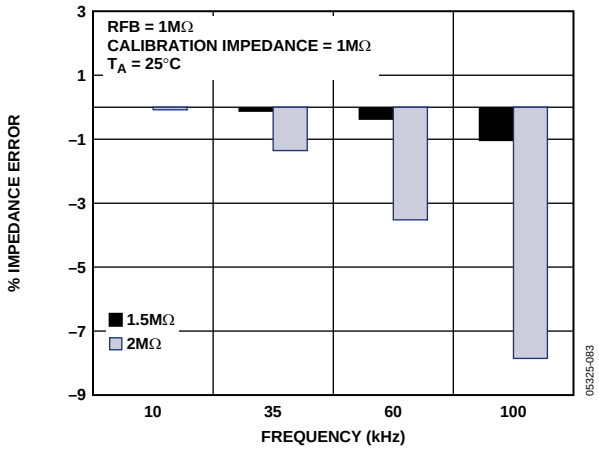


*Figure 26. Range 5: Typical % Impedance Error over Frequency*

### Range 6 (9 MΩ to 10 MΩ)

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 9 MΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current to voltage amplifier gain resistor = 9 MΩ

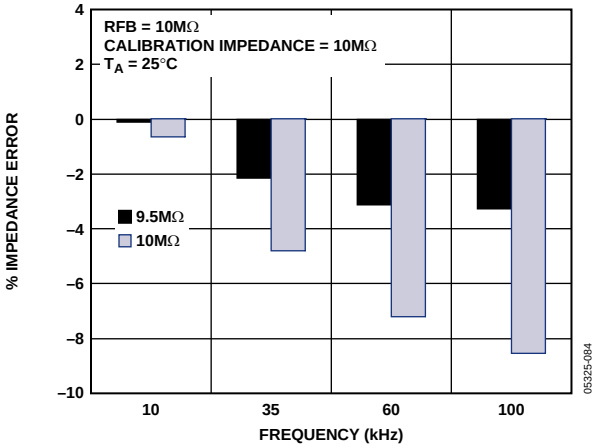


*Figure 27. Range 6: Typical % Impedance Error over Frequency*

# PERFORMING A FREQUENCY SWEEP

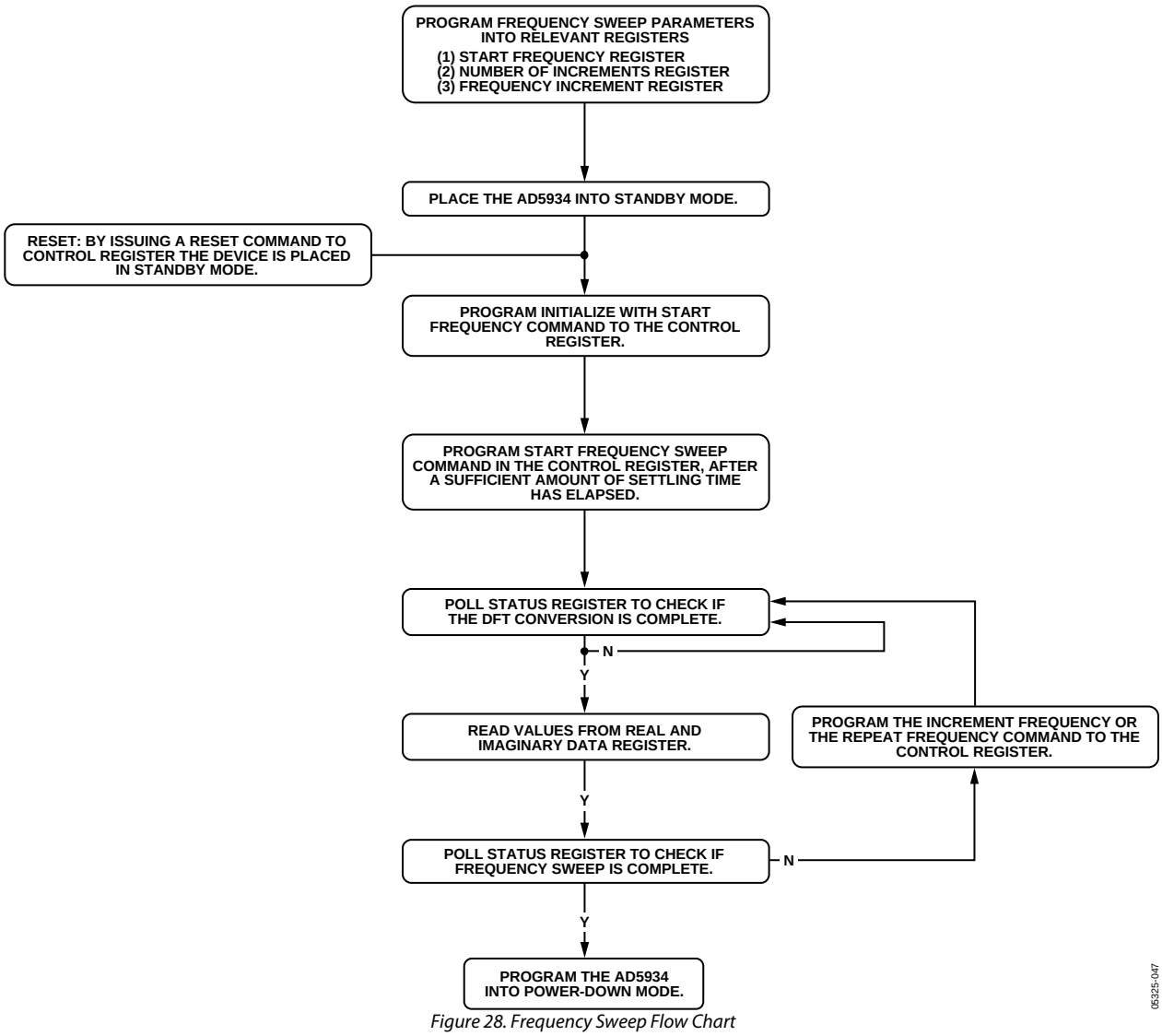


*Figure 28. Frequency Sweep Flow Chart*

# REGISTER MAP

**Table 7.**

| Register Name | Register Address | Register Data | Read/Write Register |
|---|---|---|---|
| CONTROL | 80 h | D15 to D8 | Read/Write |
| | 81 h | D7 to D0 | Read/Write |
| START FREQUENCY | 82 h | D23 to D16 | Read/Write |
| | 83 h | D15 to D8 | Read/Write |
| | 84 h | D7 to D0 | Read/Write |
| FREQUENCY INCREMENT | 85 h | D23 to D16 | Read/Write |
| | 86 h | D15 to D8 | Read/Write |
| | 87 h | D7 to D0 | Read/Write |
| NUMBER OF INCREMENTS | 88 h | D15 to D8 | Read/Write |
| | 89 h | D7 to D0 | Read/Write |
| NUMBER OF SETTLING TIME CYCLES | 8A h | D15 to D8 | Read/Write |
| | 8B h | D7 to D0 | Read/Write |
| STATUS | 8F h | D7 to D0 | Read Only |
| REAL DATA | 94 h | D15 to D8 | Read Only |
| | 95 h | D7 to D0 | Read Only |
| IMAGINARY DATA | 96 h | D15 to D8 | Read Only |
| | 97 h | D7 to D0 | Read Only |

## CONTROL REGISTER

**Table 8. 16-Bit Register**

| | | |
|---|---|---|
| 80 h | D15 to D8 | Read or Write |
| 81 h | D7 to D0 | Read or Write |

The CONTROL register is a 16-bit register that sets the AD5934 control modes. The 4 MSBs of the CONTROL register are decoded to provide control functions, such as performing a frequency sweep, powering down the part, and various other control functions defined in the CONTROL register map.

The user may choose to write only to Register Location 80 h and not to alter the contents of 81 h. Note that the CONTROL register should not be written to as part of a Block Write command. The CONTROL register also allows the user to program the excitation voltage and set the system clock. A Reset command to the CONTROL register does not reset any programmed values associated with the sweep (that is, Start frequency, number of increments, frequency increment). After a Reset command, an Initialize with Start Frequency command must be issued to the CONTROL register to restart the frequency sweep sequence (see Figure 28).

Default value upon reset: D15 to D0 reset to A0 00H upon power-up. The AD5934 contains a 16-bit control register (Address 80h and 81h) that sets the AD5934 control modes.

**Table 9. Control Register Map**

| Bit | D15 | D14 | D13 | D12 | |
|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | No operation |
| | 0 | 0 | 0 | 1 | Initialize with Start Frequency |
| | 0 | 0 | 1 | 0 | Start Frequency Sweep |
| | 0 | 0 | 1 | 1 | Increment Frequency |
| | 0 | 1 | 0 | 0 | Repeat Frequency |
| | 1 | 0 | 0 | 0 | No operation |
| | 1 | 0 | 0 | 1 | No operation |
| | 1 | 0 | 1 | 0 | Power down mode |
| | 1 | 0 | 1 | 1 | Standby mode |
| | 1 | 1 | 0 | 0 | No operation |
| | 1 | 1 | 0 | 1 | No operation |
| D11 | | | | | No operation |
| | | D10 | D9 | | Output voltage range |
| | | 0 | 0 | | Range 1 ( 2.0 V p-p typ) |
| | | 0 | 1 | | Range 3 (200 mV p-p typ) |
| | | 1 | 0 | | Range 4 (400 mV p-p typ) |
| | | 1 | 1 | | Range 2 (1.0 V p-p typ) |
| D8 | | | | | PGA gain 0 = ×5, 1 = ×1 |
| D7 | | | | | Reserved. Set to 0. |
| D6 | | | | | Reserved. Set to 0. |
| D5 | | | | | Reserved. Set to 0. |
| D4 | | | | | Reset |
| D3 | | 1 | | | External System clock. Must be set to 1. |
| D2 | | 0 | | | Must be Set to 0. |
| D1 | | | | | Reserved. Set to 0. |
| D0 | | | | | Reserved. Set to 0. |

### *CONTROL Register Decode*

**Initialize with Start Frequency**
This command enables the DDS to output the programmed start frequency for an indefinite time. It is used is to excite the unknown impedance initially. When the output unknown impedance has settled after a time determined by the user, the user must initiate a Start Frequency Sweep command to begin the frequency sweep.

**Start Frequency Sweep**
In this mode the ADC starts measuring after the programmed number of settling time cycles has elapsed. The user has the ability to program an integer number of output frequency cycles (settling time cycles) to Register 8A h and Register 8B h before the commencement of the measurement at each frequency point. See Figure 28.

**Increment Frequency**
The Increment Frequency command is used to step to the next frequency point in the sweep. This usually happens after data from the previous step has been transferred and verified by the DSP. When the AD5934 receives this command, it waits for the programmed number of settling time cycles before beginning the ADC conversion process.

**Repeat Frequency**
There is the facility to repeat the current frequency point measurement by issuing a Repeat Frequency command to the CONTROL register. This has the benefit of allowing the user to average successive readings.

**Power-Down**
The default state on power-up of the AD5934 is power-down mode. The CONTROL register contains the code 1010000000000000 (A000h). In this mode both the output and input VOUT and VIN pins are connected internally to GND.

**Standby Mode**
Powers up the part for general operation; in standby mode the VIN and VOUT pins are internally connected to ground.

**Reset**
A Reset command allows the user to interrupt a sweep. The START FREQUENCY, NUMBER OF INCREMENTS, and FREQUENCY INCREMENT register contents are not overwritten. An Initialize with Start Frequency command is required to restart the Frequency Sweep command sequence.

**Output Voltage Range**
This allows the user to program the excitation voltage range at VOUT.

**PGA Gain**
This allows the user to amplify the response signal into the ADC by a multiplication factor of ×5 or ×1.

## START FREQUENCY REGISTER

**Table 10. 24-Bit Register**

| | | |
|---|---|---|
| 82 h | D23 to D16 | Read or Write |
| 83 h | D15 to D8 | Read or Write |
| 84 h | D7 to D0 | Read or Write |

The START FREQUENCY register contains the 24-bit digital representation of the frequency from where the subsequent frequency sweep is initiated. For example, if the user requires the sweep to start from frequency 30 kHz (using a 16.00 MHz clock), then the user programs 3D hex to Register Location 82 h, 70 hex to Register Location 83h, and A3 hex to Register Location 84 h. This ensures the output frequency starts at 30 kHz.

The code to be programmed to the START FREQUENCY register is

$$Start\ Frequency\ Code = \left( \frac{30\ \text{kHz}}{\left( \frac{16\ \text{MHz}}{16} \right)} \right) \times 2^{27} \equiv \text{3D70A3 hexidecimal}$$

Default value upon reset: D23 to D0 are not reset on power-up. After a Reset command the contents of this register are not reset.

## FREQUENCY INCREMENT REGISTER

**Table 11.**

| | | |
|---|---|---|
| 85 h | D23 to D16 | Read or Write |
| 86 h | D15 to D8 | Read or Write |
| 87 h | D7 to D0 | Read or Write |

The FREQUENCY INCREMENT register contains a 24-bit representation of the frequency increment between consecutive frequency points along the sweep. For example, if the user requires an increment step of 30 Hz using a 16.0 MHz clock, the user should program 00 hex to Register Location 85 h, 0F hex to Register Location 86 h and BA hex to Register Location 87 h.

The formula for calculating the increment frequency is given by

$$Frequency\ Increment\ Code = \left( \frac{10\ \text{Hz}}{\left( \frac{16\ \text{MHz}}{16} \right)} \right) \times 2^{27} \equiv \text{00053E hexidecimal}$$

The user programs 00 hex to Register 85 h, 05 hex to Register 86 h, and 3E hex to Register 87 h.

Default value upon reset: D23 to D0 are not reset on power-up. After a Reset command, the contents of this register are not reset.

## NUMBER OF INCREMENTS REGISTER

**Table 12. 16-Bit Register**

| | | | | |
|---|---|---|---|---|
| Bits D15 to D9 = Don't care | 88 h | D15 to D8 | Read or Write | Integer number stored in binary format |
| Bits D8 to D0 = Number of frequency increments | 89 h | D7 to D0 | Read or Write | |

This register determines the number of frequency points in the frequency sweep. The number of points is represented by a 9-bit word, D8 to D0. D9 to D15 are don't care bits. This register in conjunction with the START FREQUENCY register and the INCREMENT FREQUENCY registers determine the frequency sweep range for the sweep operation. The maximum number of increments which can be programmed is 511.

Default value upon reset: D8 to D0 are not reset on power-up. After a Reset command, the contents of this register are not reset.

## NUMBER OF SETTLING TIME CYCLES REGISTER

**Table 13. 16-Bit Register**

| | | | | |
|---|---|---|---|---|
| D15 to D11 = Don't Care<br>D10 to D9 = 2-Bit Decode<br>D8 = MSB Number of Settling Time Cycles<br>D10 D9<br>0 0 Default<br>0 1 Number Cycles × 2<br>1 0 Reserved<br>1 1 Number Cycles × 4 | 8A h | D15 to D8 | Read or Write | Integer number stored in binary format |
| Number of Settling Time Cycles | 8B h | D7 to D0 | Read or Write | |

This register determines the number of output excitation cycles that are allowed to pass through the unknown impedance, after receipt of a Start, Increment, or Repeat Frequency command, before the ADC is triggered to perform a conversion of the response signal. The SETTLING TIME CYCLES register value determines the delay between a Frequency Start/Increment/Repeat command and the time an ADC conversion commences. The number of cycles is represented by a 9-bit word, D8 to D0. The value programmed into the SETTLING TIME CYCLES register can be increased by a factor of 2 or 4 depending upon the status of bits D10 to D9. The 5 most significant bits, D15 to D11, are don't care bits. The maximum number of output cycles that can be programmed is 511 × 4 = 2044 cycles. For example, consider an excitation signal of 30 kHz. The maximum delay between the programming of this frequency and the time that this signal is first sampled by the ADC is ≈ 511 × 4 × 33.33 μs = 68.126 ms. The ADC takes 1024 samples, and the result is stored as real and imaginary data in Register 94 h to Register 97 h. The conversion process takes approximately 1 ms using a 16.777 MHz clock.

Default value upon reset: D10 to D0 are not reset on power-up. After a Reset command, the contents of this register are not reset.

## STATUS REGISTER

**Table 14. 8-Bit Register**

| | | | |
|---|---|---|---|
| 8F h | D7 to D0 | Read Only | Bits |

The STATUS register is used to confirm that particular measurement tests have been successfully completed. Each of the bits from D7 to D0 indicates the status of specific functionality of the AD5934.

D0, and Bit D4 to Bit D7 are treated as don't care bits, these bits do not indicate the status of any measurement

The status of bit D1 indicates the status of a frequency point impedance measurement. This bit is set when the AD5934 has completed the current frequency point impedance measurement. This indicates that there is valid real and imaginary data in Register 93 h to Register 97 h. This bit is reset on receipt of a Start, Increment, Repeat Frequency, or Reset command. This bit is also reset on power-up.

The status of bit D2 indicates the status of the programmed frequency sweep. This bit is set when all programmed increments to the NUMBER of INCREMENTS register are complete. This bit is reset on power-up and on receipt of a Reset command.

**Table 15. STATUS Register**

| STATUS Register Address | Control Word | Function |
|---|---|---|
| 8F h | 0000 0001 | Reserved |
| 8F h | 0000 0010 | Valid real/imaginary data |
| 8F h | 0000 0100 | Frequency sweep complete |
| 8F h | 0000 1000 | Reserved |
| 8F h | 0001 0000 | Reserved |
| 8F h | 0010 0000 | Reserved |
| 8F h | 0100 0000 | Reserved |
| 8F h | 1000 0000 | Reserved |

### *Valid Real/Imaginary Data*

Set when data processing for the current frequency point is finished, indicating real/imaginary data available for reading. Reset when a DDS Start/Increment/Repeat command is issued. Also this bit is reset to 0 when a Reset command is issued to the CONTROL register.

### *Frequency Sweep Complete*

Set when data processing for the last frequency point in the sweep is complete. Reset when a Start Frequency Sweep command is issued to the CONTROL register. This bit is also reset when a Reset command is issued to the CONTROL register.

## REAL AND IMAGINARY DATA REGISTERS (16 BITS)

**Table 16. Real Data**

| | | | |
|---|---|---|---|
| 94 h | D15 to D8 | Read Only | Twos complement data |
| 95 h | D7 to D0 | Read Only | |

**Table 17. Imaginary Data**

| | | | |
|---|---|---|---|
| 96 h | D15 to D8 | Read Only | Twos complement data |
| 97 h | D7 to D0 | Read Only | |

These registers contain a digital representation of the real and imaginary components of the impedance measured for the current frequency point. The values are stored in 16-bit, twos complement format. To convert this number to an actual impedance value, the magnitude— $\sqrt{(Real^2 \text{ and } Imaginary^2)}$ — must be multiplied by an admittance/code number (called a gain factor) to give the admittance, and the result inverted to give impedance. The gain factor varies for each ac excitation voltage/gain combination.

Default value upon reset: These registers are not reset on power-up or on receipt of a Reset command. Note that the data in these registers is only valid if Bit D1 in the STATUS register is set, indicating that the processing at the current frequency point is complete.

# SERIAL BUS INTERFACE

Control of the AD5934 is carried out via the $1^2C$-compliant serial interface protocol. The AD5934 is connected to this bus as a slave device under the control of a master device. The AD5934 has a 7-bit serial bus slave address. When the device is powered up, it has a default serial bus address, 0001101 (0D hex)

## GENERAL $I^2C$ TIMING

The general $I^2C$ protocol operates as described in this section. Figure 29 shows the timing diagram for general read and write operations using the $I^2C$-compliant interface.

The master initiates data transfer by establishing a start condition, defined as a high to low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The slave responds to the start condition and shifts in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus an R/W bit, which determines the direction of the data transfer—that is, whether data is written to or read from the slave device (0 = write, 1 = read).

The slave responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0, then the master writes to the slave device. If the R/W bit is 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses, 8 bits of data followed by an acknowledge bit, which can be from the master or slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written. Because data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before performing a read operation, it is sometimes necessary to perform a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge (NACK). The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

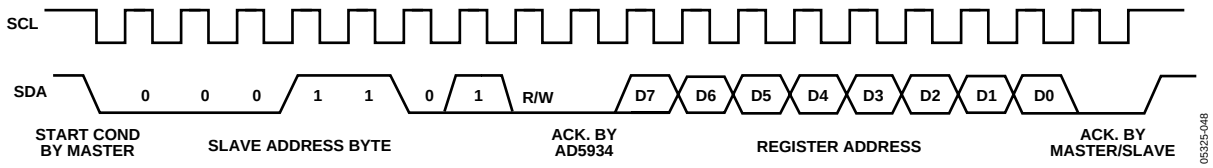


*Figure 29.*

## WRITING/READING TO THE AD5934

The interface specification defines several different protocols for different types of read and write operations. This section describes the protocols used in the AD5934. The figures in this section use the following abbreviations:

S Start
P Stop
R Read
W Write
A Acknowledge
$\overline{A}$ No acknowledge write byte/command byte

### *User Command Codes*

The command codes in Table 18 are used for reading/writing to the interface. They are further explained in this section, but are grouped here for easy reference.

**Table 18.**

| Command Code | Code Name | Code Description |
|---|---|---|
| 1010 0000 | Block Write | This command is used when writing multiple bytes to the RAM. See the Block Write section. |
| 1010 0001 | Block Read | This command is used when reading multiple bytes from RAM/memory. See the Block Read section. |
| 1011 0000 | Address Pointer | This command enables the user to set the address pointer to any location in the memory. The data contains the address of the register where the pointer should be pointing. |

### *Write Byte/Command Byte*

In this operation the master device sends a byte of data to the slave device. The write byte can either be a data byte write to a RAM location or can be a command operation. To write data to a register the command sequence is as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a register address.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.


*Figure 30. Writing Register Data to Register Address*

In the AD5934, the write byte protocol is also used to set a pointer to a register location. This is used for a subsequent single-byte read from the same address or block read or write starting at that address.

To set a register pointer, the following sequence is applied:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a pointer command code (see Table 18, a pointer command = 1011 0000).
5. The slave asserts ACK on SDA.
6. The master sends a data byte (a register location where pointer is to point).
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA to end the transaction.


*Figure 31. Setting Pointer to Register Address*

## BLOCK WRITE

In this operation, the master device writes a block of data to a slave device. The start address for a block write must previously have been set. In the case of the AD5934 this is done by setting a pointer to set the register address.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends an 8-bit command code (1010 0000) that tells the slave device to expect a block write.
5. The slave asserts ACK on SDA.
6. The master sends a data byte that tells the slave device the number of data bytes to be sent to it.
7. The slave asserts ACK on SDA.
8. The master sends the data bytes.
9. The slave asserts ACK on SDA after each data byte.
10. The master asserts a stop condition on SDA to end the transaction.

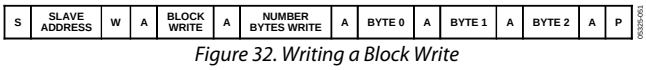


*Figure 32. Writing a Block Write*

## AD5934 READ OPERATIONS

The AD5934 uses the following I²C read protocols:

### *Receive Byte*

In the AD5934, the receive byte protocol is used to read a single byte of data from a register location whose address has previously been set by setting the address pointer.

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NACK on SDA (slave needs to check that master has received data).
6. The master asserts a stop condition on SDA and the transaction ends.

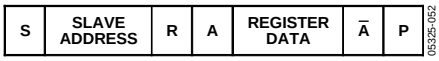


*Figure 33. Reading Register Data*

### *Block Read*

In this operation, the master device reads a block of data from a slave device. The start address for a block read must previously have been set by setting a pointer.

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code (1010 0001) that tells the slave device to expect a block read.
5. The slave asserts ACK on SDA.
6. The master sends a byte count data byte that tells the slave how many data bytes to expect.
7. The slave asserts ACK on SDA.
8. The master asserts a repeat start condition on SDA. This is required to set the read bit high.
9. The master sends the 7-bit slave address followed by the read bit (high).
10. The slave asserts ACK on SDA.
11. The master receives the data bytes.
12. The master asserts ACK on SDA after each data byte.
13. A NACK is generated after the last byte to signal the end of the read.
14. The master asserts a stop condition on SDA to end the transaction.

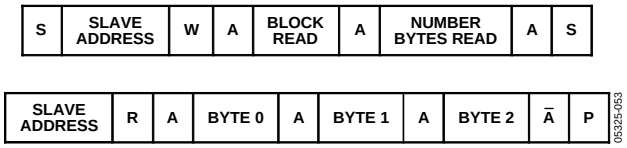


*Figure 34. Performing a Block Read*

# TYPICAL APPLICATIONS

This section describes typical applications for the AD5934.

## BIOMEDICAL: NONINVASIVE BLOOD IMPEDANCE MEASUREMENT

When a known strain of a virus is added to a blood sample that already contains a virus, a chemical reaction takes place whereby the impedance of the blood under certain conditions changes. By characterizing this effect across different frequencies it is possible to detect a specific strain of virus. For example, a strain of the disease exhibits a certain characteristic impedance at one frequency but not at another, therefore the requirement to sweep different frequencies to check for different viruses. The AD5934, with its 27-bit phase accumulator, allows for sub-Hz frequency tuning.

The AD5934 can be used to inject a stimulus signal through the blood sample via a probe. The response signal is analyzed and the effective impedance of the blood is tabulated. The AD5934 is ideal for this application because it allows the user to tune to the specific frequency required for each test.

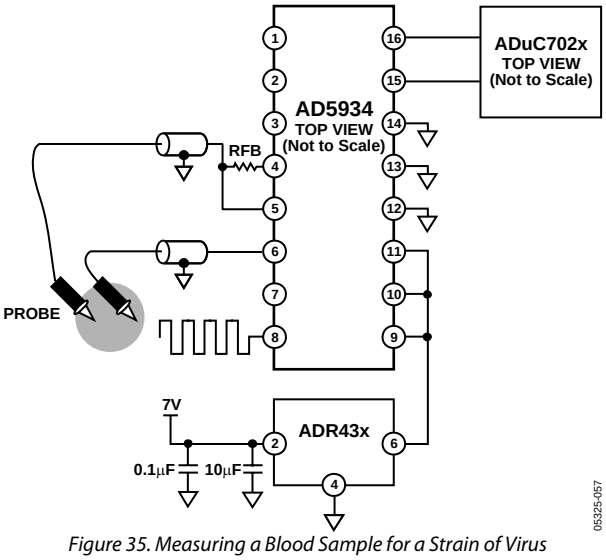


*Figure 35. Measuring a Blood Sample for a Strain of Virus*

## SENSOR/COMPLEX IMPEDANCE MEASUREMENT

The operational principle of a capacitive proximity sensor is based on the change of a capacitance in a RLC resonant circuit. This leads to changes in the resonant frequency of the RLC circuit, which can be evaluated as shown Figure 36.

It is first required to tune the RLC circuit to the area of resonance. At the resonant frequency, the impedance of the RLC circuit is at a maximum. Therefore, a programmable frequency sweep and tuning capability is required, which is provided by the AD5934.

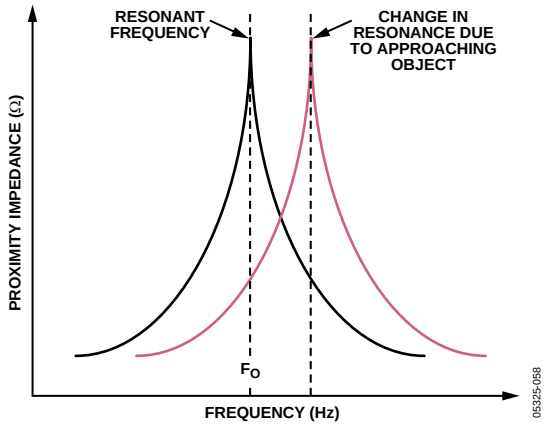


*Figure 36. Detecting a Change in Resonant Frequency*

An example of the use of this type of sensor is for a train proximity measurement system. The magnetic fields of the train approaching on the track change the resonant frequency to an extent that can be characterized. This information can be sent back to a mainframe system to show the train location on the network.

Another application for the AD5934 is in parked vehicle detection. The AD5934 is placed in an embedded unit connected to a coil of wire underneath the parking location. The AD5934 outputs a single frequency within the 80 kHz to 100 kHz frequency range, depending upon the wire composition. The wire can be modeled as a resonant circuit. The coil is calibrated with a known impedance value and at a known frequency. The impedance of the loop is monitored constantly. If a car is parked over the coil, the impedance of the coil changes and the AD5934 detects the presence of the car.

## ELECTRO-IMPEDANCE SPECTROSCOPY

The AD5934 has found use in the area of corrosion monitoring. Corrosion in a metal such as aluminum, which is used in air craft and ships, requires continuous assessment because the metal is exposed to a wide variety of conditions such as temperature and moisture. The AD5934 offers an accurate and compact solution for this type of measurement compared to the large and expensive existing units on the market.

Mathematically the corrosion of a metal is modeled using a RC network which consists of a resistance,Rs, in series with a parallel resistor and capacitor, Rp and Cp. A system metal would typically have values as follows: Rs 10 Ω to 10 kΩ, Rp 1 kΩ to 1 MΩ, and Cp 5 μf to 70 μf.

The frequency range of interest when monitoring corrosion is 0.1 Hz to 100 kHz.

To ensure that the measurement itself does not introduce a corrosive effect, the metal needs to be excited with minimal voltage, typically in the 200 mV region which the AD5934 is capable of outputting. A nearby processor or control unit like the ADuc702x would log a single impedance sweep from 0.1 kHz to 100 kHz every 10 minutes and download the results back to a control unit. In order to achieve system accuracy from the 0.1 kHz to 1 kHz region, the system clock needs to be scaled down from the 16.776 MHz nominal clock frequency to 500 kHz, typically. The clock scaling can be achieved digitally using an external direct digital synthesizer like the AD9834 as a programmable divider, which supplies a clock signal to MCLK and which can be controlled digitally by the nearby microprocessor.

# CHOOSING A REFERENCE FOR THE AD5934

To achieve the best performance from the AD5934, thought should be given to the choice of a precision voltage reference. The AD5934 has three reference inputs: (AVDD1, AVDD2, and DVDD). It is recommended that the voltage on these reference inputs be run from the same voltage supply.

There are four possible sources of error that should be considered when choosing a voltage reference for high accuracy applications: initial accuracy, ppm drift, long-term drift, and output voltage noise. To minimize these errors, a reference with high initial accuracy is preferred. Also, choosing a reference with an output trim adjustment, such as a device in the ADR43X family, allows a system designer to trim system errors by setting a reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Because the supply current required by the AD5934 is extremely low, the parts are ideal for low supply applications. The ADR395 voltage reference is recommended in this case. This requires less than 100 μA of quiescent current. It also provides very good noise performance at 8 μV p-p in the 0.1 Hz to 10 Hz range.

Long-term drift is a measure of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains stable during its entire lifetime. A reference with a tight temperature coefficient specification should be chosen to reduce temperature dependence of the system output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference with as low an output noise voltage as practical for the system noise resolution required is important. Precision voltage references such as the ADR433 produce low output noise in the 0.1 Hz to 10 Hz region. Examples of some recommended precision references for use as supply to the AD5934 are shown in Table 19.

**Table 19. List of Precision References for theAD5934**

| Part No. | Initial Accuracy (mV max) | Output Voltage (V) | Temp. Drift (ppm/°C max) | 0.1 Hz to 10 Hz Noise (μV p-p typ) |
|---|---|---|---|---|
| ADR433B | ±1.4 | 3. 0 | 3 | 3.75 |
| ADR433A | ±4.0 | 3. 0 | 10 | 3.75 |
| ADR434B | ±1.5 | 4. 096 | 3 | 6.25 |
| ADR434A | ±5 | 4. 096 | 10 | 6.25 |
| ADR435B | ±2 | 5.0 | 3 | 8 |
| ADR435A | ±6 | 5.0 | 10 | 8 |
| ADR439B | ±2 | 4.5 | 3 | 7.5 |
| ADR439A | ±5.4 | 4.5 | 10 | 7.5 |

# LAYOUT AND CONFIGURATION

## POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5934 should have separate analog and digital sections, each having its own area of the board. If the AD5934 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5934.

The power supply to the AD5934 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitor has low effective series resistance (ESR) and effective series inductance (ESI); common ceramic types of capacitors are suitable. The 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

# OUTLINE DIMENSIONS

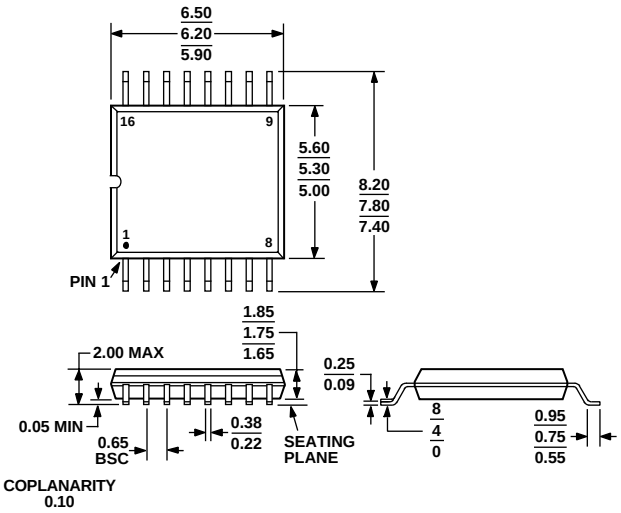


*Figure 37. 16-Lead Shrink Small Outline Package [SSOP]*
*(RS-16)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD5934YRSZ[1] | −40°C to +125°C | 16-Lead Shrink Small Outline Package (SSOP) | RS-16 |
| AD5934YRSZ-REEL7[1] | −40°C to +125°C | 16-Lead Shrink Small Outline Package (SSOP) | RS-16 |
| EVAL-AD5934EB | −40°C to +125°C | Evaluation Board | |

[1] Z = Pb-free part.

## NOTES

# NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.


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