DataSheet

AS1156/AS1154
Single/Dual LVDS Driver

1 General Description

The AS1156/AS1154 is a Single/Dual Flow-Through LVDS (Low-Voltage Differential Signaling) Line Driver which accepts and converts LVTTL/LVCMOS input levels into LVDS output signals. The device is perfect for low-power low-noise applications requiring high signaling rates and reduced EMI emissions.

The device is guaranteed to transmit data at speeds up to 800Mbps (400MHz) over controlled impedance media of approximately 100Ω. Supported transmission media are PCB traces, backplanes, and cables.

The AS1156 is a single LVDS transmitter, and the AS1154 is a dual LVDS transmitter.

Outputs conform to the *ANSI TIA/EIA-644 LVDS* standards. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVTTL/LVCMOS inputs and LVDS outputs.

The AS1156/AS1154 operates from a single +3.3V supply and is specified for operation from -40 to +85°C.

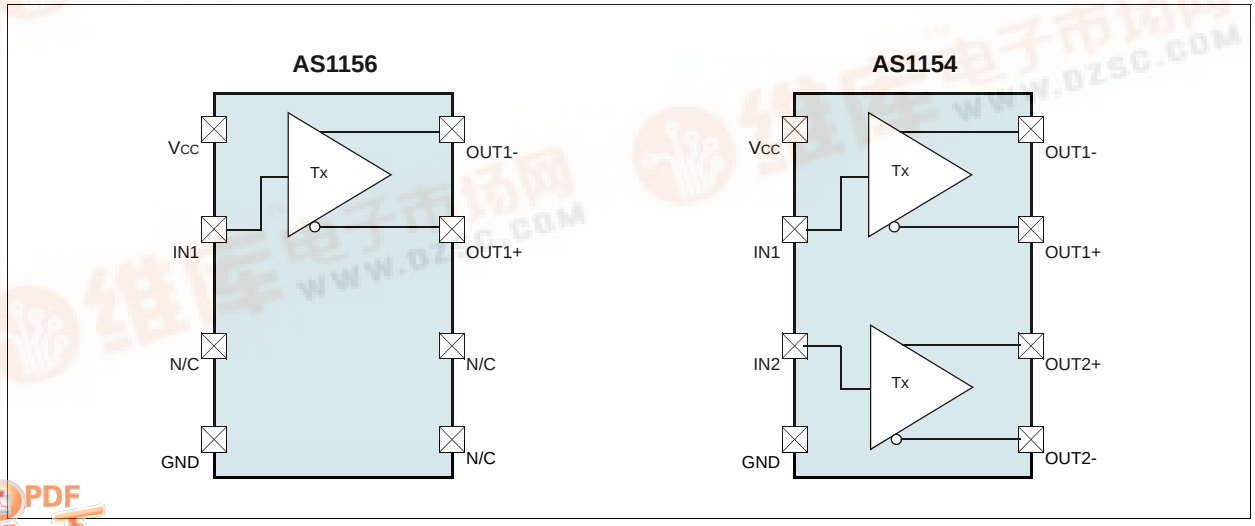
2 Key Features

- Flow-Through Pinout
- Guaranteed 800Mbps Data Rate
- 250ps Pulse Skew (Max)
- Conforms to *ANSI TIA/EIA-644* LVDS Standards
- Single +3.3V Supply
- Operating Temperature Range: -40 to +85°C
- 8-Pin SOIC Package

3 Applications

Digital Copiers, Laser Printers, Cellular Phone Base Stations, Add/Drop Muxes, Digital Cross-Connects, DSLAMs, Network Switches/Routers, Backplane Interconnect, Clock Distribution Computers, Intelligent Instruments, Controllers, Critical Microprocessors and Microcontrollers, Power Monitoring, and Portable/Battery-Powered Equipment.

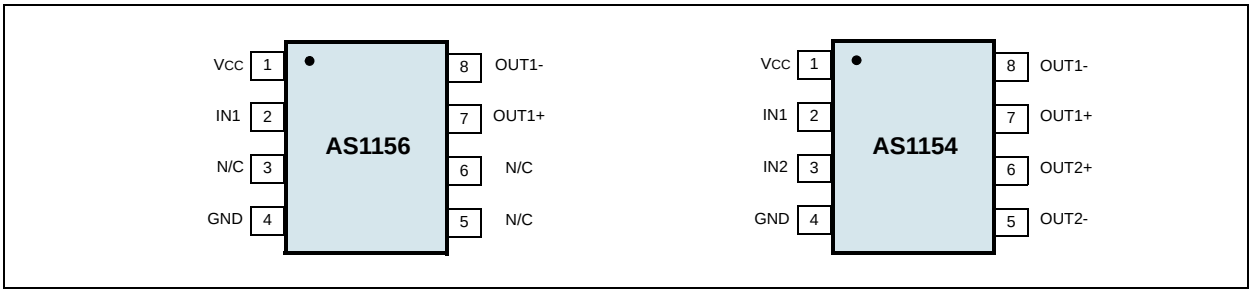
Figure 1. Block Diagram



4 Pinout and Packaging

Pin Assignments

Figure 2. AS1156/AS1154 Pin Assignments (Top View)



Pin Descriptions

Table 1. AS1156/AS1154 Pin Descriptions

Pin Number		Pin Name	Description
AS1154	AS1156		
1	1	Vcc	**Power Supply Input.** Bypass Vcc to GND with 0.1µF and 0.001µF ceramic capacitors.
2	2	IN1	**LVTTL/LVCMOS Driver Input**
3		IN2	**LVTTL/LVCMOS Driver Input**
4	4	GND	**Ground**
5		OUT2-	**Inverting LVDS Driver Output**
6		OUT2+	**Noninverting LVDS Driver Output**
7	7	OUT1+	**Noninverting LVDS Driver Output**
8	8	OUT1-	**Inverting LVDS Driver Output**
	3, 5, 6	N/C	**Not connected**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Limits	Units	Notes
V_{CC} to GND	-0.3 to +5.0	V	
IN*x*, EN, ENn to GND	-0.3 to (V_{CC} + 0.3)	V	
OUT*x*+, OUT*x*- to GND	-0.3 to +5	V	
Short Circuit Duration (OUT*x*+, OUT*x*-)	Continuous		
Continuous Power Dissipation (T_A = +70°C)	755	mW	Derate 9.4mW/°C Above +70°C
Storage Temperature Range	-65 to +150	ºC	
Maximum Junction Temperature	+150	ºC	
Operating Temperature Range	-40 to +85	ºC	
Package Body Temperature	260	ºC	The reflow peak soldering temperature (body temperature) specified is in compliance with *IPC/JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*.
ESD Protection	±4	kV	Human Body Model, IN*x*, OUT*x*+, OUT*x*--

6 Electrical Characteristics

DC Electrical Characteristics

(V_{CC} = +3.0 to +3.6V, T_A = -40 to +85°C , R_L = 100Ω ±1%
Typical values are at V_{CC} = +3.3V, T_A = +25°C, Unless Otherwise Noted.) [1]

Table 3. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVDS Output (OUT*x*+, OUT*x*-)						
Differential Output Voltage	V_{OD}	Figure 21 on page 11	250	355	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 21 on page 11		1	35	mV
Offset Voltage	V_{OS}	Figure 21 on page 11	1.125	1.25	1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 21 on page 11		4	25	mV
Output High Voltage	V_{OH}				1.6	V
Output Low Voltage	V_{OL}		0.90			V
Differential Output Short-Circuit Current [2]	I_{OSD}	V_{OD} = 0V			-9	mA
Output Short-Circuit Current	I_{OS}	OUT*x*+ = 0V at IN*x* = V_{CC} or OUT*x*- = 0V at IN*x* = 0V		-3.7	-9	mA
Power-Off Output Current	I_{OFF}	V_{CC} = 0V or open, OUT*x*+ = 0V or 3.6V OUT*x*- = 0V or 3.6V, R_L = ∞	-20		20	µA
Inputs (INx)						
High-Level Input Voltage	V_{IH}		2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}		GND		0.8	V
Input Current	I_{IN}	IN*x* = 0V or V_{CC}	-20		20	µA
Supply Current						
No-Load Supply Current	I_{CC}	R_L = ∞ , IN*x* = V_{CC} or 0V for all channels		2	3.5	mA
Loaded Supply Current	I_{CCL}	R_L = 100Ω, IN*x* = V_{CC} or 0V for all channels, AS1156		5.5	7.5	mA
		R_L = 100Ω, IN*x* = V_{CC} or 0V for all channels, AS1154		8.5	12	mA

Notes:

1. Currents into the device are positive, and current out of the device is negative. All voltages are referenced to ground except V_{OD}.
2. Guaranteed by correlation data.

Switching Characteristics

(V_{CC} = +3.0 to +3.6V, R_L = 100Ω ±1%, C_L = 2.5pF (differential), T_A = -40 to +85°C
Typical values are at V_{CC} = +3.3V, T_A = +25ºC, Unless Otherwise Noted.) [1, 2, 3, 10]

Table 4. Switching Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Propagation Delay, High-to-Low	t_{PHLD}	Figure 20 on page 11 and Figure 21 on page 11	1.1	1.268	1.5	ns
Differential Propagation Delay, Low-to-High	t_{PLHD}	Figure 20 on page 11 and Figure 21 on page 11	1.1	1.267	1.5	ns
Differential Pulse Skew [4]	t_{SKD1}	Figure 20 on page 11 and Figure 21 on page 11		90	200	ps
Differential Channel-to-Channel Skew [5]	t_{SKD2}	Figure 20 on page 11 and Figure 21 on page 11		110	250	ps
Differential Part-to-Part Skew [6]	t_{SKD3}	Figure 20 on page 11 and Figure 21 on page 11			750	ps
Differential Part-to-Part Skew [7]	t_{SKD4}	Figure 20 on page 11 and Figure 21 on page 11			900	ps
Rise Time	t_{TLH}	Figure 20 on page 11 and Figure 21 on page 11	200	356	800	ps
Fall Time	t_{THL}	Figure 20 on page 11 and Figure 21 on page 11	200	352	800	ps
Maximum Operating Frequency [8, 9]	f_{MAX}		400			MHz

Notes:

1. Parameters are guaranteed by design and characterization.
2. C_L includes probe and jig capacitance.
3. Signal generator conditions for dynamic tests: V_{OL} = 0, V_{OH} = 2.4V, f = 100MHz, 50% duty cycle, RO = 50Ω, $t_R \leq$ 1ns, $t_F \leq$ 1ns (0 to 100%).
4. t_{SKD1} is the magnitude difference of differential propagation delay. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.
5. t_{SKD2} is the magnitude difference of t_{PHLD} or t_{PLHD} of one channel to the t_{PHLD} or t_{PLHD} of another channel on the same device.
6. t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.
7. t_{SKD4} is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.
8. f_{MAX} signal generator conditions: V_{OL} = 0, V_{OH} = 2.4V, 50% duty cycle, RO = 50Ω, $t_R \leq$ 1ns, $t_F \leq$ 1ns (0 to 100%).
9. Transmitter output criteria: duty cycle = 45 to 55%, $V_{OD} \geq$ 250mV.
10. For optimum performance matched circuits should be used.

7 Typical Operating Characteristics

VCC = *+3.3V,* CLOAD = *2.5pF (differential), Freq = 20MHz,* Tamb = *+25ºC, unless otherwise noted*

Figure 3. Transition Time vs. VCC

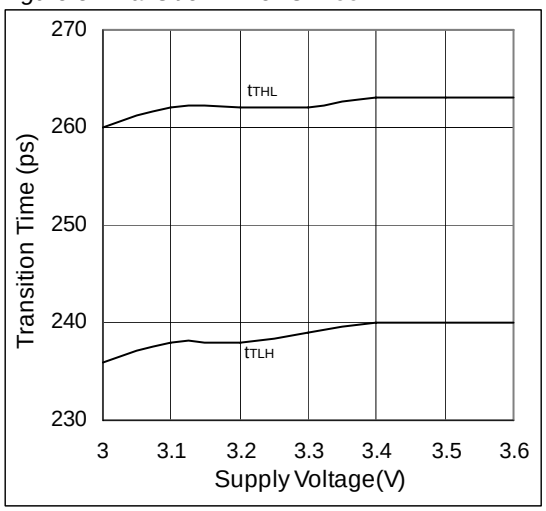


Figure 4. Transition Time vs. Temperature

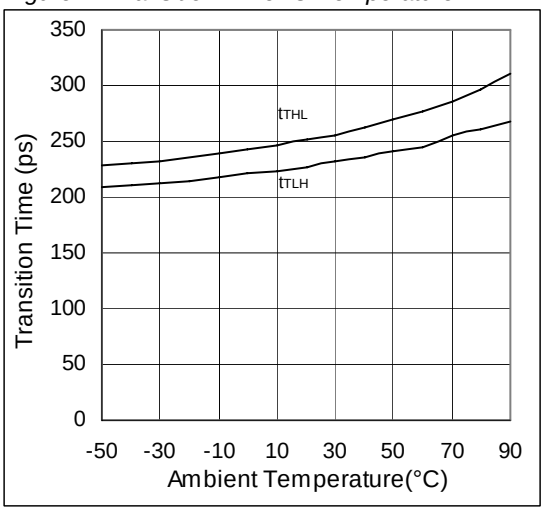


Figure 5. Differential Pulse Skew vs. VCC

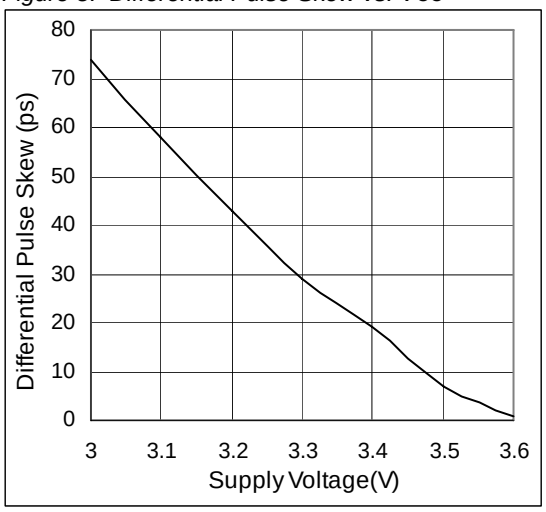


Figure 6. Pulse Skew vs. Temperature

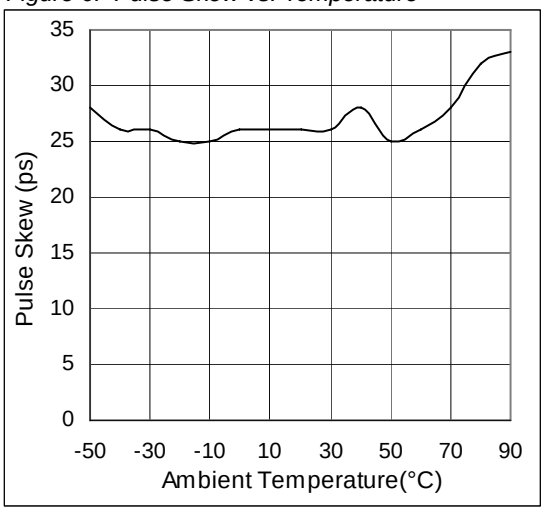


Figure 7. Differential Propagation Delay vs. VCC;

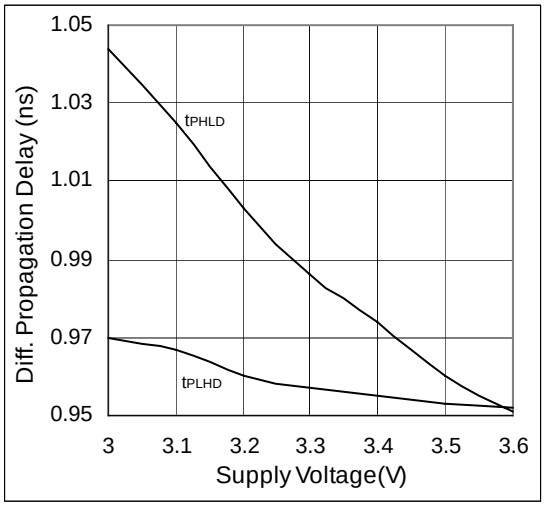


Figure 8. Differential Propagation Delay vs. Temp.

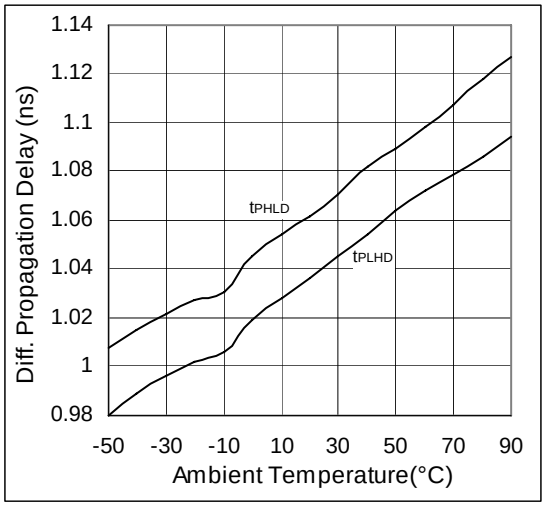


Figure 9. Differential Output Voltage vs. VCC

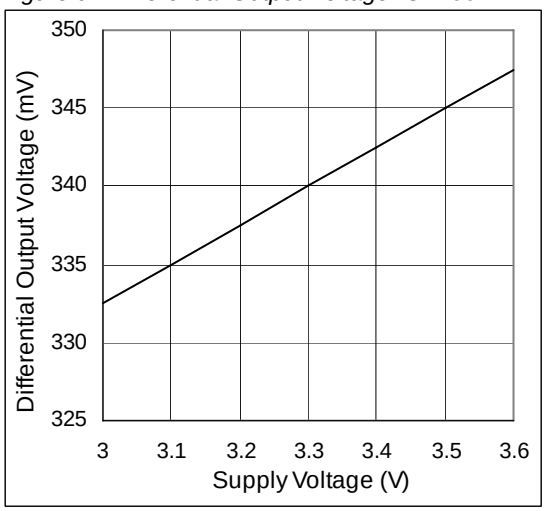


Figure 10. Differential Output Voltage vs. Frequency

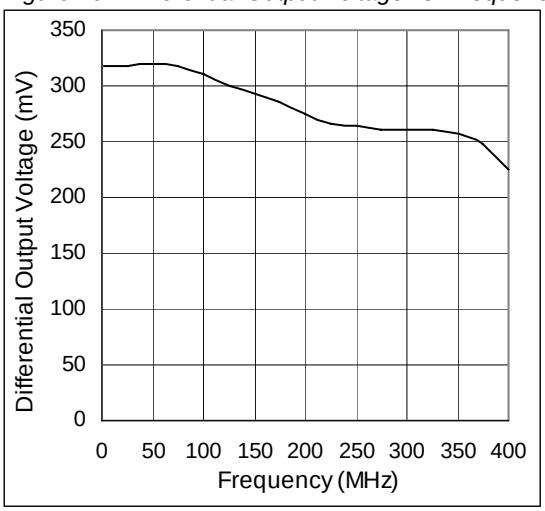


Figure 11. Offset Voltage vs. VCC

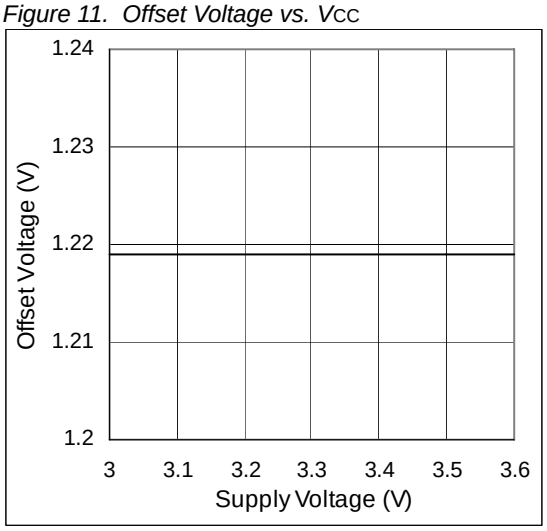


Figure 12. Offset Voltage vs. Frequency

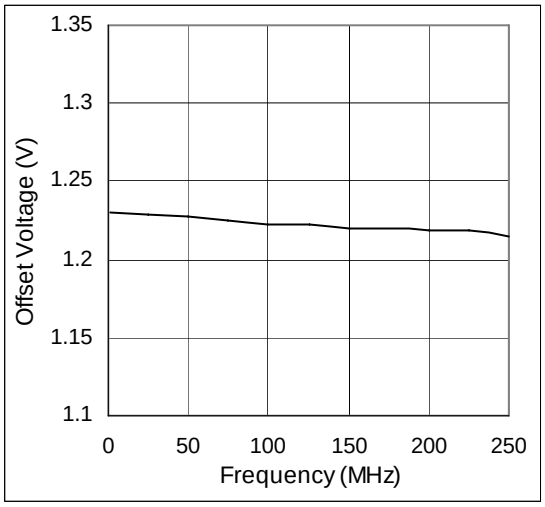


Figure 13. Output Voltage vs. VCC;

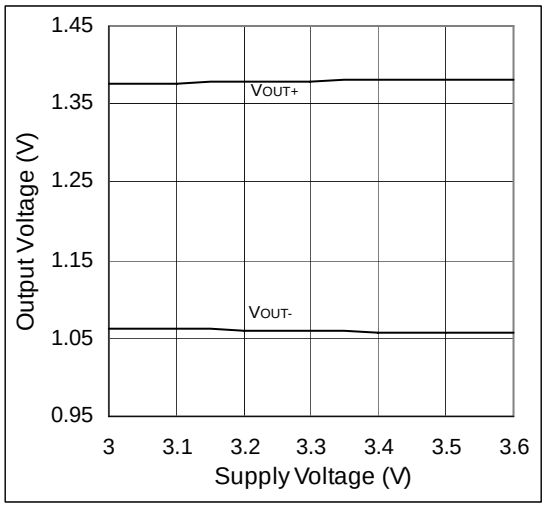


Figure 14. Output Voltage vs. Load Resistance;

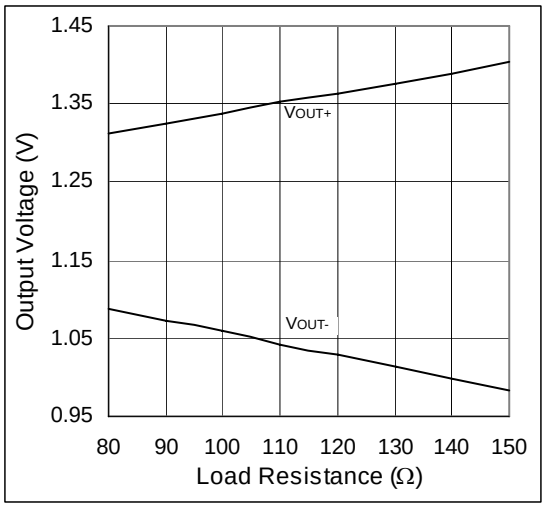


Figure 15. ICC vs. VCC

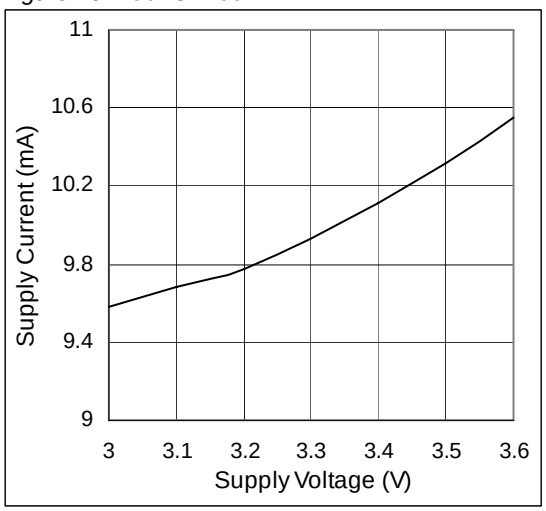


Figure 16. ICC vs. Temperature;

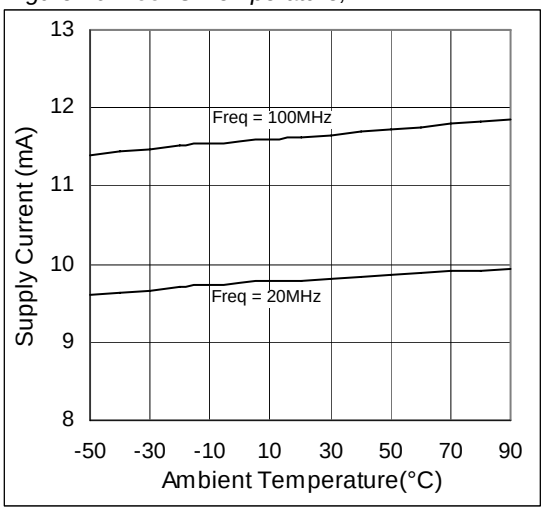


Figure 17. Short Circuit Current vs. VCC

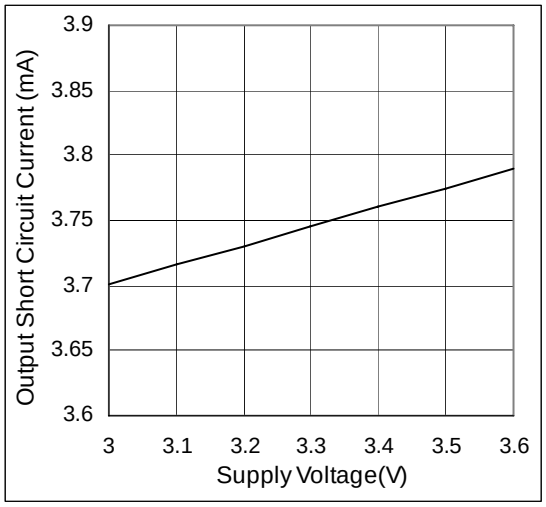
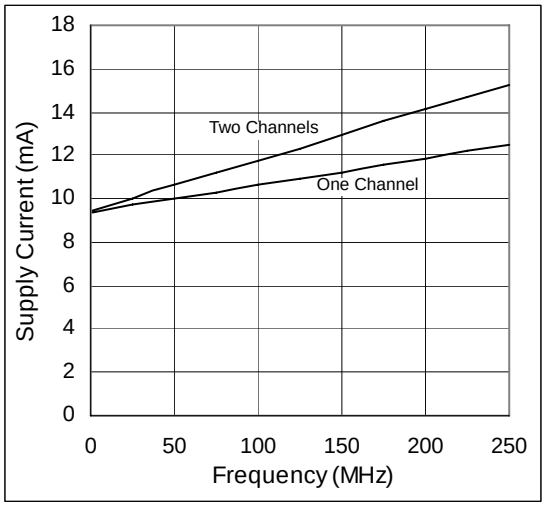


Figure 18. ICC vs. Frequency



8 Detailed Description

LVDS Interface

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the *ANSI/TIA/EIA-644* and *IEEE 1596.3* standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The AS1156/AS1154 is an 800Mbps single/dual differential LVDS driver that is designed for high-speed, point-to-point, low-power applications. This device accepts LVTTL/LVCMOS input levels and translates them to LVDS output signals.

The AS1156/AS1154 generates a 2.5mA to 4.5mA output current using a current-steering configuration. This current steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited, and enter a high-impedance state when the device is not powered or is disabled.

The current-steering architecture of the AS1156/AS1154 requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver (AS1157, AS1158). Logic states are determined by the direction of current flow through the termination resistor.

With a typical 3.7mA output current, the AS1156/AS1154 produces an output voltage of 370mV when driving a 100Ω load.

Termination

Because the AS1156/AS1154 is a current-steering device, no output voltage will be generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels depend upon the value of the termination resistor.

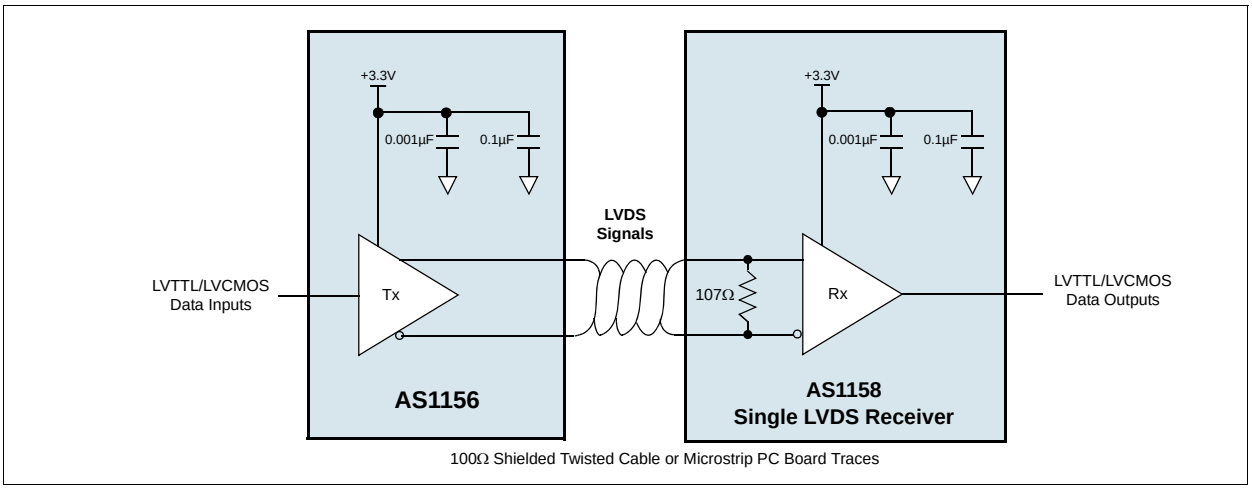
The AS1156/AS1154 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90 and132Ω, depending on the characteristic impedance of the transmission medium.

9 Applications

Table 5. Function Table

Input	Output	
IN*x*	**OUT*x*+**	**OUT*x*-**
L	L	H
H	H	L
0.8V < V_{INx} < 2.0V	Undetermined	Undetermined

Figure 19. Typical Application Circuit



Power-Supply Bypassing

To bypass V_{CC}, use high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to pin V_{CC}.

Differential Traces

Input trace characteristics can adversely affect the performance of the AS1156/AS1154.

- Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor is also matched to this characteristic impedance.
- Eliminate reflections and ensure that noise couples as common mode by running the differential traces near each other.
- Reduce skew by using matched trace lengths. Tight skew control is required to minimize emissions and proper data recovery of the devices.
- Route each channel's differential signals very close to each other for optimal cancellation of their respective external magnetic fields. Use a constant distance between the differential traces to avoid irregularities in differential impedance.
- Avoid 90° turns (use two 45° turns).
- Minimize the number of vias to further prevent impedance irregularities.

Cables and Connectors

Supported transmission media include printed circuit board traces, backplanes, and cables.

- Use cables and connectors with matched differential impedance (typically 100Ω) to minimize impedance mismatches.
- Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.
- Avoid the use of unbalanced cables such as ribbon cable or simple coaxial cable.

Board Layout

The device should be placed as close to the interface connector as possible to minimize LVDS trace length.

- Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.
- Use a four-layer PC board that provides separate power, ground, LVDS signals, and input signals.
- Isolate the input LVDS signals from each other and the output LVCMOS/LVTTL signals from each other to prevent coupling.
- Separate the input LVDS signals from the output signals planes with the power and ground planes for best results.

Figure 20. Driver Propagation Delay and Transition Time Waveforms

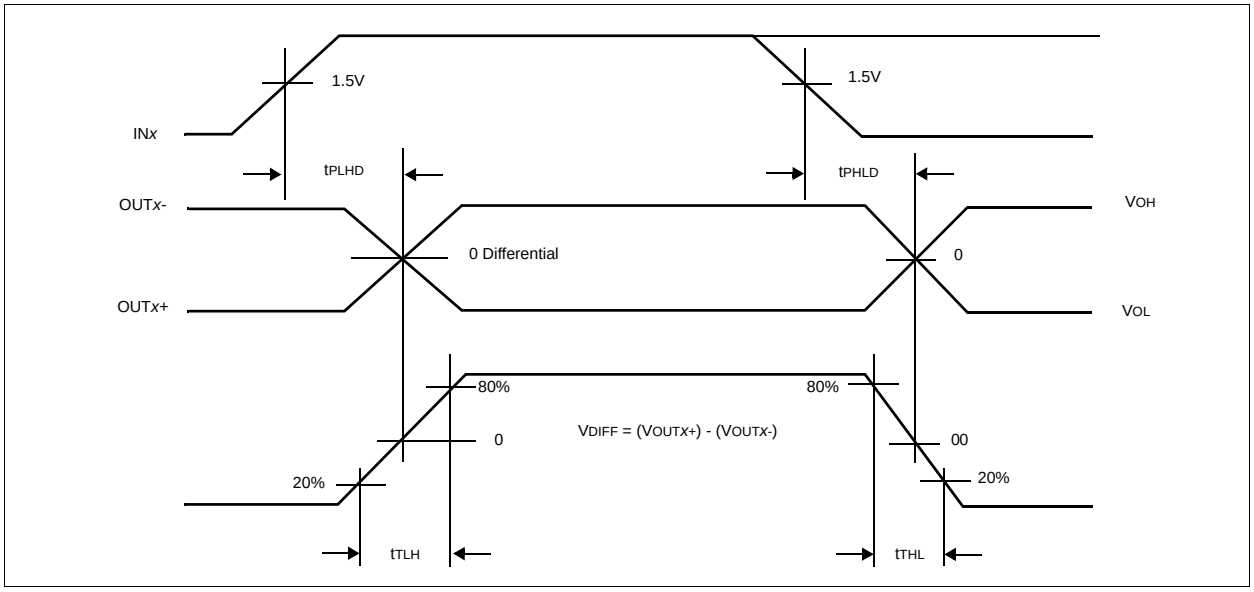


Figure 21. Driver Propagation Delay and Transition Time Test Circuit

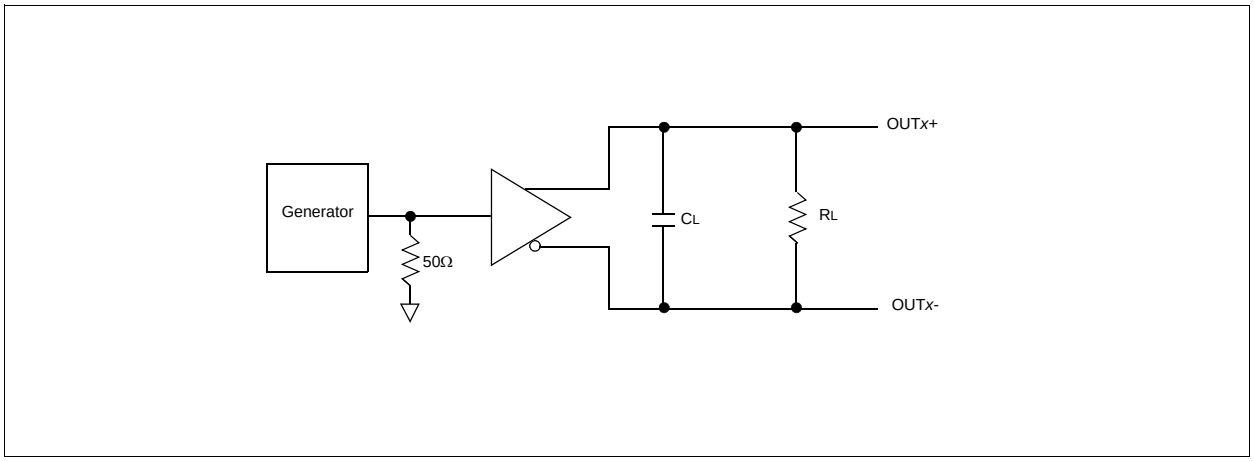
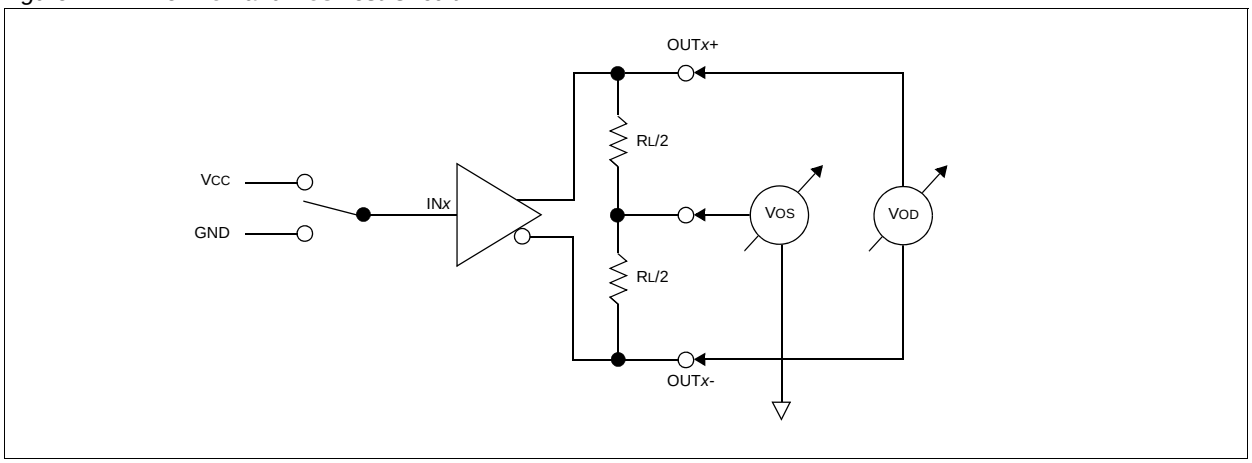


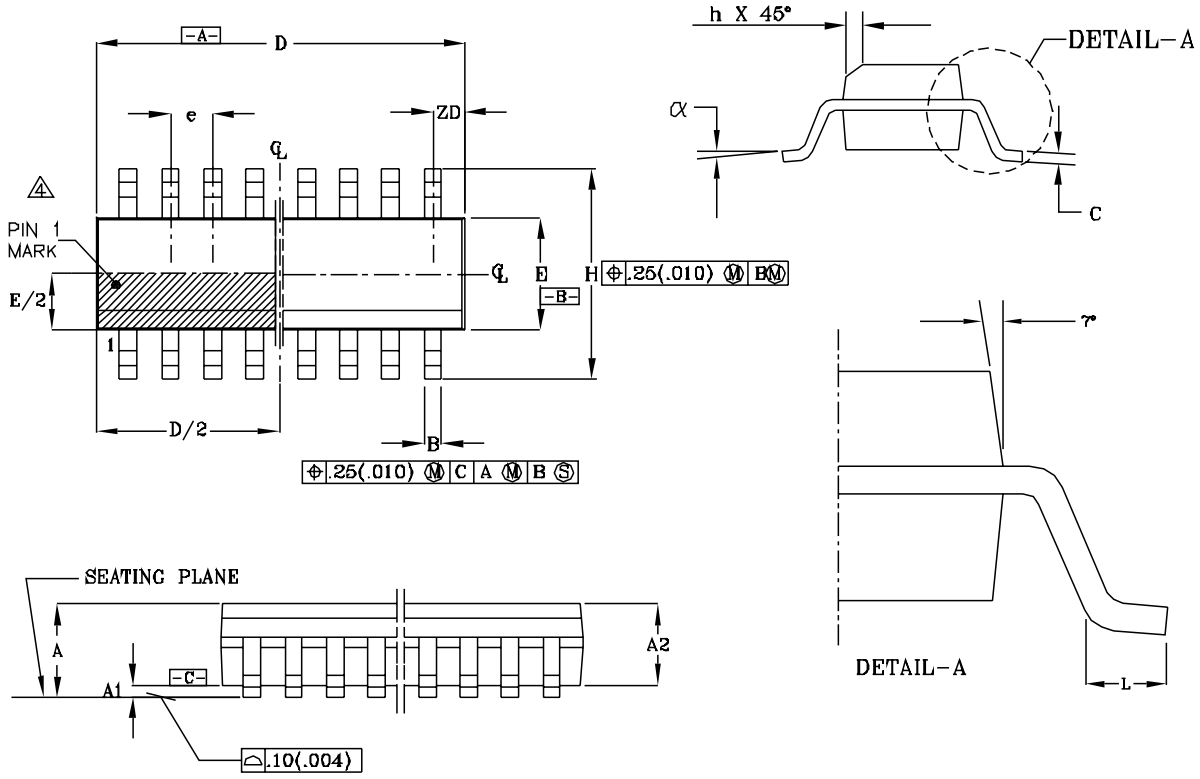
Figure 22. Driver VOD and VOS Test Circuit



10 Package Drawings and Markings

The AS1156/AS1154 is available in a 8-pin SOIC package.

Figure 23. 8-pin SOIC Package



Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004") max.
2. Package surface finishing:
   - Top, matte (charmilles #18-30)
   - All sides, matte (charmilles +18-30)
   - Bottom, smooth or matte (charmilles +18-30)
3. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.25mm (.010") per side.
4. Details of pin #1 mark are optional but must be located within the area indicated.

Symbol	Min	Max
A	1.52	1.72
A1	0.10	0.25
A2	1.37	1.57
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
α	0°	8°
ZD	0.53REF	

11 Ordering Information

Part Number	Description	Delivery Form	Package
AS1156-BSOU	Single Channel LVDS Line Driver	Tubes	SOIC-8
AS1156-BSOT	Single Channel LVDS Line Driver	Tape and Reel	SOIC-8
AS1154-BSOU	Dual Channel LVDS Line Driver	Tubes	SOIC-8
AS1154-BSOT	Dual Channel LVDS Line Driver	Tape and Reel	SOIC-8

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