

# AS1361/AS1362

Data Sheet

## 150mA/300mA, Ultra-Low-Noise, High-PSRR Low Dropout Regulators, with POK

### 1 General Description

The AS1361/AS1362 are ultra-low-noise, low-dropout linear regulators specifically designed to deliver up to 150/300mA continuous output current, and can achieve a low 140mV dropout for 300mA load current. The LDOs are designed and optimized to work with low-cost, small-capacitance ceramic capacitors.

The devices are available as the standard products listed in Table 1.

Table 1. Standard Products

Model	Load Current	Output Voltage
AS1361	150mA	Preset – 1.5 to 4.5V
AS1362	300mA	Preset – 1.5 to 4.5V

An integrated P-channel MOSFET pass transistor allows the devices to maintain extremely low quiescent current (40µA).

The AS1361/AS1362 uses an advanced architecture to achieve ultra-low output voltage noise of 9µVRMS and a power-supply rejection-ratio of better than 80dB (up to 10kHz).

An active-Low, open-drain power-ok output indicates if the output voltage is within regulation.

The AS1361/AS1362 requires only 1µF output capacitor for stability at any load. When the LDO is disabled, current consumption drops below 500nA.

The devices are available in a TSOT23 6-pin package.

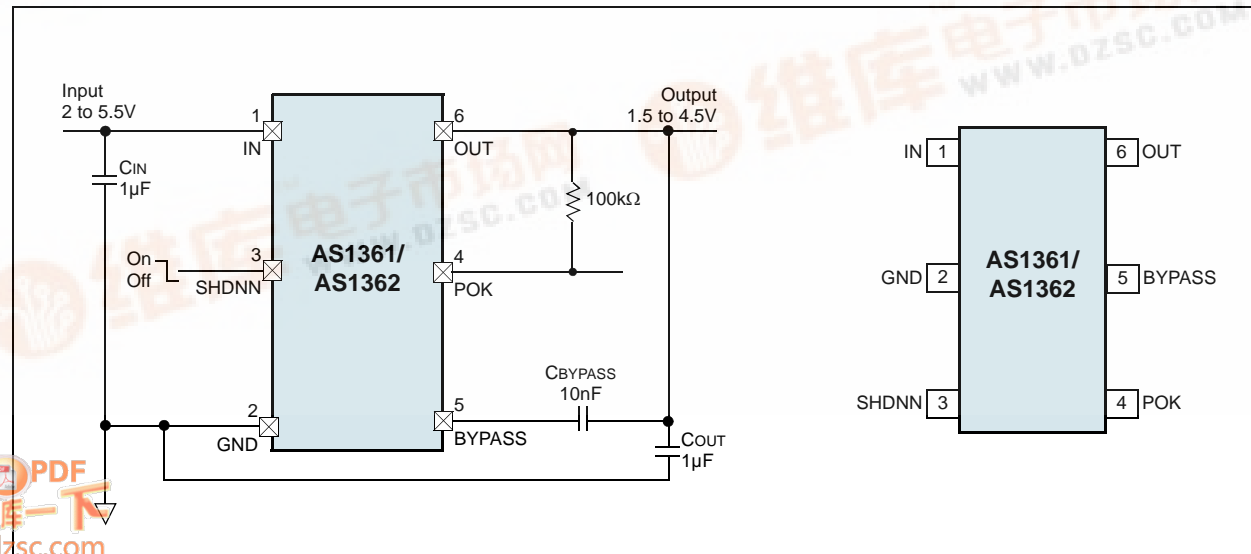
### 2 Key Features

- Preset Output Voltages: 1.5 to 4.5V (in 50mV steps)
- Output Noise: 9µVRMS @ 100Hz to 100kHz
- Power-Supply Rejection Ratio: 92dB @ 1kHz
- Low Dropout: 140mV @ 300mA Load
- Power-OK Output
- Stable with 1µF Ceramic Capacitor for any Load
- Guaranteed 150/300mA Output
- 1.25V Internal Reference
- Extremely-Low Quiescent Current: 40µA
- Excellent Load/Line Transient
- Overcurrent and Thermal Protection
- TSOT23 6-pin Package

### 3 Applications

The devices are ideal for mobile phones, wireless phones, PDAs, handheld computers, mobile phone base stations, Bluetooth portable radios and accessories, wireless LANs, digital cameras, personal audio devices, and any other portable, battery-powered application.

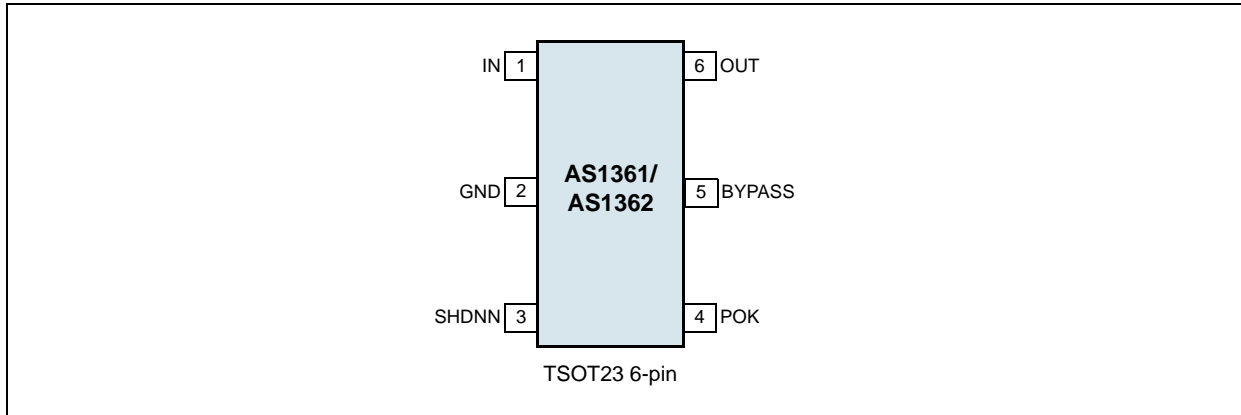
Figure 1. Typical Application Circuit



## 4 Pinout

### Pin Assignments

Figure 2. Pin Assignments (Top View)



### Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	IN	<b>Unregulated Input Supply.</b>
2	GND	<b>Ground</b>
3	SHDNN	<b>Shutdown.</b> Pull this pin low to disable the LDO.
4	POK	<b>Power-OK Output.</b> Active-Low, open-drain output indicates if the output voltage is within regulation. 0 = $V_{OUT} < 94\% V_{OUTNOM}$ 1 = $V_{OUT} > 94\% V_{OUTNOM}$
5	BYPASS	<b>Noise Bypass for Low-Noise Operation.</b> Connect a 10nF capacitor from this pin to <b>OUT</b> . <b>Note:</b> This pin is shorted to GND in shutdown mode.
6	OUT	<b>Regulated Output Voltage.</b> Bypass this pin with a capacitor to GND. See <a href="#">Capacitor Selection and Regulator Stability on page 10</a> for more details.

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
IN to GND	-0.3	+7	V	
OUT, SHDNN, POK to GND	-0.3	IN + 0.3	V	
BYPASS to GND	-0.3	OUT + 0.3	V	
Output Short-Circuit Duration		Infinite		
Thermal Resistance $\Theta_{JA}$		201.7	$^{\circ}\text{C}/\text{W}$	on PCB
Operating Temperature Range	-40	+85	$^{\circ}\text{C}$	
Junction Temperature		+150	$^{\circ}\text{C}$	
Storage Temperature Range	-65	+150	$^{\circ}\text{C}$	
Package Body Temperature		+260	$^{\circ}\text{C}$	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn).

## 6 Electrical Characteristics

$V_{IN} = V_{OUT} + 0.5V$ ,  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 1\mu F$ ,  $C_{BYPASS} = 10nF$ ,  $T_{AMB} = -40$  to  $+85^{\circ}C$  (unless otherwise specified). Typ values are at  $T_{AMB} = +25^{\circ}C$ . Limits 100% tested at  $+25^{\circ}C$ . Limits over operating temperature range guaranteed by design.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IN}$	Input Voltage Range		2		5.5	V
	Output Voltage Accuracy	$I_{OUT} = 1mA$ , $T_{AMB} = +25^{\circ}C$	-0.5		+0.5	%
		$I_{OUT} = 100\mu A$ to $150mA$ , $T_{AMB} = +25^{\circ}C$ (AS1361)	-0.75		+0.75	
		$I_{OUT} = 100\mu A$ to $300mA$ , $T_{AMB} = +25^{\circ}C$ (AS1362)	-1.0		+1.0	
		$I_{OUT} = 100\mu A$ to $150mA$ , (AS1361)	-1.5		+1.5	
		$I_{OUT} = 100\mu A$ to $300mA$ , (AS1362)	-2.0		+2.0	
$I_{OUT}$	Maximum Output Current	AS1361	150			mA
		AS1362	300			
$I_{LIMIT}$	Current Limit	AS1361, $OUT = 90\%$ of nom., $T_{AMB} = +25^{\circ}C$	250	270		mA
		AS1362, $OUT = 90\%$ of nom., $T_{AMB} = +25^{\circ}C$	470	510		
	Dropout Voltage <sup>1</sup>	$V_{OUT} \geq 3V$ , $I_{OUT} = 150mA$		70	95	mV
		$V_{OUT} \geq 3V$ , $I_{OUT} = 300mA$ , (AS1362 only)		140	200	
$I_Q$	Quiescent Current	$I_{OUT} = 0.05mA$		40	90	$\mu A$
		$V_{IN} = V_{OUTNOM} - 0.1V$ , $I_{OUT} = 0mA$		150	250	
$V_{LNR}$	Line Regulation	$V_{IN} = (V_{OUT} + 0.5V)$ to $5.5V$ , $I_{OUT} = 0.1mA$		0.02		%/V
$V_{LDR}$	Load Regulation	$I_{OUT} = 1$ to $150/300mA$		0.0005		%/mA
$I_{SHDNN}$	Shutdown Supply Current	$SHDNN = 0V$		9	500	nA
PSRR	Ripple Rejection	$f = 1kHz$ , $I_{OUT} = 10mA$		92		dB
		$f = 10kHz$ , $I_{OUT} = 10mA$		80		
		$f = 100kHz$ , $I_{OUT} = 10mA$		62		
	Output Noise Voltage (RMS)	$f = 100Hz$ to $100kHz$ , $I_{LOAD} = 0$ to $150/300mA$		9		$\mu V$
<b>Shutdown</b>						
	Shutdown Exit Delay <sup>2</sup>	$R_{LOAD} = 50\Omega$			300	$\mu s$
	SHDNN Logic Low Level	$V_{IN} = 2$ to $5.5V$			0.4	V
	SHDNN Logic High Level	$V_{IN} = 2$ to $5.5V$	1.5			V
<b>Power-OK Output</b>						
$V_{POK}$	Power-OK Voltage Threshold	$I_{OUT} = 0$ , $V_{OUTRISING}$	90	94	98	% $V_{OUT}$
		Hysteresis, $I_{OUT} = 0$		1.5		
$V_{OL}$	POK Output Voltage Low	$I_{SINK} = 1mA$			0.3	V
	POK Output Leakage Current	$V_{OUT}$ in regulation			1	$\mu A$
<b>Thermal Protection</b>						
$T_{SHDNM}$	Thermal Shutdown Temperature			160		$^{\circ}C$
$\Delta T_{SHDNM}$	Thermal Shutdown Hysteresis			15		$^{\circ}C$

1. Dropout is defined as  $V_{IN} - V_{OUT}$  when  $V_{OUT}$  is 100mV below the value of  $V_{OUT}$  for  $V_{IN} = V_{OUT} + 0.5V$ .

2. Time needed for  $V_{OUT}$  to reach 90% of final value.

## 7 Typical Operating Characteristics

$V_{IN} = V_{OUT} + 0.5V$ ,  $C_{IN} = C_{OUT} = 1\mu F$ ,  $C_{BYPASS} = 10nF$ ,  $T_{AMB} = 25^{\circ}C$  (unless otherwise specified).

Figure 3. Output Voltage vs. Input Voltage

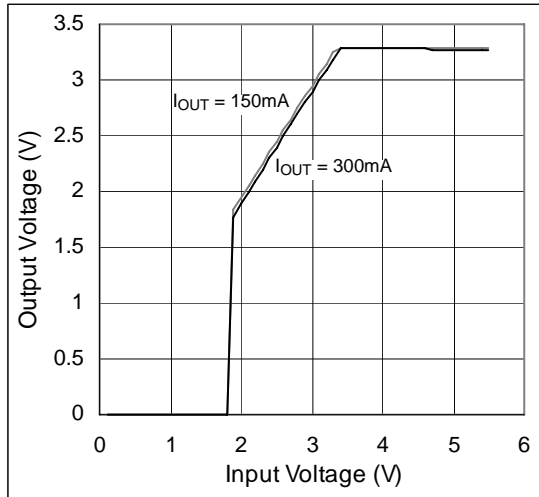


Figure 4. Output Voltage Accuracy vs. Load Current

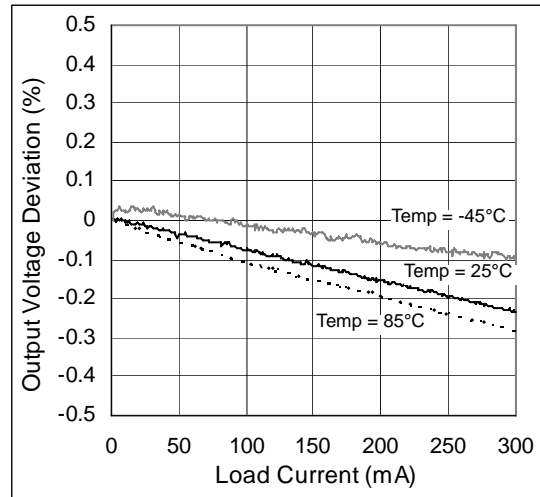


Figure 5. Output Voltage Accuracy vs. Temperature

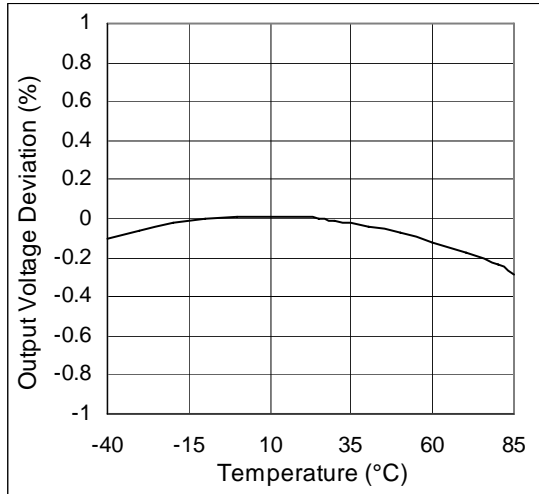


Figure 6. Dropout Voltage vs. Load Current

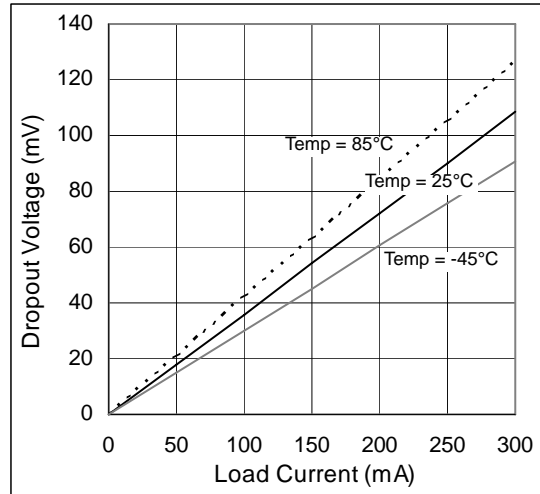


Figure 7. Dropout Voltage vs. Output Voltage

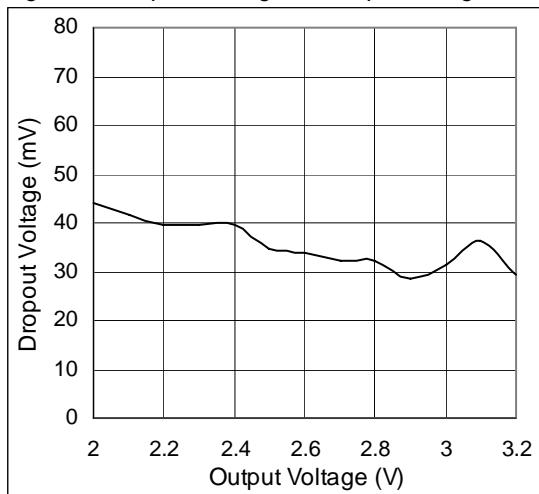


Figure 8. Ground Pin Current vs. Input Voltage

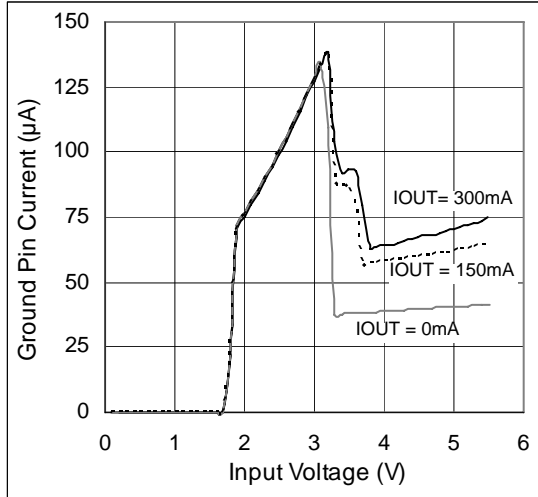


Figure 9. Ground Pin Current vs. Load Current

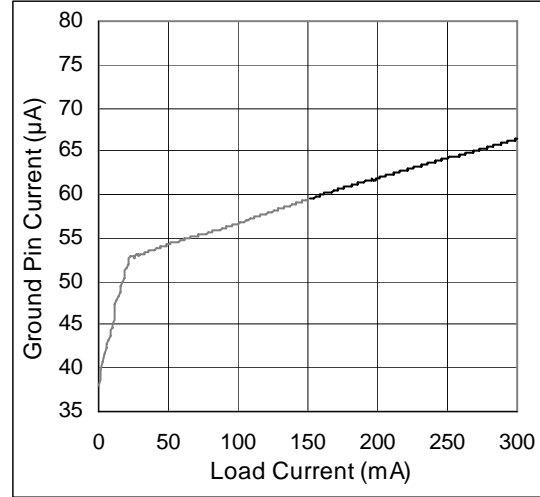


Figure 10. Ground Pin Current vs. Temperature

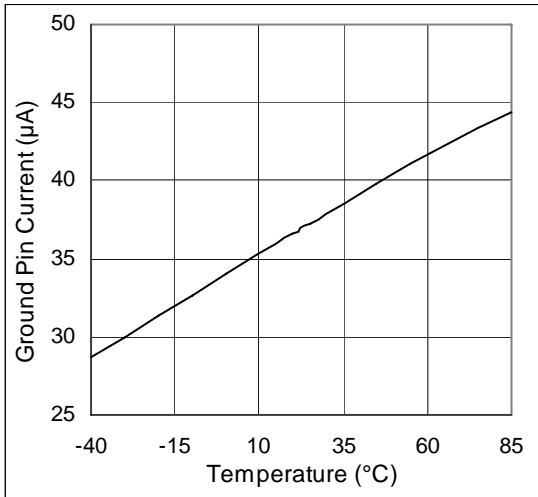


Figure 11. PSRR vs. Frequency

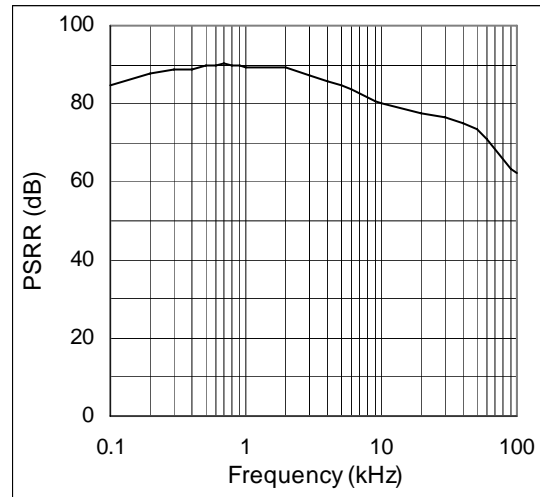


Figure 12. Output Noise Spectral Density vs. Freq.

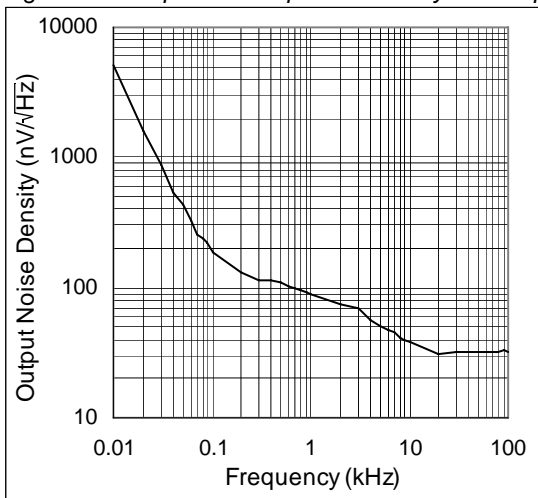


Figure 13. Output Noise vs. Bypass Capacitance

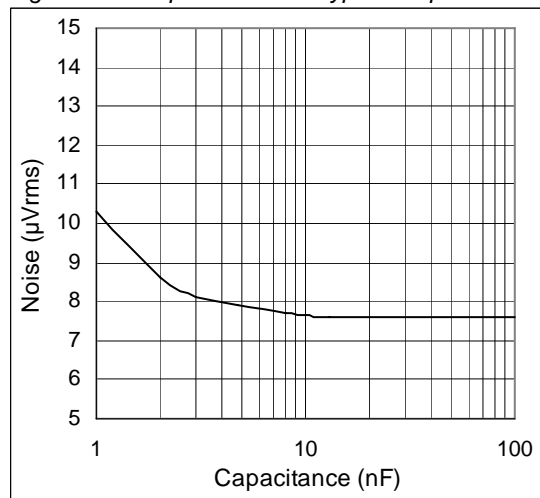


Figure 14. Load Transient Response,  
 $V_{IN} = 3.8V$ ,  $V_{OUT} = 3.3V$

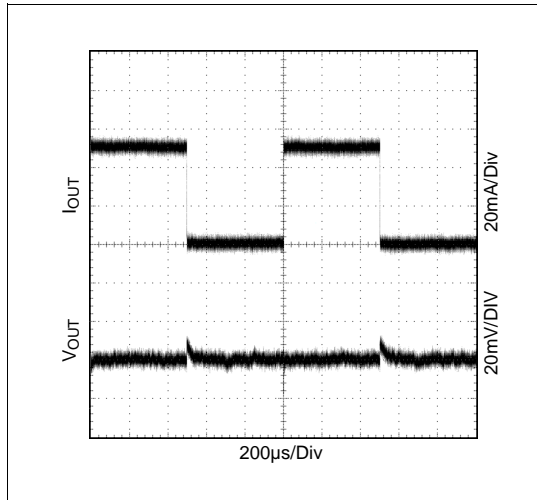


Figure 15. Load Transient Response near Dropout,  
 $V_{IN} = 3.4V$ ,  $V_{OUT} = 3.3V$

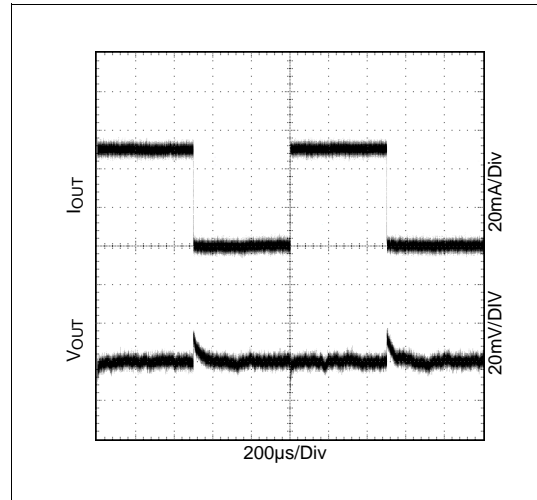


Figure 16. Line Transient Response

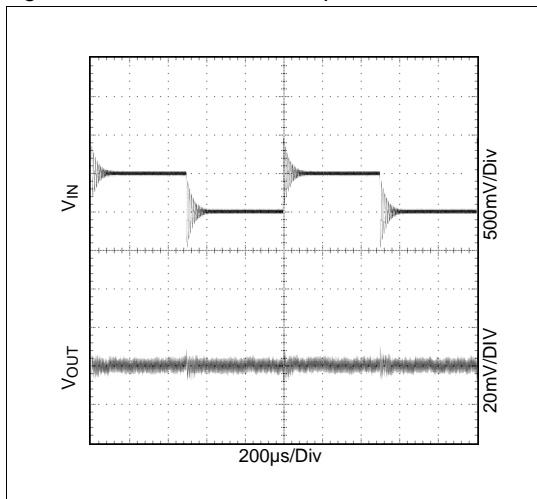
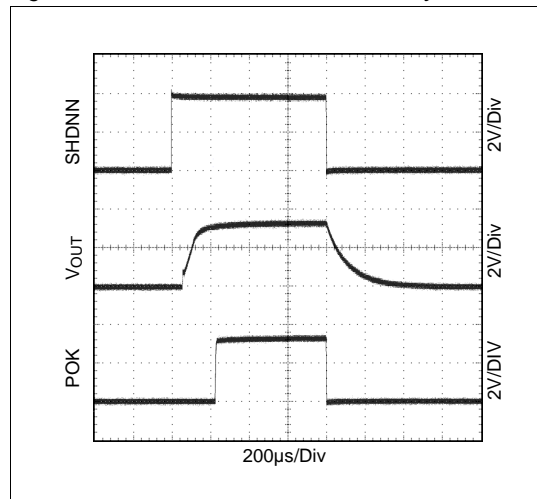


Figure 17. Enter & Exit Shutdown Delay



## 8 Detailed Description

The AS1361/AS1362 are ultra-low-noise, low-dropout, low-quiescent current linear-regulators specifically designed for space-limited applications. The devices are available with preset output voltages from 1.5 to 4.5V in 50mV increments.

These devices can supply loads up to 150/300mA. As shown in [Figure 18](#), the AS1361/AS1362 consist of an integrated bandgap core and noise bypass circuitry, error amplifier, P-channel MOSFET pass transistor, and internal feedback voltage-divider.

The output voltage is fed back through an internal resistor voltage-divider connected to pin OUT. An external bypass capacitor connected to pin BYPASS reduces noise at the output. Additional blocks include a current limiter, thermal sensor, and shutdown logic.

### Internal Voltage Reference

The 1.25V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled high, allowing less current to pass to the output.

### Internal P-Channel Pass Transistor

The AS1361/AS1362 feature a 0.5Ω (typ) P-channel MOSFET pass transistor, which provides several advantages over similar designs using a PNP pass transistor, including prolonged battery life. The P-channel MOSFET does not require a base driver, thus quiescent current is dramatically reduced. The AS1361/AS1362 LDOs do not exhibit problems associated with typical PNP-based LDOs, and consume only 40μA of quiescent current in light load and 220μA in dropout (see [Typical Operating Characteristics on page 5](#)).

### Output Voltage

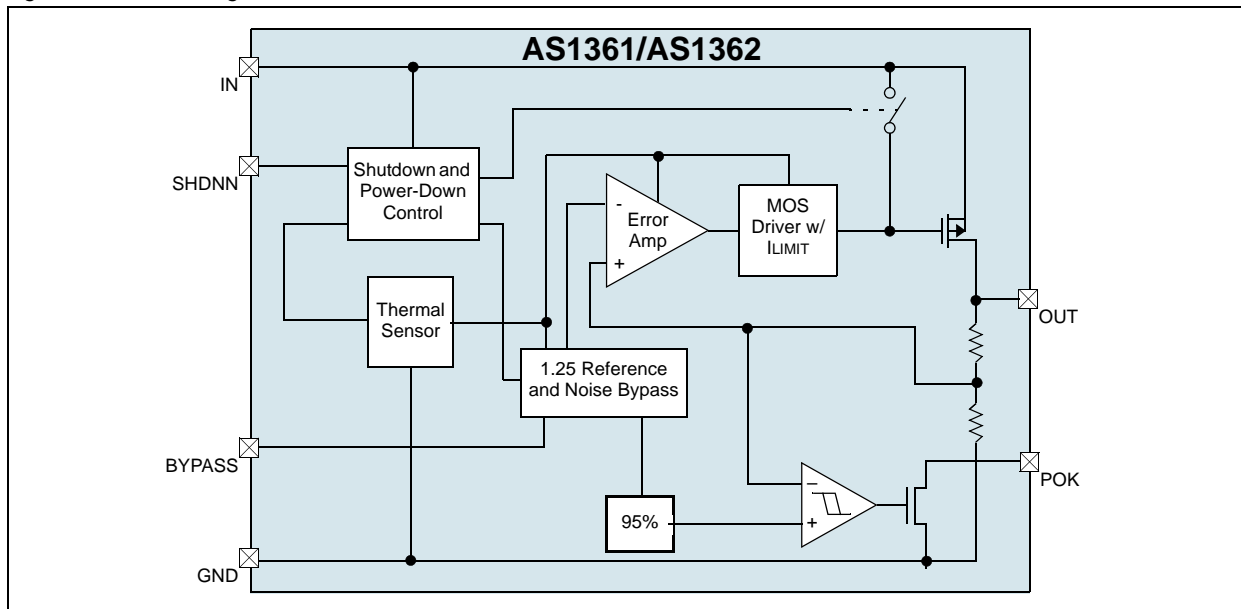
The AS1361/AS1362 deliver preset output voltages from 1.5 to 4.5V, in 50mV increments (see [Ordering Information on page 12](#)).

### Shutdown

The AS1361/AS1362 feature a low-power shutdown mode that reduces quiescent current to <200nA. Driving SHDNN low disables the internal voltage reference, error amplifier, gate-drive circuitry, and P-channel MOSFET pass transistor (see [Figure 18](#)), and the device output enters a high-impedance state.

**Note:** For normal operation connect pin SHDNN to pin IN.

Figure 18. Block Diagram



## Power-OK

The power-ok circuitry is built around an N-channel MOSFET. The circuitry monitors the output voltage and if the voltage goes out of regulation (e.g. during dropout, current limit, or thermal shutdown) pin POK goes low.

The power-OK feature is not active during shutdown and provides a power-on-reset (POR) function that can operate down to  $V_{IN} = 1V$ . A capacitor to GND may be added to generate a POR delay.

To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help minimize current consumption; a 100k $\Omega$  resistor is perfect for most applications (see Figure 1 on page 1).

## Current Limit

The AS1361/AS1362 include a current limiting circuitry to monitor and control the P-channel MOSFET pass transistor's gate voltage, thus limiting the device output current to 270mA (AS1361) and 510mA (AS1362).

**Note:** See Table 4 on page 4 for the recommended min and max current limits. The output can be shorted to ground indefinitely without causing damage to the device.

## Thermal Protection

Integrated thermal protection circuitry limits total power dissipation in the AS1361/AS1362. When the junction temperature ( $T_J$ ) exceeds +160°C, the thermal sensor signals the shutdown logic, turning off the P-channel MOSFET pass transistor and allowing the device to cool down. The thermal sensor turns the pass transistor on again after the device's junction temperature drops by 10°C, resulting in a pulsed output during continuous thermal-overload conditions.

**Note:** Thermal protection is designed to protect the devices in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

## Operating Region and Power Dissipation

The AS1361/AS1362 maximum power dissipation is dependant on the thermal resistance of the case and PCB, the temperature difference between the die junction and  $T_{AMB}$ , and airflow rate.

Power dissipation across the device is calculated as:

$$PD = I_{OUT} (V_{IN} - V_{OUT}) \quad (EQ 1)$$

The maximum power dissipation is calculated:

$$PD_{MAX} = (T_J - T_{AMB}) / (\theta_{JC} + \theta_{CA}) \quad (EQ 2)$$

### Where:

$T_J - T_{AMB}$  is the temperature difference between the AS1361/AS1362 die junction and the surrounding air;

$\theta_{JC}$  is the thermal resistance of the package;

$\theta_{CA}$  is the thermal resistance through the PC board/copper traces/other materials to the surrounding air.

**Note:** Pin GND of the AS1361/AS1362 provides the electrical connection to system ground and also serves as a heat sink. Connect pin GND to the system ground using a large pad or ground plane.

## Noise Reduction

The AS1361/AS1362 noise bypass circuitry dramatically reduces output noise, exhibiting 9 $\mu$ V<sub>RMS</sub> of output voltage noise with  $C_{BYPASS} = 0.01\mu$ F and  $C_{OUT} = 1\mu$ F. Use an external 0.01 $\mu$ F bypass capacitor between pin BYPASS and pin OUT (see Figure 1 on page 1).

**Note:** Startup time is minimized by internal power-on circuitry which pre-charges  $C_{BYPASS}$ .

## 9 Application Information

### Capacitor Selection and Regulator Stability

For normal operation, use a 1  $\mu\text{F}$  capacitor at pin IN and a 1  $\mu\text{F}$  capacitor at pin OUT. Larger input capacitor values and lower ESR provide better noise rejection and line-transient response. Reduce output noise and improve load-transient response, stability, and power-supply rejection by using large output capacitors.

**Note:** Some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use a 2.2  $\mu\text{F}$  or larger output capacitor to ensure stability at temperatures below  $-10^{\circ}\text{C}$ . With X7R or X5R dielectrics, 1  $\mu\text{F}$  is sufficient at all operating temperatures.

### Bypass Capacitor

Use a 0.01  $\mu\text{F}$  bypass capacitor at pin BYPASS for low-output voltage noise reduction. The leakage current going into pin BYPASS should be less than 10 nA. Increasing the capacitance slightly decreases the output noise. Values above 0.1  $\mu\text{F}$  and below 0.001  $\mu\text{F}$  are not recommended.

### Noise, PSRR, and Transient Response

The AS1361/AS1362 are designed to deliver ultra-low noise and high PSRR, as well as low dropout and low quiescent currents in battery-powered systems. The power-supply rejection is 92 dB at 1 kHz and 62 dB at 100 kHz. ([see PSRR vs. Frequency on page 6](#)).

When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors, and through passive filtering techniques.

The [Figure 16](#) and [Figure 14 on page 7](#) show the AS1361/AS1362 line- and load-transient responses.

### Dropout Voltage

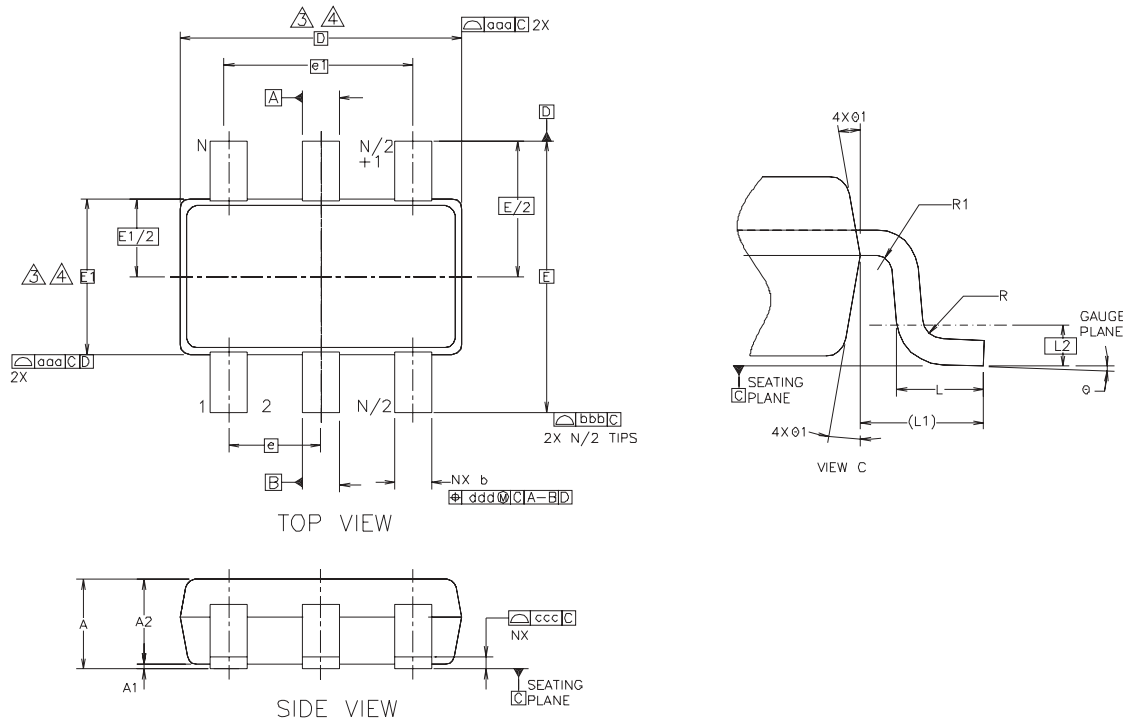
The AS1361/AS1362 minimum dropout voltage determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage.

Since the AS1361/AS1362 use a P-channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance ( $R_{\text{DS(ON)}}$ ) multiplied by  $I_{\text{LOAD}}$  ([see Figure 6 on page 5](#)).

# 10 Package Drawings and Markings

The devices are available in a TSOT23 6-pin package.

Figure 19. TSOT23 6-pin Package



Symbol	Min	Typ	Max	Notes	Symbol	Min	Typ	Max	Notes
A			1.00		L	0.30	0.40	0.50	
A1	0.01	0.05	0.10		L1	0.60REF			
A2	0.84	0.87	0.90		L2	0.25BSC			
b	0.30		0.45		N		6		
b1	0.31	0.35	0.39		R	0.10			
c	0.12	0.15	0.20		R1	0.10		0.25	
c1	0.08	0.13	0.16		θ	0°	4°	8°	
D		2.90BSC		3,4	θ1	4°	10°	12°	
E		2.80BSC		3,4	<b>Tolerances of Form and Position</b>				
E1		1.60BSC		3,4	aaa		0.15		
e		0.95BSC			bbb		0.25		
e1		1.90BSC			ccc		0.10		
					ddd		0.20		

**Notes:**

1. Dimensioning and tolerancing conform to ASME Y14.5M - 1994.
2. Dimensions are in millimeters.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15mm per side. Dimensions D and E1 are determined at datum H.
4. The package top can be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but include any mismatches between the top of the package body and the bottom. D and E1 are determined at datum H.

## 11 Ordering Information

The devices are available as the standard products shown in [Table 5](#).

Table 5. Ordering Information

Model	Marking	Output Current	Output Voltage	Delivery Form	Package
AS1361-BTTT-15	ASL2	150mA	1.5V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-18	ASL3	150mA	1.8V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-25	ASL4	150mA	2.5V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-26	ASL5	150mA	2.6V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-27	ASL6	150mA	2.7V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-28	ASL7	150mA	2.8V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-285	ASL8	150mA	2.85V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-30	ASL9	150mA	3.0V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-33	ASMA	150mA	3.3V	Tape and Reel	TSOT23 6-pin
AS1361-BTTT-45	ASMB	150mA	4.5V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-15	ASMC	300mA	1.5V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-18	ASMD	300mA	1.8V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-25	ASME	300mA	2.5V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-26	ASMF	300mA	2.6V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-27	ASMG	300mA	2.7V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-28	ASMH	300mA	2.8V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-285	ASMI	300mA	2.85V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-30	ASMJ	300mA	3.0V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-33	ASMK	300mA	3.3V	Tape and Reel	TSOT23 6-pin
AS1362-BTTT-45	ASML	300mA	4.5V	Tape and Reel	TSOT23 6-pin

Non-standard devices from 1.5 to 4.5V are available in 50mV steps. For more information and inquiries contact <http://www.austriamicrosystems.com/contact>

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