austria**micro**systems

programming rates up to 10MHz. The AS1500 is available in four different resistor values. The AS1500 incorporates a

 $10k\Omega$, the AS1501 a $20k\Omega$, the AS1502 a $50k\Omega$ and the

AS1503 a $100k\Omega$ fixed resistor. The wiper contact taps the

fixed resistor at points determined by the 8-bit digital code

word. The resistance between the wiper and the endpoint of

the resistor is linear. The switching action is performed in a

way that no glitches occur. Furthermore the AS150x product

family includes a shutdown mode, where it consumes less

than $1\mu A$. The AS150x is available in an 8-pin SOIC

package. All parts are guaranteed to operate over the

extended industrial temperature range of -40°C to +125°C.

WWW.DZSC.CO

Digital Potentiometer AS1500/AS1501/AS1502/AS1503

DATASHEET

Key Features

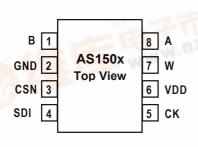
- 256-Position
- Available in four Resistance values
 - AS1500 resistance 10kOhms
 - AS1501 resistance 20kOhms
 - AS1502 resistance 50kOhms
 - -AS1503 resistance 100kOhms
- Power Shutdown —Less than 1 μA
- 3-Wire SPI-Compatible Serial Data Input
- 10 MHz Update Data Loading Rate
- 2.7 V to 5.5 V Single-Supply Operation
- Temperature Range –40°C to +125°C
- Package SO-8
- Compatible to AD8400

Applications

- Line Impedance Matching
- Volume Control, Panning
- Mechanical Potentiometer Replacement
- Power Supply Adjustment
- Programmable Filters, Delays, Time Constants

General Description

The AS1500 is a digital potentiometer with 256 programmable steps. The values of the resistor can be controlled via 3 wire serial interface capable to handle



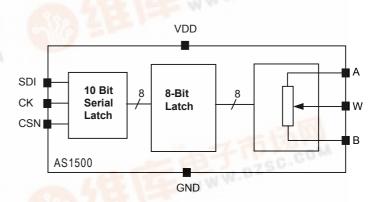


Figure 1 Pinout andfunctional Block Diagram of Digital Potentiometer AS150x family

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Data Sheet AS1500/1/2/3

ABSOLUTE MAXIMUM RATINGS

(TA = 25°C, unless otherwise noted.)

Parameter	Limits
VDD to GND	-0.3V, +7V
VA, VB, VW to GND	0V, VDD
AX – BX, AX – WX, BX – WX	±20mA
Digital Input and Output Voltage to GND	0V, +7V
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature (TJ max)	150°C
Storage Temperature	-65°C to +150°C
Package body temperature ¹	260°C
Package Power Dissipation	(TJ max – TA) / θJA
ESD ²	1kV

Table 1: Absolute Maximum Ratings

Pin	Name	Description
1	В	Terminal B RDAC
2	GND	Ground
		Chip Select Input, Active Low. When CS returns high,
3	CSN	data in the serial input register is loaded into the DAC
		register.
4	SDI	Serial Data Input
5	CK	Serial Clock Input, Positive Edge Triggered.
6	VDD	Positive power supply, specified for operation at both 3V
0 100		and 5V.
7	W	Wiper RDAC
8	Α	Terminal A RDAC

Table 2: Pin Function Description

The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for non hermetic Solid State Surface Mount Devices".

² HBM MIL-Std883E 3015.7methods.

AS1500 / AS1501 - SPECIFICATIONS

VDD = $3V\pm10\%$ or $5V\pm10\%$, V_A = VDD, V_B = 0V, $-40^{\circ}C \le T_A \le +125^{\circ}C$ unless otherwise noted.

ELECTRICAL CHARACTERISTICS – 10k and 20k VERSIONS

Parameter	Symbol	Conditions	Min	Typ ³	Max	Unit
DC CHARACTERISTICS RE	HEOSTAT N	NODE				
Naminal Danistana 4	1	$T_A = 25$ °C, VDD = 5V, AS1500, Version: $10k\Omega$	8	10	12	kΩ
Nominal Resistance ⁴	R_{AB}	$T_A = 25$ °C, VDD = 5V, AS1501, Version: $20k\Omega$	16	20	24	kΩ
Resistance Tempco ⁵	$\Delta R_{AB}/\Delta T$	V _{AB} = VDD, Wiper = No Connect		500		ppm/°C
Wiper Resistance	Rw	VDD = 5V	20	100	200	Ω
Resistor Differential NL ⁶	R-DNL	R _{WB} , VDD = 5V, V _A = No Connect	-1	±1/4	+1	LSB
Resistor Integral NL	R-INL	R _{WB} , VDD = 5V, V _A = No Connect	-2	±1/2	+2	LSB
DC CHARACTERISTICS PC		TED DIVIDED		1 1/2	'-	LOD
Resolution	N	TER DIVIDER		8		Bits
Resolution	IN	VDD = 5.5V T _A = 25°C	-2	±1/2	+2	LSB
Integral Nonlinearity	INL		-2 -2			
		VDD = 2.7V T _A = 25°C		±1/2	+2	LSB
Differential Nonlinearity	DNL	VDD = 5.5V T _A = 25°C	-1	±1/4	+1	LSB
<u> </u>		VDD = 2.7V T _A = 25°C	-1	±1/4	+1	LSB
Voltage Divider Tempco	$\Delta V_W / \Delta T$	Code = 80 _H		15		ppm/°C
Full-Scale Error	V _{WFSE}	Code = FF _H , VDD = 5.5V	-4	-2.8	0	LSB
Zero-Scale Error	Vwzse	Code = 00 _H , VDD = 5.5V	0	1.3	2	LSB
RESISTOR TERMINALS						
Voltage Range ⁷	$V_{A, B, W}$		0		VDD	V
Capacitance ⁸ Ax, Bx	Са, в	f =1MHz, Measured to GND, Code = 80н		75		pF
Capacitance Wx	Cw	f =1MHz, Measured to GND, Code = 80H		120		pF
DIGITAL INPUTS AND OUT		,				
Input Logic High	VIH	VDD = 5V	2.4			V
Input Logic Low	V _{IL}	VDD = 5V			0.8	V
Input Logic High	VIH	VDD = 3V	2.1		0.0	V
Input Logic Low	VIL	VDD = 3V			0.6	V
Input Current	IIH, IIL	V _{IN} = 5V or 0V, VDD = 5V			±1	μA
Input Capacitance	CIL	THE OF CLOV, VDD - SV		5		pF
POWER SUPPLIES	OIL			1 3		l bi
Power Supply Range	VDD		2.7		5.5	l v
Supply Current (CMOS)	IDD	V _{IH} = VDD or V _{IL} = 0V, VDD = 5.5V	2.1	0.1		-
				0.1	4	μA
Supply Current (TTL)9	IDD	V _{IH} = 2.4V or 0.8V, VDD = 5.5V		0.9	4	mA
Power Dissipation (CMOS) ¹⁰	P _{DISS}	V _{IH} = VDD or V _{IL} = 0V, VDD = 5.5V			27.5	μW
Power Supply Suppression	PSSR	$VDD = 5V + 0.5V_P$ AS1500, Version: 10kΩ		-54	-25	dB
Ratio	PSSK	sine wave @ 1kHz AS1501, Version: 20kΩ		-52	-25	dB
DYNAMIC CHARACTERIST	ICS ¹¹	3 1 1 1 1 1			ı	
Bandwidth –3dB	BW_10k	$R_{WB} = 10k\Omega$, $VDD = 5V$		1000		kHz
Bandwidth –3dB	BW_20k	$R_{WB} = 10k\Omega, VDD = 5V$ $R_{WB} = 20k\Omega, VDD = 5V$		500		kHz
Total Harmonic Distortion	THD _W			0.003		%
Total Harmonic Distortion	INDW	$V_A = 1V_{RMS} + 2V_{DC}$, $V_B = 2V_{DC}$, $f = 1kHz$		0.003		7/0
Vw Settling Time	ts_10k	R_{WB} = 5k Ω , V_A = VDD, V_B = 0V, ±1% Error Band		2		μs
Two Southing Time	ts_20k	R_{WB} = 10k Ω , V_A = VDD, V_B = 0V, ±1% Error Band		4		μs
D : (N :)/ !/	e _{NWB} _10k	$R_{WB} = 5k\Omega$, $f = 1kHz$		9		nV/ √ Hz
Resistor Noise Voltage			13		nV/ √ Hz	

Table 3: Electrical Characteristics – 10k and 20k Versions

³ Typicals represent average readings at 25°C and VDD = 5V.

⁴ Wiper is not connected. I_{AB} = 350μA for the 10kΩ version and 175μA for the 20kΩ version.

⁵ All Tempcos are guaranteed by design and not subject to production test.

⁶ Terminal A is not connected. I_W = 350μA for the 10kΩ version and 175μA for the 20kΩ version.

 $^{^{}m 7}$ Resistor terminals A, B, W have no limitations on polarity with respect to each other.

⁸ All capacitances are guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5V bias on the measured terminal. The remaining resistor terminals are left open circuit.

⁹ Worst-case supply current consumed when input logic level at 2.4V, standard characteristic of CMOS logic.

¹⁰ P_{DISS} is calculated from (IDD×VDD). CMOS logic level inputs result in minimum power dissipation.

¹¹ All dynamic characteristics are guaranteed by design and not subject to production test. All dynamic characteristics use VDD=5V.

AS1502 / AS1503 - SPECIFICATIONS

VDD = $3V\pm10\%$ or $5V\pm10\%$, V_A = VDD, V_B = 0V, $-40^{\circ}C \le T_A \le +125^{\circ}C$ unless otherwise noted.

ELECTRICAL CHARACTERISTICS – 50k and 100k VERSIONS

Parameter	Symbol	Con	Min	Typ ¹²	Max	Unit	
DC CHARACTERISTICS RI	HEOSTAT N	MODE					
	_	$T_A = 25^{\circ}C, VDD = 5V,$	AS1502, Version: 50kΩ	40	50	60	kΩ
Nominal Resistance ¹³	R _{AB}	$T_A = 25$ °C, VDD = 5V,	80	100	120	kΩ	
Resistance Tempco ¹⁴	$\Delta R_{AB}/\Delta T$	V _{AB} = VDD, Wiper = No			500		ppm/°C
Wiper Resistance	Rw	VDD = 5V		20	100	200	Ω
Resistor Differential NL ¹⁵	R-DNL	R_{WB} , $VDD = 5V$, $V_A = N$	No Connect	<u>-1</u>	±1/4	+1	LSB
Resistor Integral NL	R-INL	R_{WB} , $VDD = 5V$, $V_A = N$		-2	±1/2	+2	LSB
DC CHARACTERISTICS PO				_		_	
Resolution	N				8		Bits
1.1. 1.51 12 24	1811	VDD = 5.5V T _A = 25°C	,	-4	±1	+4	LSB
Integral Nonlinearity	INL	VDD = 2.7V T _A = 25°C		-4	±1	+4	LSB
B:# (: 1 N 1: ')	DAII	VDD = 5.5V T _A = 25°C		-1	±1/4	+1	LSB
Differential Nonlinearity	DNL	VDD = 2.7V T _A = 25°C		-1	±1/4	+1	LSB
Voltage Divider Tempco	ΔVw /ΔΤ	Code = 80 _H			15		ppm/°C
Full-Scale Error	V _{WFSE}	Code = FF _H , VDD = 5.	5V	-1	-0.25	0	LSB
Zero-Scale Error	Vwzse	Code = 00 _H , VDD = 5.5		0	0.1	1	LSB
RESISTOR TERMINALS	•	,					•
Voltage Range ¹⁶	Va, b, w			0		VDD	V
Capacitance ¹⁷ Ax, Bx	Са, в	f = 1MHz, Measured to	GND, Code = 80 _H		15		pF
Capacitance Wx	Cw	f = 1MHz, Measured to			80		pF
DIGITAL INPUTS AND OUT	TPUTS						
Input Logic High	V _{IH}	VDD = 5V		2.4			V
Input Logic Low	VIL	VDD = 5V				0.8	V
Input Logic High	V _{IH}	VDD = 3V		2.1			V
Input Logic Low	VIL	VDD = 3V				0.6	V
Input Current	lih, lil	V _{IN} = 5V or 0V, VDD =	5V			±1	μA
Input Capacitance	Cıl				5		pF
POWER SUPPLIES							
Power Supply Range	VDD			2.7		5.5	V
Supply Current (CMOS)	IDD	$V_{IH} = VDD$ or $V_{IL} = 0V$,			0.1	1	μΑ
Supply Current (TTL) ¹⁸	IDD	$V_{IH} = 2.4V \text{ or } 0.8V, VD$	D = 5.5V		0.9	4	mA
Power Dissipation	P _{DISS}	VIH = VDD or VIL = 0V,	VDD = 5.5V			27.5	μW
(CMOS) ¹⁹	1 0100	VIH - VDD OI VIL - OV,	- 3.57			21.5	·
Power Supply Suppression		VDD = 5V + 0.5V _P	AS1502, Version: $50k\Omega$		-43	tbd.	dB
Ratio	PSSR	sine wave @ 1kHz	AS1503, Version:		-48	tbd.	dB
		sine wave @ TKHZ 100kΩ			-40	tbu.	uБ
DYNAMIC CHARACTERIST					_		,
Bandwidth –3dB	BW_50k	$R_{WB} = 50k\Omega$, $VDD = 5$			220		kHz
Bandwidth –3dB	BW_100k			110		kHz	
Total Harmonic Distortion	THDw	V _A = 1V _{RMS} + 2V _{DC} , V _B = 2V _{DC} , f = 1kHz			0.003		%
$t_{S_{-}}50k$ RwB = $50k\Omega$, VA = VDD, VB = 0V, ±1% Error		O, V _B = 0V, ±1% Error		9		μs	
Vw Settling Time	ts_100k	R_{WB} = 100k Ω , V_A = VDD, V_B = 0V, ±1% Error Band			18		μs
	enwb_50k	$R_{WB} = 50k\Omega$, $f = 1kHz$			20		nV/ √ Hz
Resistor Noise Voltage	e _{NWB} _100	$R_{WB} = 100k\Omega$, $f = 1kH$	z		29		nV/ √ Hz

Table 4: Electrical Characteristics - 50k and 100k Versions

Page 4 of 8

¹² Typicals represent average readings at 25°C and VDD = 5V.

¹³ Wiper is not connected. I_{AB} = 70μA for the 50kΩ version and 35μA for the 100kΩ version.

¹⁴ All Tempcos are guaranteed by design and not subject to production test. ¹⁵ Terminal A is not connected. I_W = 70µA for the 50kΩ version and 35µA for the 100kΩ version.

¹⁶ Resistor terminals A, B, W have no limitations on polarity with respect to each other.

¹⁷ All capacitances are guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5V bias on the measured terminal. The remaining resistor terminals are left open circuit.

¹⁸ Worst-case supply current consumed when input logic level at 2.4V, standard characteristic of CMOS logic.

¹⁹ P_{DISS} is calculated from (IDD×VDD). CMOS logic level inputs result in minimum power dissipation.

²⁰ All dynamic characteristics are guaranteed by design and not subject to production test. All dynamic characteristics use VDD=5V.

AS150x - SPECIFICATIONS

(VDD = $3V\pm10\%$ or $5V\pm10\%$, VA = VDD, VB = 0V, $-40^{\circ}C \le TA \le +125^{\circ}C$ unless otherwise noted.)

ELECTRICAL CHARACTERISTICS-ALL VERSIONS

Parameter	Sym- bol	Conditions	Min	Typ 21	Max	Unit
SWITCHING CHARA	CTERIS	STICS 22, 23				
Input Clock Pulsewidth	tcн, tcL	Clock Level High or Low	50			ns
Data Setup Time	tos		5			ns
Data Hold Time	tон		5			ns
CSN Setup Time	tcss		10			ns
CSN High Pulsewidth	tcsw		10			ns
CK Fall to CSN Rise Hold Time	tcsh		0			ns
CSN Rise to Clock Rise Setup	tcs1		10			ns

Table 5: Switching Characteristics

Detailed Description

Serial-Programming

Programming of the AS150x is done via the 3 wire serial interface. The three input signals are serial data input (SDI), clock(CK) and chip select (CS). A programming sequence consists of 10-bit, where the last eight bit contain the code word for the resistor value. The first two bits A1 and A0 have to be low(see Table). The data is shifted into the internal 10 Bit register with the rising edge of the CK signal. With the rising edge of the CSN signal the data becomes valid and the resistance is updated (see figure 2). A detailed block diagram is shown in figure 3.

		D7	D6	D5	D4	D3	D2	D1	D0
0	0	MSB		Data					LSB

Table 6: Serial data format (16 bits)

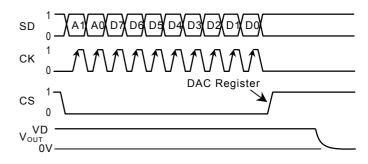


Figure 2: Timing Diagram

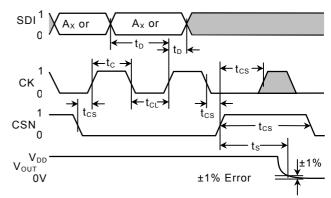


Figure 3: Detailed Timing Diagram

Rheostat Operation

The digital potentiometer family AS150x offers nominal resistor values of $10k\Omega$, $20~k\Omega$, $50k\Omega$ and $100k\Omega$. The resistor has 256 contact points where the wiper can access the resistor. The 8-bit code word determines the position of the wiper and is decoded through an internal logic. The lowest code 00h is related to the terminal B. The resistance is then only determined by the wiper resistance (100Ω) . The resistance for the next code 01h is the nominal resistor RAB ($10k\Omega$, $20 k\Omega$, $50k\Omega$ or $100k\Omega$) divided through 256 plus the wiper resistor. In case of AS1501 (10k Ω) the total resistance is $39\Omega + 100\Omega = 139\Omega$. Accordingly the resistor for code 02h is $78\Omega + 100\Omega = 178\Omega$. The last code 255h does not connect to terminal A directly (see Figure 5). So the maximum value is 10000Ω - 39Ω +100 Ω = 10061 Ω . The general formula for the calculation of the resistance RwB is:

 R_{WB} (Dx)= (Dx)/256· R_{AB} + R_{W}

where R_{AB} is the nominal resistance between terminal A and B, R_W is the wiper resistance and D_X is the 8-Bit Code word. In Table 7 the resistor values between the wiper and terminal B for AS1501 are given for specific codes D_X . In the zero-scale condition the wiper resistance of 100Ω remains present.

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²¹ Typicals represent average readings at 25°C and VDD=5V.

²² Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5V bias on the measured terminal. The remaining resistor terminals are left open circuit.

 $^{^{23}}$ See timing diagram for location of measured values. All input control voltages are specified with $t_{\rm R}$ = $t_{\rm F}$ = 1ns (10% to 90% of VDD) and timed from a voltage level of 1.6V. Switching characteristics are measured using VDD=3V or 5V. To avoid false clocking, a minimum input logic slew rate of 1V/ μs should be maintained

Dx (Dec)	$R_{WB}\left(\mathbf{\Omega}\right)$	Output State		
255	10061	Full Scale		
128	5100	Midscale		
1	139	1 LSB		
0	100	Zero-Scale (Wiper Contact Resistance)		

Table 7: RDAC-Codes WB

The maximum current through the wiper and terminal B is 5mA. If the current exceeds this limit the internal switches can degrade or even be damaged. As a mechanical potentiometer the resistance R_{WA} and R_{WB} are totally symmetrical. The relation between them is shown in Figure 4.

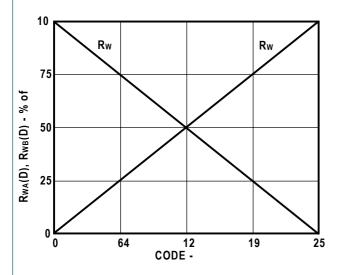


Figure 4: RwA and RwB versa Code

The resistance RWA is the complimentary resistor to RWB and can be controlled digitally as well. RWA starts at the maximum value of the nominal resistance and is reduced with increasing 8-Bit code words. The formula to calculate RWA is given below:

where R_{AB} is the nominal resistance between terminal A and B, R_{W} is the wiper resistance and D_{X} is the 8-Bit Code word. In Table 8 the resistor values between the wiper and terminal B for AS1501 are given for specific codes D_{X} .

Dx (Dec)	$R_{WA}(\Omega)$	Output State	
255	89	Full Scale	
128	5050	Midscale	
1	10011	1 LSB	
0	10050	Zero-Scale	

Table 8: RDAC-Codes WA

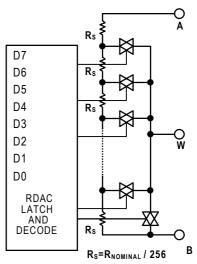


Figure 5: Equivalent RDAC Circuit

Voltage Output Operation

The AS150x family can easily used in an voltage output mode, where the output voltage is proportional to an applied voltage to a given terminal. When 5V are applied to terminal A and B is set to ground the ouput voltage at the wiper starts at zero volts up to 1LSB less then 5V. One LSB of voltage corresponds to the voltage applied at terminal AB divided through 256 steps of possible wiper settings. The formula is given by

$$V_W (Dx) = (Dx)/256 \cdot V_{AB} + V_B$$

where V_{AB} is the voltage applied between terminal A and B, V_{W} is the voltage at the wiper, D_{X} is the 8-Bit Code word and V_{B} is the voltage at terminal B. The temperature drift is significant better than in Rheostat mode, since the temperature coefficient is determined by the internal resistor ratio. Therefore the temperature drift is only $15ppm/^{\circ}C$.

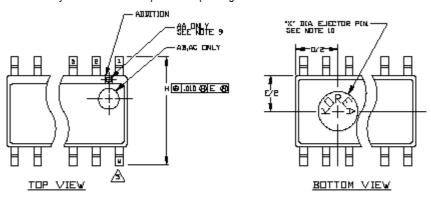
Applications

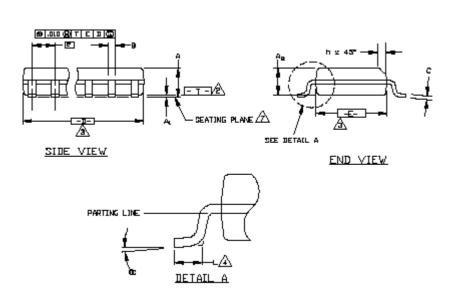
The digital potentiometer can replace in many applications the analog trimming potentiometer. The digital potentiometer is not sensitive to vibrations and shocks. It has an extremely small form-factor and can be adjusted very fast (e.g. AS1500 has an update rate of 600kHz) Furthermore the temperature drift, resolution and noise are significant better and cannot be achieved with a mechanical trimming potentiometer. Due to the programmability the resistor settings can be stored in the system memory, so that after a power down the exact settings can be recalled easily.

All analog signals must remain within 0 to VDD range. For standard potentiometer applications the wiper output can be used directly. In the case of a low impedance load a buffer shall be used.

Package Information

The AS150x family is offered in a 8-pin SOIC package:





- 🔼 DIMENSIONING & TOLERANCES PER ANSI,Y14.5M 1982.
- ⚠'T' IS A REFERENCE DATUM.
- 🕰 'D' & 'E' ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT
 DOES INCLUDE MOLD MISMATCH AND ARE MEASURED
 AT THE MOLD PARTING LINE, MOLD FLASH OR
 PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- <u>/S.</u> 'L' IS THE LENGTH OF TERMINAL FOR
- SOLDERING TO A SUBSTRATE.

 A "N" IS THE NUMBER OF TERMINAL POSITIONS.

- TERMINAL POSITIONS ARE SHOWN FOR
 REFERENCE ONLY.

 TORMED LEADS SHALL BE PLANAR WITH RESPECT TO
 ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
 THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL,
 ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR
 TYPE ON MATRIX LEADFRAME.

 TOPOTORY OF ORIGIN LOCATION AND EJECTOR
 PIN ON PACKAGE BOTTOM IS OPTIONAL AND
 DEPEND ON ASSEMBLY LOCATION.
- <u>∕IÀ</u> CONTROLLING DIMENSION: INCHES.

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Package Dimensions in Inch and mm (values for N = 8 Pin package are valid):

2		COMMON			NOTE		3		5
H	D.	<u>IMENSIO</u>	NS	No _T	VARI-		D		
밉밉	MIN.	NDM.	MAX.	T _E	ATIONS	MIN.	I N□M.	MAX.	
Α	.061	.064	.068		AΑ	.189	.194	.196	8
A_{t}	004،	.006	.0098		ΑВ	.337	.342	.344	14
Αe	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE	VARIATI	ONS	3					
E	.150	.155	.157						
6		.050 BSC							
H	.230	.236	.244						
[h	،010	013،	.016						
L	.016	.025	.035						
N	ZEE			5					
œ	O°	5	ů						
X	.085	.D93	100ء						

THIS TABLE IN MILLIMETERS

-									
17		COMMON			LNUTE		Э		5
H	D.	IMENSIO	NZ	"o_	VARI-		D		N
	MIN.	NDM.	MAX.	Τ _Ε	2NOITA	MIN.	I N□M.	MAX.	
Α	1,55	1.63	1.73		AA	4.80	4.93	4.98	l 8
Αι	0.127	0.15	0.25		AB	8.58	8,69	8,74	14
Αe	1,40	1,47	1,55		AC	9.80	9.93	9.98	16
В	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE	: VARIATI	:DNS	3					
LE	3.81	3,94	3,99						
6		1.27 BSC							
LH	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE			5					
8	°	້າ	8°						
X	2.16	2.36	2.54						

Ordering Information

Resistor	Pin Package	Delivery Form
10kΩ	8-pin SOIC	Tubes
20kΩ	8-pin SOIC	Tubes
50kΩ	8-pin SOIC	Tubes
100kΩ	8-pin SOIC	Tubes
10kΩ	8-pin SOIC	T&R
20kΩ	8-pin SOIC	T&R
50kΩ	8-pin SOIC	T&R
100kΩ	8-pin SOIC	T&R
	10kΩ 20kΩ 50kΩ 100kΩ 10kΩ 20kΩ 50kΩ	$\begin{array}{ccc} 10 k \Omega & 8\text{-pin SOIC} \\ 20 k \Omega & 8\text{-pin SOIC} \\ 50 k \Omega & 8\text{-pin SOIC} \\ 100 k \Omega & 8\text{-pin SOIC} \\ 10 k \Omega & 8\text{-pin SOIC} \\ 20 k \Omega & 8\text{-pin SOIC} \\ 50 k \Omega & 8\text{-pin SOIC} \\ \end{array}$

For Pb-free package use suffix '-Z'

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