

AS1751, AS1752, AS1753

High-Speed, Low-Voltage, Single-Supply, 0.9Ω, Quad SPST Analog Switches

Data Sheet

1 General Description

The AS1751/AS1752/AS1753 are high-speed, low-voltage, quad single-pole/single-throw (SPST) analog switches.

Fast switching speeds, low ON-resistance, and low power consumption make these devices ideal for single-cell battery powered applications.

These highly-reliable devices operate from a single +1.6 to +3.6V supply, and are differentiated by the type and number of switches:

- AS1751 – Four normally open (NO) switches
- AS1752 – Four normally closed (NC) switches
- AS1753 – Two NO switches and Two NC switches

The AS1753 supports break-before-make switching.

With very low ON-resistance (RON), RON matching and RON flatness, the devices can accurately switch signals for sample and hold circuits, digital filters, and op-amp gain switching networks.

The AS1751/AS1752/AS1753 digital logic input is 1.8V CMOS-compatible when using a +3V supply, and all devices can handle Rail-to-Rail signals.

The devices are available in a 3mm x 3mm 16-pin QFN package and a 14-pin TSSOP package.

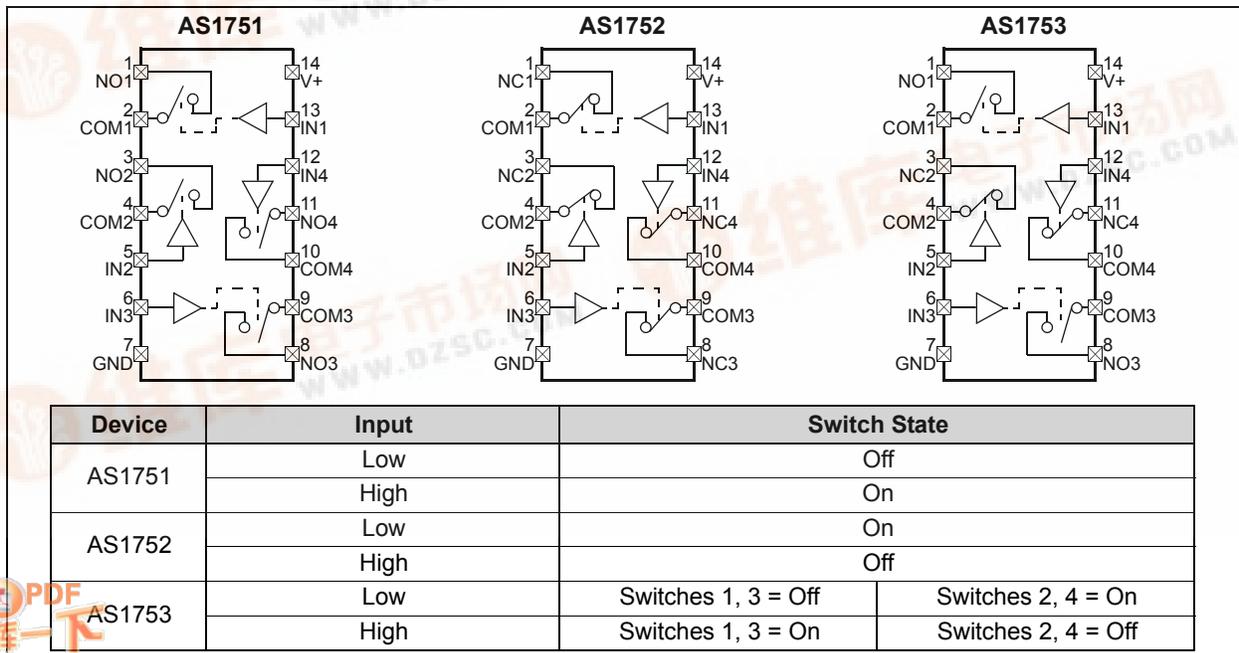
2 Key Features

- ON-Resistance:
 - 0.9Ω (+3V supply)
 - 2.5Ω (+1.8V supply)
- RON Matching:
 - 0.12Ω (+3V supply)
 - 0.25Ω (+1.8V supply)
- RON Flatness: 0.1Ω (+3V Supply)
- Supply Voltage Range: +1.6 to +3.6V
- Switching Speed: tON = 22ns, tOFF = 14ns
- Current-Handling: 250mA Continuous
- Break-Before-Make Switching (AS1753)
- Rail-to-Rail Signal Handling
- 1.8V CMOS Logic Compatible (+3V Supply)
- Operating Temperature Range: -40 to +85°C
- Package Types:
 - 16-pin QFN (3mm x 3mm)
 - 14-pin TSSOP

3 Applications

The devices are ideal for use in power routing systems, cordless and mobile phones, MP3 players, CD and DVD players, PDAs, handheld computers, digital cameras, hard drives, and any other application where high-speed signal switching is required.

Figure 1. 14-pin TSSOP Block Diagrams



4 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics on page 3 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V+, INx to GND	-0.3	+5	V	
COMx, NOx, NCx to GND †	-0.3	V+ + 0.3	V	
COMx, NOx, NCx Continuous Current	-250	+250	mA	
COMx, NOx, NCx Peak Current	-350	+350	mA	Pulsed at 1ms 10% duty cycle
Continuous Power Dissipation (T _{AMB} = +70°C)	16-pin QFN	727	mW	Derate at 9.1W/°C above +70°C
	14-pin TSSOP	1349		Derate at 16.9W/°C above +70°C
Operating Temperature Range	-40	+85	°C	
Electro-Static Discharge		2500	V	HBM Mil-Std883E 3015.7 methods
Latch Up Immunity		250	mA	Norm: JEDEC 17
Junction Temperature		+150	°C	
Storage Temperature Range	-65	+150	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"

† Signals on pins COM1, COM3, NO1, NO2, NC1, or NC2 that exceed V+ or GND are clamped by internal diodes. Forward-diode current should be limited to the maximum current rating.

5 Electrical Characteristics

Table 2. Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V+	Power Supply Range	T _{AMB} = T _{MIN} to T _{MAX}	1.6		3.6	V
I+	Positive Supply Current	V+ = 3.6V, V _{INx} = 0 or V+, T _{AMB} = +25°C			0.1	μA

V+ = +2.7 to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values @ V+ = +3.0V, T_{AMB} = +25°C.

Table 3. +3V Supply Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Analog Switch							
V _{COMx} , V _{NOx} , V _{NCx}	Analog Signal Range		0		V+	V	
R _{ON}	ON-Resistance	V+ = 2.7V, I _{COMx} = 100mA, V _{NOx} or V _{NCx} = 1.5V		0.4	0.9	Ω	
		T _{AMB} = +25°C			1		
ΔR _{ON}	ON-Resistance Match Between Channels ¹	V+ = 2.7V, I _{COMx} = 100mA, V _{NOx} or V _{NCx} = 1.5V		0.03	0.12	Ω	
		T _{AMB} = T _{MIN} to T _{MAX}			0.15		
R _{FLAT(ON)}	ON-Resistance Flatness ²	V+ = 2.7V, I _{COMx} = 100mA, V _{NOx} or V _{NCx} = 1, 1.5, or 2V		0.02	0.1	Ω	
		T _{AMB} = T _{MIN} to T _{MAX}			0.12		
I _{NOx(OFF)} , I _{NCx(OFF)}	NOx or NCx Off-Leakage Current	V+ = 3.6V, V _{COMx} = 0.3 or 3.6V, V _{NOx} or V _{NCx} = 3.6 or 0.3V			+2.5	nA	
		T _{AMB} = T _{MIN} to T _{MAX}	-2.5		+10		
I _{COMx(OFF)}	COMx Off-Leakage Current	V+ = 3.6V, V _{COMx} = 0.3 or 3.6V, V _{NOx} or V _{NCx} = 3.6 or 0.3V			+2.5	nA	
		T _{AMB} = T _{MIN} to T _{MAX}	-2.5		+10		
I _{COMx(ON)}	COMx On-Leakage Current	V+ = 3.6V, V _{COMx} = 0.3 or 3.6V, V _{NOx} or V _{NCx} = 0.3 or 3.6V			+2.5	nA	
		T _{AMB} = T _{MIN} to T _{MAX}	-2.5		+10		
Switch Dynamic Characteristics							
t _{ON}	Turn On Time ³	V _{NOx} or V _{NCx} = 1.5V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figures 11, 12			16	22	ns
		T _{AMB} = T _{MIN} to T _{MAX}				24	
t _{OFF}	Turn Off Time ³	V _{NOx} or V _{NCx} = 1.5V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figures 11, 12			5	14	ns
		T _{AMB} = T _{MIN} to T _{MAX}				15	
t _{BBM}	Break-Before-Make ³	V _{NOx} or V _{NCx} = 1.5V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figure 13 (AS1753)			11		ns
		T _{AMB} = T _{MIN} to T _{MAX}	2				
Q	Charge Injection	V _{GEN} = V+, R _{GEN} = 0, C _{LOAD} = 1.0nF, Figure 14			2		pC
C _{OFF}	NOx, NCx Off-Capacitance	f = 1MHz, Figure 15			45		pF
C _{COMx(OFF)}	COMx Off-Capacitance	f = 1MHz, Figure 15			49		pF
C _{COMx(ON)}	COMx On-Capacitance	f = 1MHz, Figure 15			85		pF

Table 3. +3V Supply Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VISO	Off-Isolation ⁴	f = 10MHz, RLOAD = 50Ω, CLOAD = 5pF, Figure 16		-40		dB
		f = 1MHz, RLOAD = 50Ω, CLOAD = 5pF, Figure 16		-55		
	Crosstalk ⁵	f = 10MHz, RLOAD = 50Ω, CLOAD = 5pF, Figure 16		-70		dB
		f = 1MHz, RLOAD = 50Ω, CLOAD = 5pF, Figure 16		-80		
THD	Total Harmonic Distortion	f = 20Hz to 20kHz, VCOMx = 2Vp-p, RLOAD = 32Ω		0.033		%
Logic Input						
VIH	Input Logic High		1.4			V
VIL	Input Logic Low				0.5	V
IIN	Input Leakage Current	VINx = 0 or V+	-1	0.0001	+1	μA

V+ = +1.8V, VIH = +1.0V, VIL = 0.4V, TAMB = TMIN to TMAX (unless otherwise specified). Typ values @ TAMB = +25°C.

Table 4. +1.8V Supply Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog Switch						
VCOMx, VNOx, VNCx	Analog Signal Range		0		V+	V
RON	ON-Resistance	V+ = 1.8V, ICOMx = 10mA, VNOx or VNCx = 0.9V	TAMB = +25°C	0.9	2.5	Ω
			TAMB = TMIN to TMAX		3	
ΔRON	ON-Resistance Match Between Channels ¹	V+ = 1.8V, ICOMx = 10mA, VNOx or VNCx = 0.9V	TAMB = +25°C	0.05	0.25	Ω
			TAMB = TMIN to TMAX		0.25	
Switch Dynamic Characteristics						
ton	Turn On Time ³	VNOx or VNCx = 1.0V, RLOAD = 50Ω, CLOAD = 35pF, Figures 11, 12	TAMB = +25°C	22	30	ns
			TAMB = TMIN to TMAX		35	
toff	Turn Off Time ³	VNOx or VNCx = 1.0V, RLOAD = 50Ω, CLOAD = 35pF, Figures 11, 12	TAMB = +25°C	12	20	ns
			TAMB = TMIN to TMAX		25	
Q	Charge Injection	VGEN = V+, RGEN = 0, CLOAD = 1.0nF, Figure 14		1		pC
Logic Input						
VIH	Input Logic High		1.0			V
VIL	Input Logic Low				0.4	V
IIN	Input Leakage Current	VINx = 0 or V+	-1	0.0001	+1	μA

1. ΔRON = RON(MAX) - RON(MIN).

2. Flatness is defined as the difference between the maximum and the minimum value of ON-resistance as measured over the specified analog signal ranges.

3. Guaranteed by design.

4. Off-Isolation = 20log10(VCOMx/VNOx), VCOMx = output, VNOx = input to off switch.

5. Between two switches.

6 Typical Operating Characteristics

Figure 2. Frequency Response

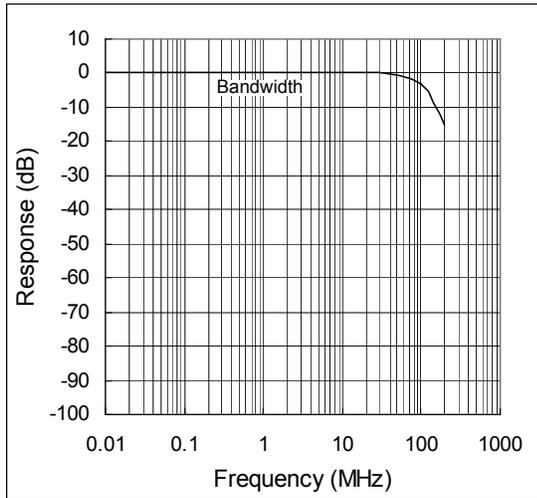


Figure 3. Total Harmonic Distortion vs. Frequency

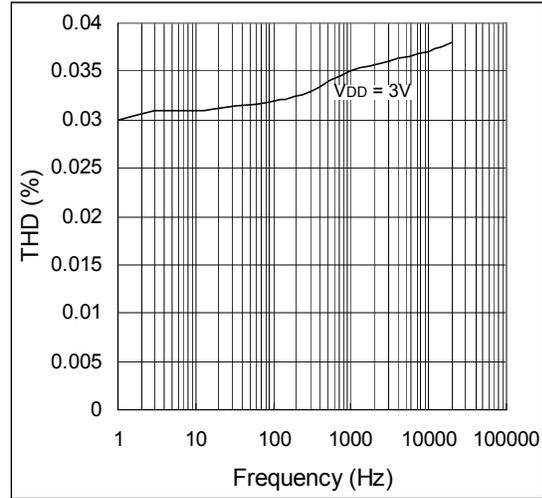


Figure 4. Turn On/Turn Off Time vs. Temperature

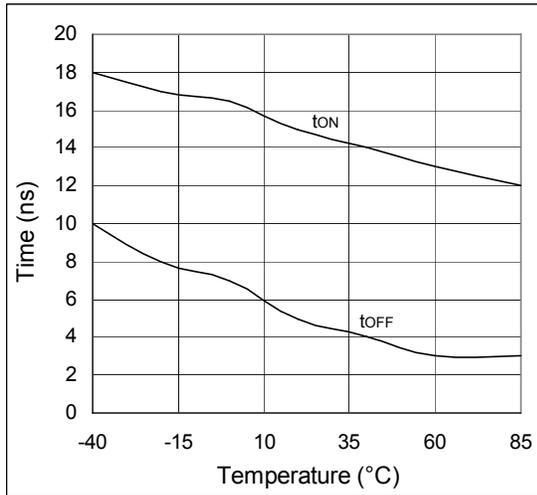


Figure 5. Turn On/Off Time vs. Supply Voltage

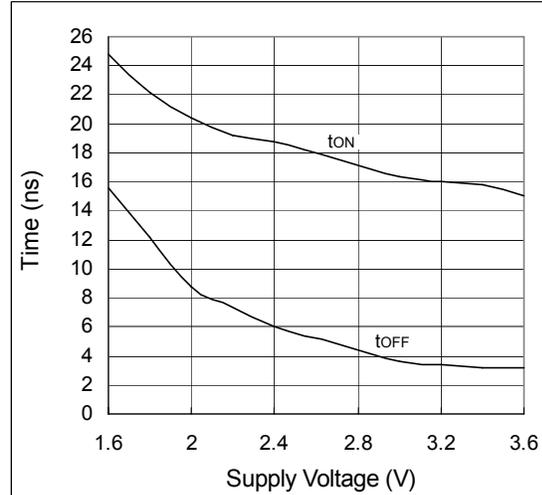


Figure 6. R_{ON} vs. V_{COM} and Temperature; V_{DD} = 2.7V

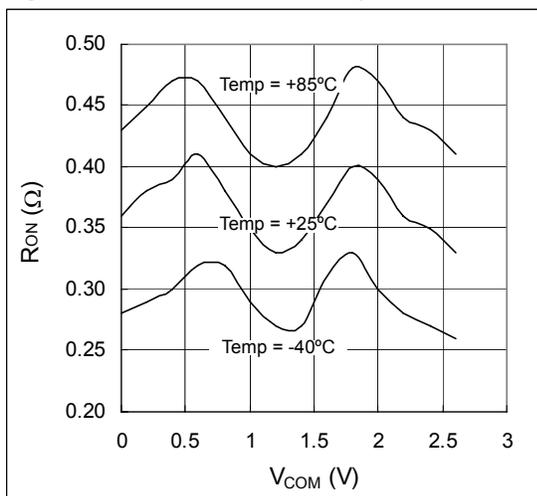


Figure 7. R_{ON} vs. V_{COM}

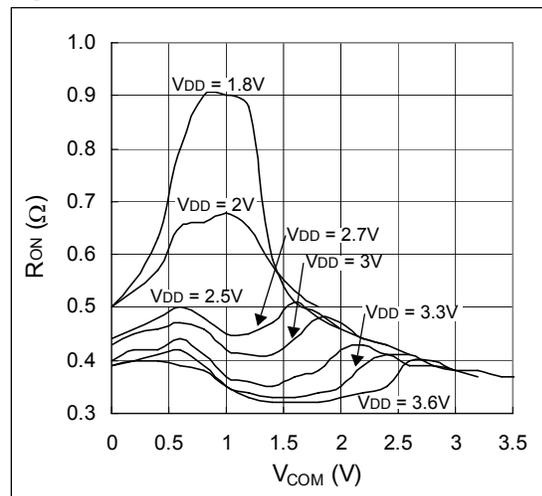
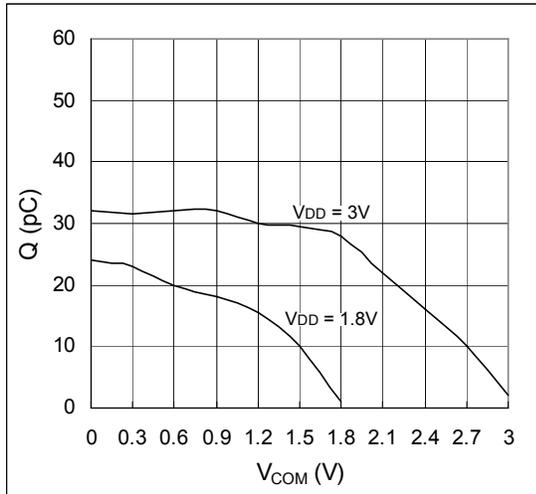


Figure 8. Charge Injection vs. V_{COM} 

7 Detailed Description

The AS1751/AS1752/AS1753 are low ON-resistance, low-voltage, quad analog SPST switches that operate from a single +1.6 to +3.6V supply.

CMOS process technology allows switching of analog signals that are within the supply voltage range (GND to V+).

Figure 9. 16-pin QFN Block Diagrams

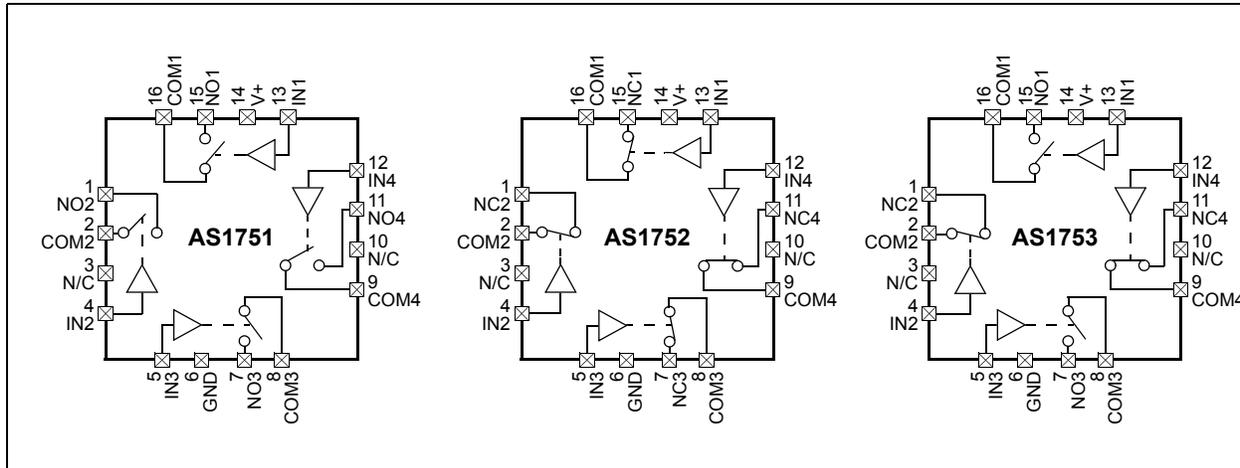


Table 5. Truth Tables

Device	Input	Switch State	
AS1751	Low	Off	
	High	On	
AS1752	Low	On	
	High	Off	
AS1753	Low	Switches 1, 3 = Off	Switches 2, 4 = On
	High	Switches 1, 3 = On	Switches 2, 4 = Off

ON-Resistance

When powered from a +3V supply, the low (0.9Ω, max) ON-resistance allows high-speed, continuous signals to be switched in a variety of applications.

Bi-Directional Switching

Pins NO_x, NC_x, and COM_x are bi-directional, thus they can be used as inputs to- or outputs from other components.

Analog Signal Levels

Analog signals ranging over the entire supply voltage range (V+ to GND) can be switched with very little change in ON-resistance (see Typical Operating Characteristics on page 5).

Logic Inputs

The devices' logic inputs can be driven up to +3.6V regardless of the supply voltage value. For example, with a +1.8V supply, IN_x may be driven low to GND and high to +3.6V. This allows the devices to interface with +3V systems using a supply of less than 3V.

8 Application Information

Power Supply Sequencing

Proper power-supply sequencing is critical for proper switch operation. The power supplies should be started up in the following sequence:

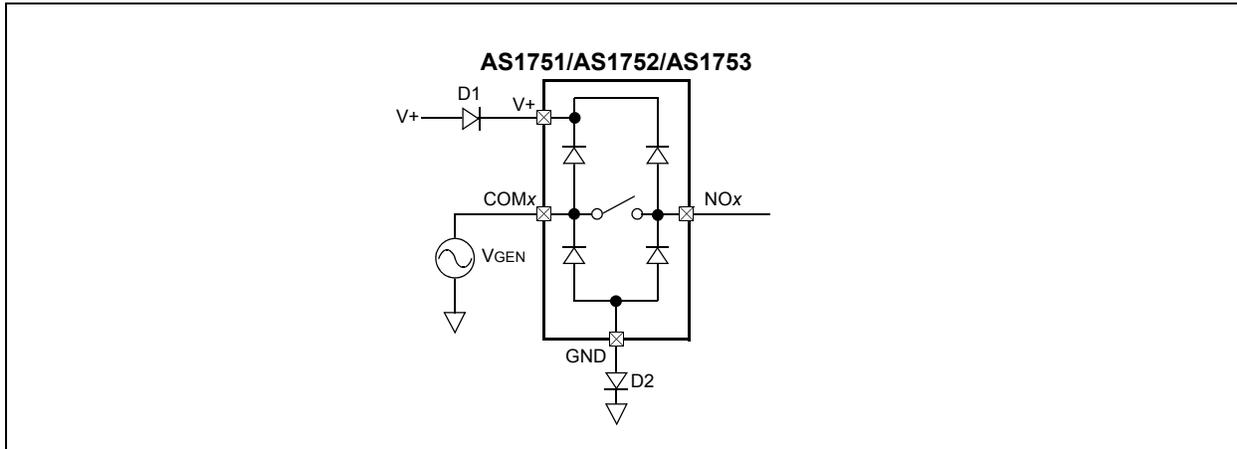
1. V+
2. NO_x, NC_x, COM_x

Note: Do not exceed the absolute maximum ratings (see page 2).

Overvoltage Protection

ON-resistance increases slightly at lower supply voltages.

Figure 10. Overvoltage Protection using 2 External Blocking Diodes



Adding diode D2 to the circuit shown in Figure 10 causes the logic threshold to be shifted relative to GND. Diodes D1 and D2 also protect against overvoltage conditions.

For example, in the circuit shown in Figure 10, if the supply voltage goes below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Power Supply Bypass

Power supply connections to the devices must maintain a low impedance to ground. This can be done using a bypass capacitor, which will also improve noise margin and prevent switching noise propagation from the V+ supply to other components.

A 0.1µF bypass capacitor, connected from V+ to GND (see Figure 16 on page 10), is adequate for most applications.

Logic Inputs

Driving IN_x Rail-to-Rail will help minimize power consumption.

Layout Considerations

High-speed switches require proper layout and design procedures for optimum performance.

- Short, wide traces should be used to reduce stray inductance and capacitance.
- Bypass capacitors should be as close to the device as possible.
- Large ground planes should be used wherever possible.

Timing Diagrams and Test Setups

Figure 11. AS1751/AS1753 Test Circuit and Timing Diagram

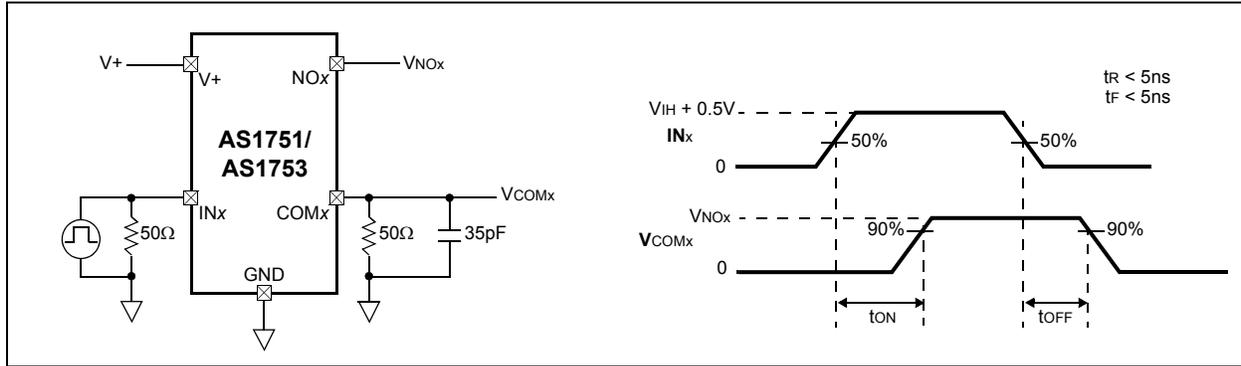


Figure 12. AS1752/AS1753 Test Circuit and Timing Diagram

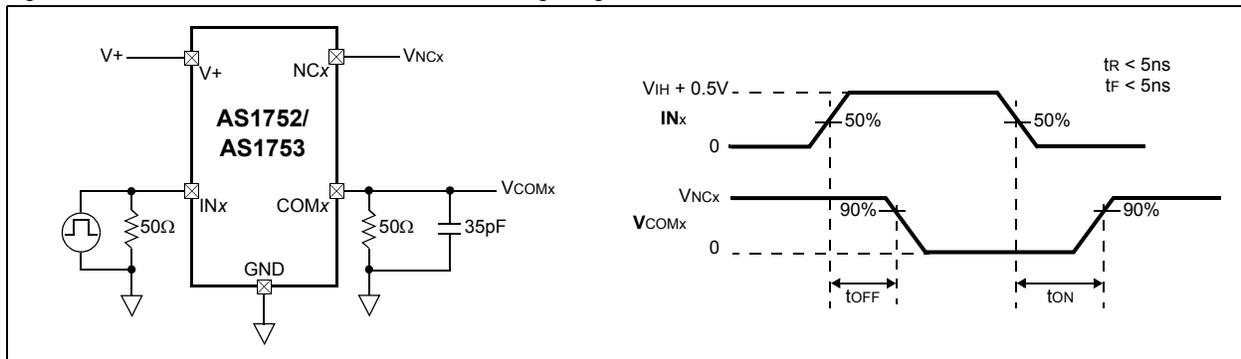


Figure 13. AS1753 Test Circuit and Timing Diagram

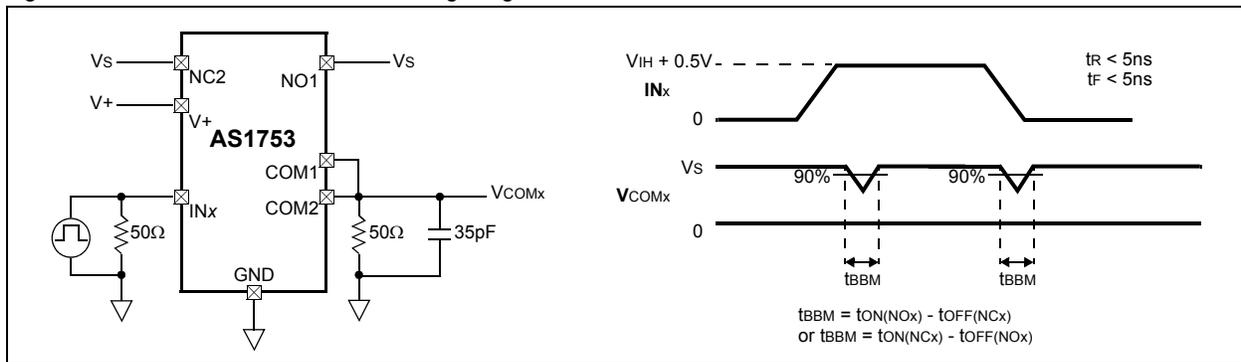


Figure 14. Charge Injection

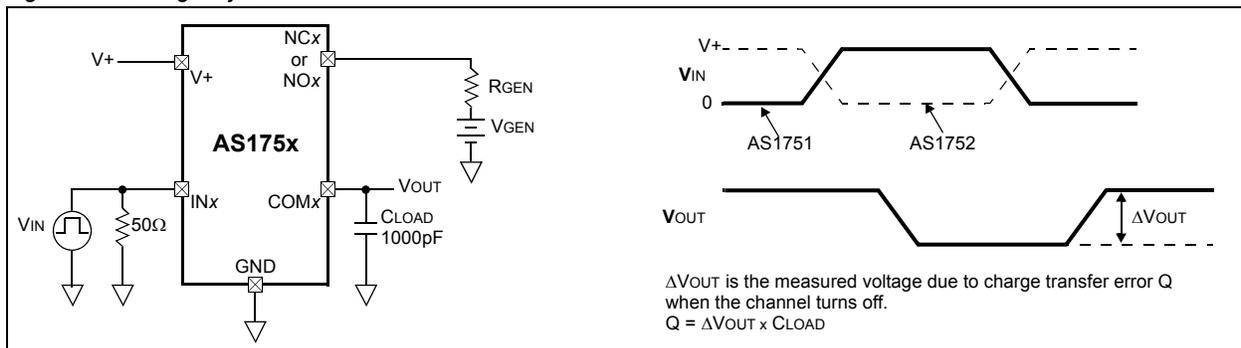


Figure 15. NOx, NCx, and COMx Capacitance

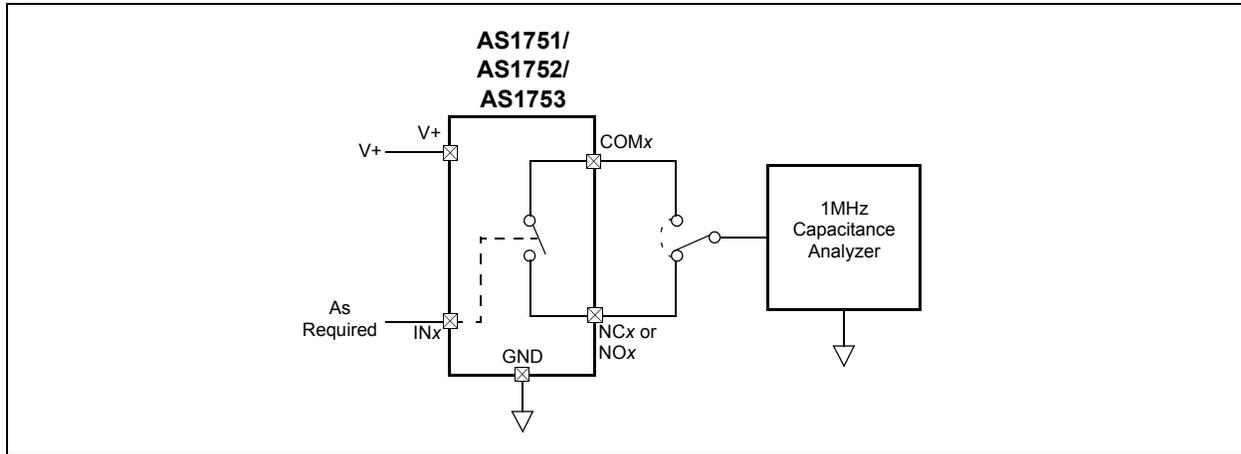
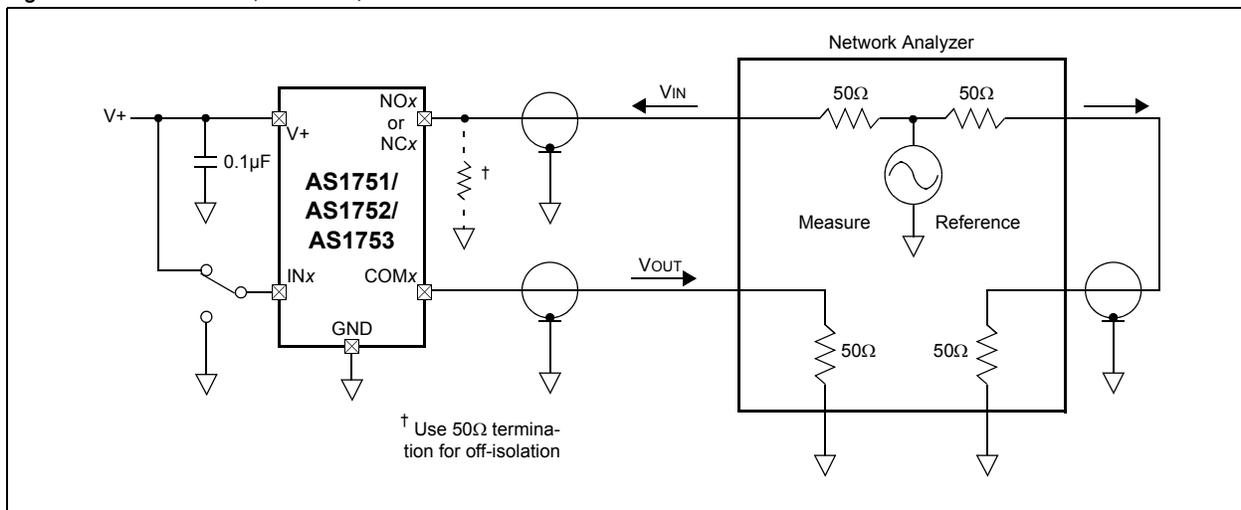


Figure 16. Off-Isolation, On-Loss, and Crosstalk



Notes:

1. Measurements are standardized against short-circuit at socket terminals.
2. Off-isolation is measured between COMx and the off NCx/NOx terminal on each switch. Off-isolation = $20\log(V_{OUT}/V_{IN})$.
3. On-loss is measured between COMx and the on NCx/NOx terminal on each switch. On-loss = $20\log(V_{OUT}/V_{IN})$.
4. Signal direction through the switch is reversed; worst values are recorded.

9 Pinout and Packaging

Pin Assignments

Figure 17. QFN Pin Assignments (Top View)

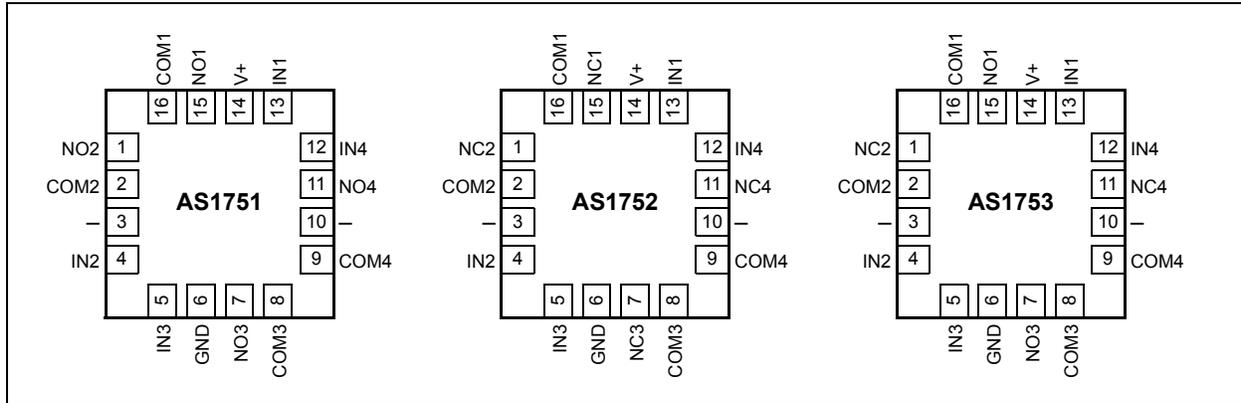
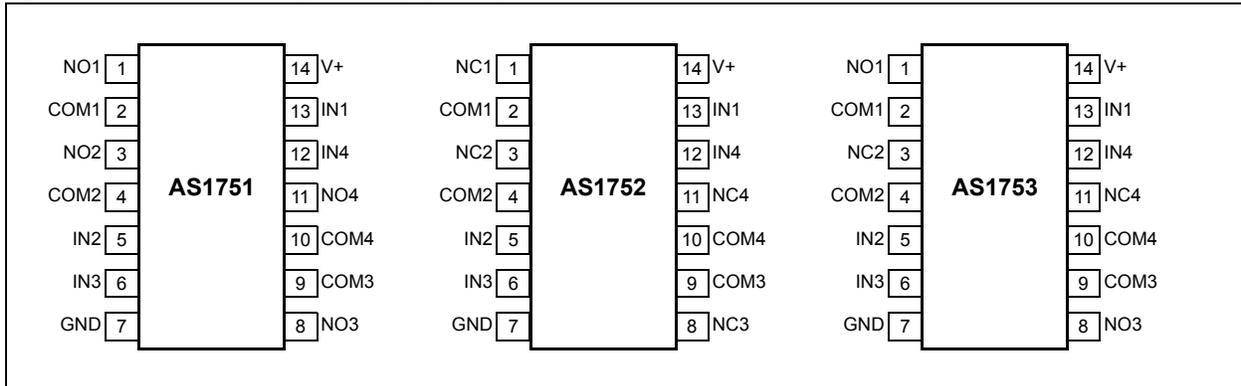


Figure 18. TSSOP Pin Assignments (Top View)



Pin Descriptions

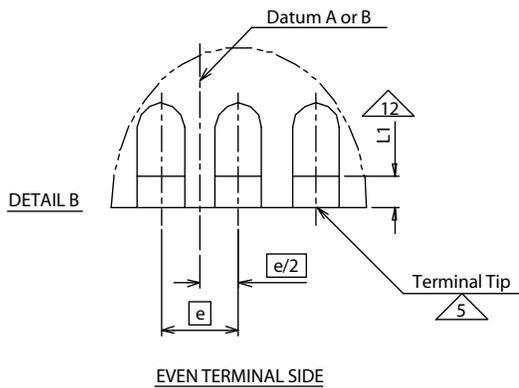
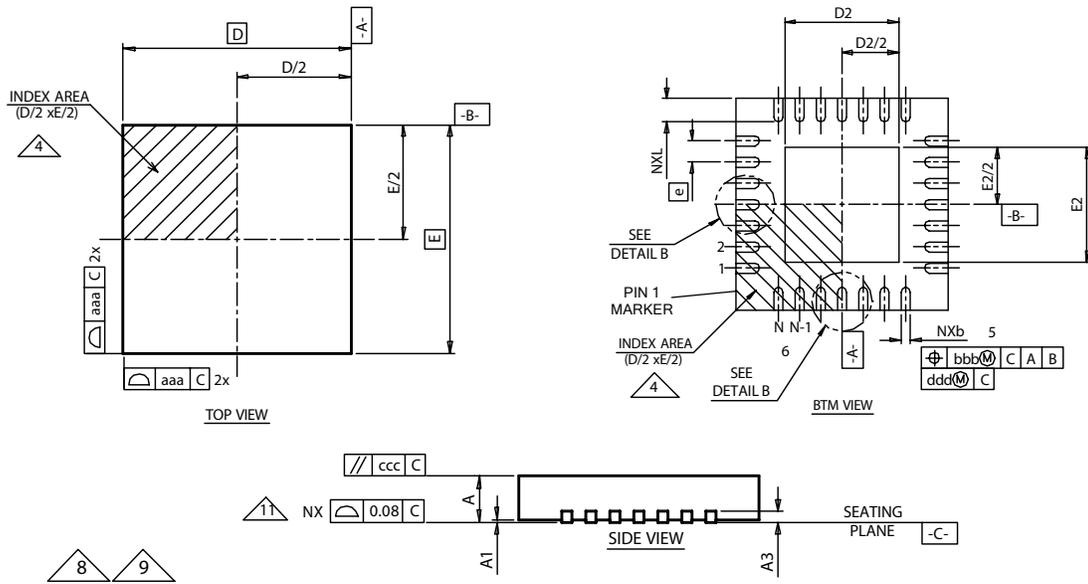
Table 6. Pin Descriptions

Pin Number	Pin Name	Description
(see Figure 17 and Figure 18)	COM1: COM4	Analog Switch 1, 2, 3, 4 Common
	GND	Ground
	IN1:IN4	Analog Switch 1, 2, 3, 4 Logic Control Input
	NC1:NC4	Analog Switch 1, 2, 3, 4 Normally Closed Terminal
	NO1:NO4	Analog Switch 1, 2, 3, 4 Normally Open Terminal
	V+	Input Supply Voltage, +1.6 to +3.6V

Package Drawings and Markings

The devices are available in an 16-pin QFN package and an 14-pin TSSOP package.

Figure 19. 16-pin QFN Package



Common Dimensions				
Symbol	Min	Nom	Max	Notes
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
L1	0.03		0.15	
D BSC		3.00		1, 2, 10
E BSC		3.00		1, 2, 10
D2	1.30	1.45	1.55	1, 2, 10
E2	1.30	1.45	1.55	1, 2, 10
L	0.30	0.40	0.50	1, 2, 10
N		16		1, 2, 10
ND		4		1, 2, 10
NE		4		1, 2, 10

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters; angles in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95 SPP-012*. Details of terminal #1 identifier are optional but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip. If one end of the terminal has the optional radius, the b dimension should not be measured in that radius area.
6. Dimensions ND and NE refer to the number of terminals on each D and E side, respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Figure 19 is shown for illustration only and does not represent any specific variation.
9. All variations may be constructed per Figure 19, however variations may alternately be constructed between square or rectangle shape per dimensions D and E.
10. Refer to the Dimensions Table for a complete set of dimensions.
11. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
12. Depending on the method of lead termination at the edge of the package, pullback (L1) may be present. L minus L1 to be $\geq 0.33\text{mm}$.
13. For variations with more than one lead count for a given body size and terminal pitch, each lead count for that variation is denoted by a dash number (e.g., -1 or -2).
14. NJR designates non-JEDEC registered package.

10 Ordering Information

The devices are available as the standard products shown in Table 7.

Table 7. Ordering Information

Part	Description	Delivery Form	Package
AS1751S	SPST Switch	Tube	14-TSSOP
AS1751S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1751V [†]	Quad SPST Switch	Tray	16-QFN 3mmx3mm
AS1751V-T [†]	Quad SPST Switch	Tape and Reel	16-QFN 3mmx3mm
AS1752S	Quad SPST Switch	Tube	14-TSSOP
AS1752S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1752V [†]	Quad SPST Switch	Tray	16-QFN 3mmx3mm
AS1752V-T [†]	Quad SPST Switch	Tape and Reel	16-QFN 3mmx3mm
AS1753S	Quad SPST Switch	Tube	14-TSSOP
AS1753S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1753V [†]	Quad SPST Switch	Tray	16-QFN 3mmx3mm
AS1753V-T [†]	Quad SPST Switch	Tape and Reel	16-QFN 3mmx3mm

[†] Future Product

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