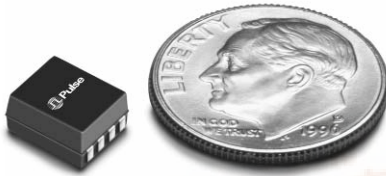


COMMON MODE CHOKE

For Fibre Channel, Gigabit Ethernet, and IEEE 1394 Applications



- Common Mode Attenuation from 200 MHz to 2.5 GHz
- Reduces radiated emissions and improves noise immunity
- 235°C Peak Reflow temperature rating
- Surface mount, auto-insertable package
- Industrial temperature range

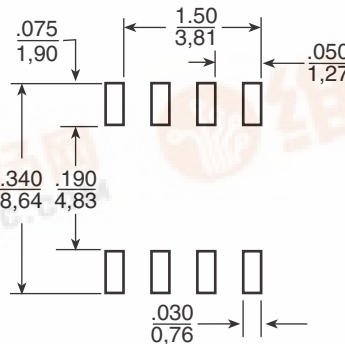
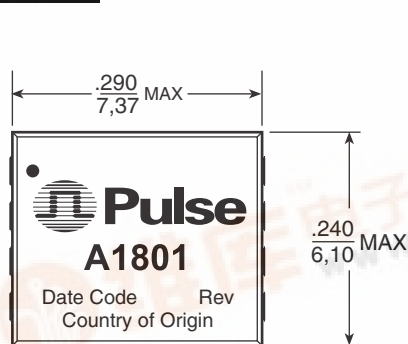
Electrical Specifications @ 25°C — Operating Temperature -40°C to +85°C

Part Number	Common Mode Attenuation (dB TYP)						Primary Inductance OCL (μH MIN)	DCR (Ω MAX)
	200 MHz	500MHz	1.0GHz	1.5GHz	2.0GHz	2.5GHz		
A1801	-11.0	-11.0	-11.0	-10.0	-9.0	-7.5	3.0	.15

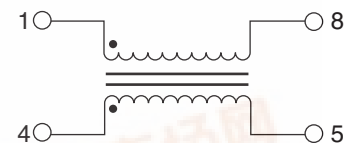
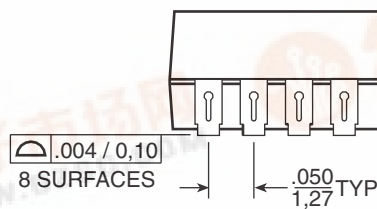
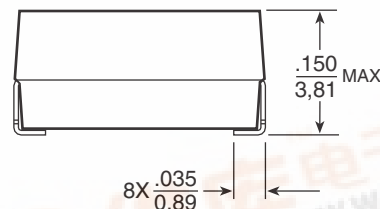
Mechanical

Schematic

A1801



SUGGESTED PAD LAYOUT



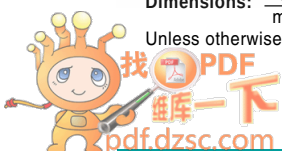
Dimensions: Inches
mm

Unless otherwise specified, all tolerances are ± .005
0.13

Weight0.2 grams (max)

Tape & Reel1750/reel

Tube80/tube



1. Values for R1 and R2 are determined by system transmit amplitude requirements. A value of 0Ω for R1 and R2 will yield an output with maximum amplitude but distorted due to impedance mismatch. A value of 68Ω will provide an optimum waveform but have 6.0 dB insertion loss. If 6.0dB loss is too great, select at least 15Ω to obtain a reasonable compromise between insertion loss and waveshape. The typical value for C1, C2, C3, and C4 is $0.1\mu\text{F}$.
2. To maintain return loss and signal integrity, transmission line methods must be used when designing the PCB. For best performance the common mode choke should be located no more than 1" from the cable connector.
3. One example of a possible layout is shown below for a Fibre Channel application. Note that actual board layouts will vary based upon specific applications and EMC considerations.

The diagram illustrates the electrical connection between a SerDes chip set and an HSDCC or DB9 connector. The SerDes chip set on the left provides TX+, TX-, RX-, and RX+ signals. The TX+ and TX- signals are connected to the non-inverting inputs of the top A1801 comparator through a network of resistors (R1, R2) and capacitors (C1, C2). The RX- and RX+ signals are connected to the non-inverting inputs of the bottom A1801 comparator through a network of resistors (R3, R4) and capacitors (C3, C4). Both comparators are configured with their inverting inputs to ground (GND) and their outputs to the HSDCC or DB9 connector (TX+, TX-, RX-, RX+). The comparators are powered by Vcc and GND. The HSDCC or DB9 connector on the right provides the TX+, TX-, RX-, and RX+ signals. The diagram also shows the connection to GND and EARTH GND, with a 75 Ω transmission line indicated for the RX- and RX+ signals.

The diagram shows a circuit for the second experiment. A dashed rectangular box is labeled "D.U.T." (Device Under Test). Inside this box, an inductor and a capacitor are connected in parallel. The inductor is represented by a series of loops, and the capacitor is represented by two parallel lines. This parallel combination is connected in series with a rectangular box labeled "75 Ω NETWORK ANALYZER". The circuit is completed by two vertical lines on the right side, which connect the top and bottom horizontal lines.

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