

CAST

C2901 4-bit Microprocessor Slice Megafunction

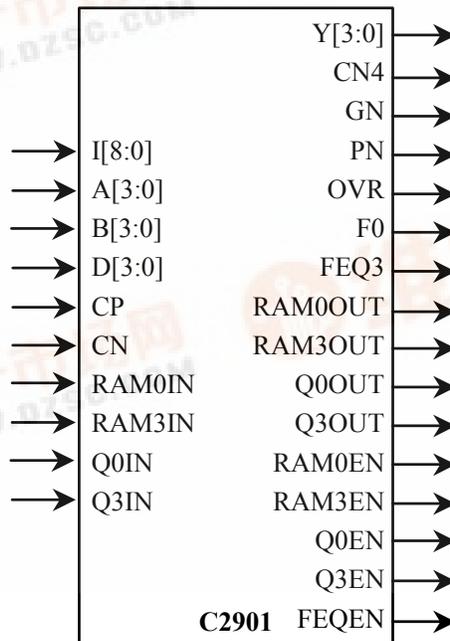
General Description

The C2901 four-bit microprocessor slice megafunction is a cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The megafunction includes a dual port RAM, ALU, shifter, register and multiplexer. The microinstructions of the C2901 allow for easy modeling of various microcontrollers.

Features

- Independent and simultaneous access to two registers save machine cycles
- Eight function ALU
- Expandable – Any number of devices can be connected for wider bus structures
- Four status flags for Carry, Overflow, Zero and Negative
- Microprogrammable
- The C2901 was developed in HDL and synthesizes to approximately 1,300 gates depending on the technology used.
- Functionality based on the Advanced Micro Devices AM2901

Symbol



Pin Description

| Name | Type | Description |
|---------|--------|--|
| CP | Input | Clock |
| I[8:0] | Input | Instruction/Microcode |
| D[3:0] | Input | Data Input |
| A[3:0] | Input | A-port Address |
| B[3:0] | Input | B-port Address |
| CN | Input | Carry In |
| Q0IN | Input | Shift Line – Q Register |
| RAM0IN | Input | Shift Line – RAM Stack |
| Q3IN | Input | Shift Line – Q Register |
| RAM3IN | Input | Shift Line – RAM Stack |
| Y[3:0] | Output | Data Output |
| GN | Output | Carry Generate |
| PN | Output | Carry Propagate |
| OVR | Output | Overflow |
| F0 | Output | ALU outputs are zero |
| F3 | Output | ALU MSB |
| CNP4 | Output | Carry out |
| Q0OUT | Output | Shift Line – Q Register |
| RAM0OUT | Output | Shift Line – RAM Stack |
| Q3OUT | Output | Shift Line – Q Register |
| RAM3OUT | Output | Shift Line – RAM Stack |
| FEQEN | Output | ALU outputs are zero (control for Open Collector Output) |
| Q0EN | Output | Enable for Q0 Tristate Output |
| Q3EN | Output | Enable for Q3 Tristate Output |
| RAM0EN | Output | Enable for RAM0 Tristate Output |
| RAM3EN | Output | Enable for RAM3 Tristate Output |

Functional Description

This section describes the Block Diagram below. A description of each of the blocks in the diagram is given here.

Dual Port RAM

The internal memory is a 4 bit by 16 Dual Port RAM. It is addressed for writing by the B Port and for reading by both the A and B Ports. The input data is defined by a microinstruction decoded from 3 bits of the 9-bit I Port.

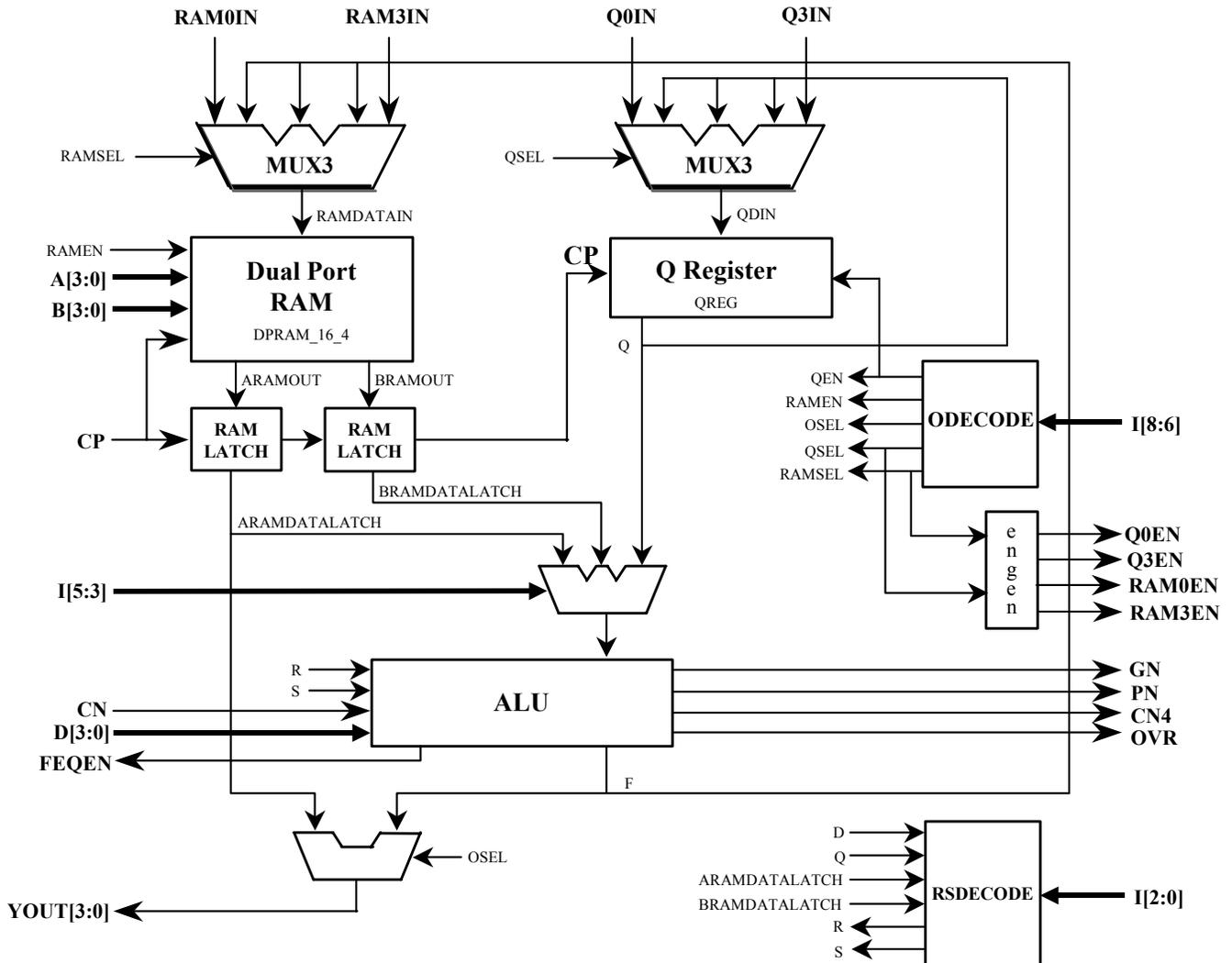
RAM Latch

These latches store the outputs of the Dual Port RAM. They are clocked using the CP input.

Q Register

This section describes the internal register. It is selected using the Instruction input (I) and clocked with the CP input.

Block Diagram



MicroInstructions

The I Port is internally decoded to define the flow of data to the above sections.

ALU

The ALU accepts input from either RAM Port, the Q Register and cascaded inputs from previous stages. It has basic functions including most logic and arithmetic operations including such functions as shifting, adding and subtracting.

ODecode

The ODecode block takes bits 6 – 8 of the MicroInstruction Bus and uses them to control the internal output enables and selects of the other blocks.

RSDecode

The RSDecode block takes bits 0 – 2 of the MicroInstruction Bus and uses them to control the 4-bit R and S buses. These buses get loaded with the outputs of the other blocks, routing various results back through the ALU block

ENGEN

This block takes the select bits for the ram and q register and decodes the enable pins for the bi-directional RAM and Q bits.

MicroInstructions

The I Port is internally decoded to define the flow of data to the above sections.

Device Utilization & Performance

| Supported Family | Device Tested | Utilization | | | Performance |
|------------------|---------------|-------------|--------|-------------|------------------|
| | | LEs | Memory | Memory bits | F _{max} |
| Cyclone | EP1C20-6 | 273 | 0 | 0 | 28 MHz |
| Stratix | EP1S20-5 | 273 | 0 | 0 | 30 MHz |
| Stratix-II | EP2S60-3 | 206 | 0 | 0 | 41 MHz |

Deliverables

Encrypted Netlist License

- Post synthesis EDIF netlist
- Assignment & Configuration
- Symbol & Include files
- Testbench
- Vectors for testing the functionality of the megafunction
- Place & Route Scripts
- Documentation

HDL Source License

- VHDL or Verilog RTL source code
- Testbenches
- Vectors for testing functionality
- Expected results
- Synthesis scripts
- Simulation scripts
- Documentation

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