# Low Voltage, 0.4 Ω, Dual SPDT Analog Switch

## DESCRIPTION

The DG2731/2732/2733 are low voltage, low on-resistance, dual single-pole/double-throw (SPDT) monolithic CMOS analog switches designed for high performance switching of analog signals. Combining low-power, high speed, low on-resistance, and small package size, the DG2731/2732/2733 are ideal for portable and battery power applications.

The DG2731/2732/2733 have an operation range from 1.6 V to 4.3 V single supply. The DG2731 and DG2732 have two separate control pins with reverse control logic. The DG2733 has an EN pin to enable the device when the logic is high.

The DG2731/2732/2733 are 1.6-V logic compatible, allowing the easy interface with low voltage DSP or MCU control logic and ideal for one cell Li-ion battery direct power.

The switch conducts signals within power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.

The DG2731/2732/2733 are built on Vishay Siliconix's sub micron CMOS low voltage process technology and provides greater than 300 mA latch-up protection, as tested per JESD78.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG2731/2732/2733 are offered in a DFN or MSOP package. The DFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The MSOP package uses 100% matte Tin device termination and is represented by the lead (Pb)-free "-E3" suffix. Both the matte Tin and nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

## FEATURES

- Low Voltage Operation (1.65 V to 4.3 V)
- Low On-Resistance - $r_{ON}$: 0.3 Ω@ 3.6 V
- Fast Switching: $T_{ON}$ = 50 ns @ 4.3 V
- $T_{OFF}$ = 14 ns @ 4.3 V
- Latch-Up Current > 300 mA (JESD78)

Pb-free
RoHS COMPLIANT

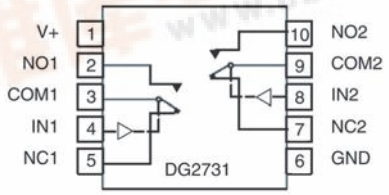
## BENEFITS

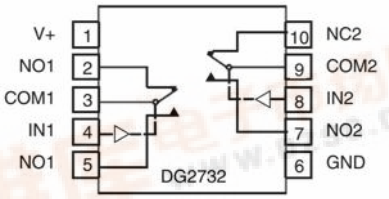
- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.6-V Logic Compatible

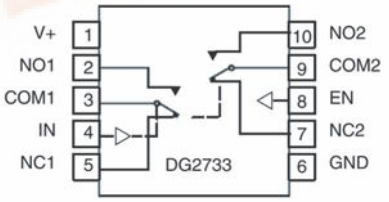
## APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE | | | |
|---|---|---|---|
| **Logic** | **EN (DG2733 only)** | **NC1, 2** | **NO1, 2** |
| 0 | 1 | ON | OFF |
| 1 | 1 | OFF | ON |
| 0 | 0 | OFF | OFF |
| 1 | 0 | OFF | OFF |

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp Range** | **Package** | **Part Number** |
| –40 to 85°C | MSOP–10 | DG2731DQ–T1–E3<br>DG2732DQ–T1–E3<br>DG2733DQ–T1–E3 |
| | DFN–10 | DG2731DN–T1–E4<br>DG2732DN–T1–E4<br>DG2733DN–T1–E4 |

| ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Reference to GND | V+ | | –0.3 to 5.0 | V |
| | IN, COM, NC, NO[a] | | –0.3 to ($V^+$ + 0.3) | |
| Current (Any terminal except NO, NC or COM) | | | 30 | mA |
| Continuous Current (NO, NC, or COM) | | | ±250 | |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | | | ±500 | |
| Storage Temperature (D Suffix) | | | –65 to 150 | °C |
| Package Solder Reflow Conditions[d] | 10–PIN MSOP | | | |
| | 10–PIN DFN | | | |
| Power Dissipation (Packages)[b] | MSOP–10[c] | | 320 | mW |
| | DFN–10[d] | | 1191 | |

Notes

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 4.0 mW/C above 70°C

d. Derate 14.9 mW/C above 70°C

e. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

| SPECIFICATIONS (V+ = 1.8 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition Otherwise Unless Specified** V+ = 1.8 V, $V_{IN}$ = 0.4 or 1.4 V[e] | **Temp[a]** | **Limits –40 to 85°C Min[b]** | **Typ[c]** | **Max[b]** | **Unit** |
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $r_{ON}$ | V+ = 1.8 V, $V_{COM}$ = 0.9 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.7 | 1.0 | Ω |
| | | | Full | | | 1.2 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{INH}$ | | Full | 1.4 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.4 | |
| Input Capacitance | $C_{in}$ | | Full | | 4 | | pF |
| **Power Supply** | | | | | | | |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | Full | | | 1.0 | µA |

## SPECIFICATIONS (V+ = 3 V)

| Parameter | Symbol | Test Condition Otherwise Unless Specified V+ = 3 V, ±10 %, $V_{IN}$ = 0.5 or 1.4 V[e] | Temp[a] | Limits –40 to 85°C Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $r_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 0.5 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.35 | 0.45 | Ω |
| | | V+ = 2.7 V, $V_{COM}$ = 1.5 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.3 | | |
| | | | Full | | | 0.6 | |
| $r_{ON}$ Match[d] | $\Delta r_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 0.5 to 1.5 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.03 | 0.06 | |
| Switch Off Leakage Current | $I_{NO(off)}$, $I_{NC(offF)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$ = 0.3 V / 4.0 V, $V_{COM}$ = 3.0 V / 0.3 V | Room<br>Full | –1<br>–10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | –1<br>–10 | | 1<br>10 | |
| Channel-On Leakage Current | $I_{COM(on)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 3.0 V / 0.3 V | Room<br>Full | –1<br>–10 | | 1<br>10 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{INH}$ | | Full | 1.4 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.5 | |
| Input Capacitance | $C_{in}$ | | Full | | 5 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | –1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | V+ = 3.6 V $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room<br>Full | | 85 | 110<br>140 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 17 | 30<br>35 | |
| Break-Before-Make Time | $t_{BBM}$ | | Full | 10 | | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 9 | | pC |
| Off-Isolation[d] | $O_{IRR}$ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz | Room | | –75 | | dB |
| Crosstalk[d] | $X_{TALK}$ | | Room | | –75 | | |
| $N_O$, $N_C$ Off Capacitance[d] | $C_{NO(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | Room | | 104 | | pF |
| | $C_{NC(off)}$ | | Room | | 104 | | |
| Channel On Capacitance[d] | $C_{NO(on)}$ | | Room | | 230 | | |
| | $C_{NC(on)}$ | | Room | | 230 | | |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | | | 2.7 | | 3.3 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | Full | | | 1.0 | µA |
| Turn-On Time DG2733 (EN) | $t_{ON(EN)}$ | V+ = 3.6 V $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room<br>Full | | 79 | 105<br>135 | ns |
| Turn-Off Time DG2733 (EN) | $t_{OFF(EN)}$ | | Room<br>Full | | 17 | 29<br>35 | |

## SPECIFICATIONS (V+ = 4.3 V)

| Parameter | Symbol | Test Condition Otherwise Unless Specified V+ = 4.3 V, $V_{IN}$ = 0.5 or 1.6 V[e] | Temp[a] | Limits –40 to 85°C Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $r_{ON}$ | V+ = 4.3 V, $V_{COM}$ = 0.9 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.29 | 0.4 | Ω |
| | | V+ = 4.3 V, $V_{COM}$ = 2.5 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.21 | | |
| | | | Full | | | 0.55 | |
| $r_{ON}$ Match[d] | $\Delta r_{ON}$ | V+ = 4.3 V, $V_{COM}$ = 0. 9 to 2.5 V+, $I_{NO}$, $I_{NC}$ = 100 mA | Room | | 0.03 | 0.06 | |
| Switch Off Leakage Current[d] | $I_{NO(off)}$, $I_{NC(off)}$ | V+ = 4.3 V, $V_{NO}$, $V_{NC}$ = 0.3 V / 4.0 V, $V_{COM}$ = 4.0 V / 0.3 V | Full | –20 | | 20 | nA |
| | $I_{COM(off)}$ | | Full | –20 | | 20 | |
| Channel-On Leakage Current[d] | $I_{COM(on)}$ | V+ = 4.3 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 3.0 V / 4.0 V | Full | –20 | | 20 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{IN}$ | | Full | 1.6 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.5 | |
| Input Capacitance | $C_{in}$ | | Full | | –4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | –1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Break-Before-Make Time | $t_{BBM}$ | $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Full | 5 | | | ns |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | | | | | 4.3 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | Full | | | 1.0 | µA |

Notes

a. Room = 25°C, Full = as determined by the operating suffix.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

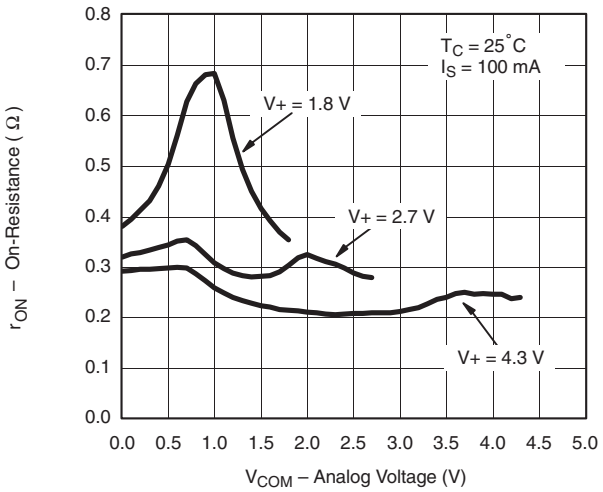
c. Typical values are for design aid only, not guaranteed nor subject to production testing.

d. Guarantee by design, not subjected to production test.

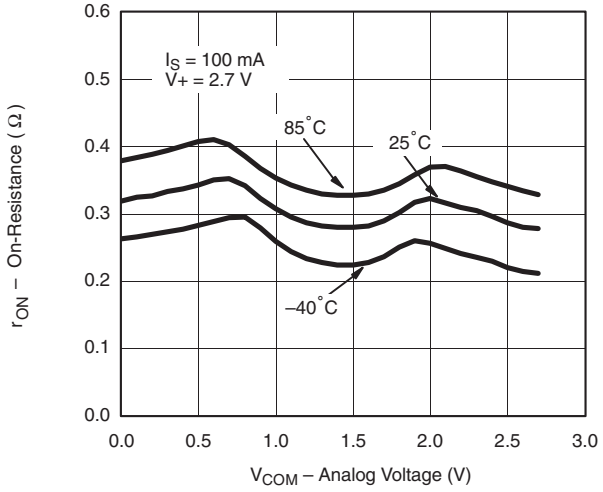
e. $V_{IN}$ = input voltage to perform proper function.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

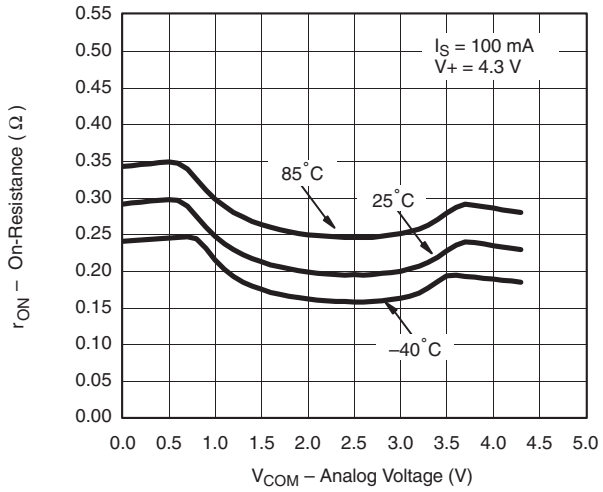
## TYPICAL CHARACTERISTICS $T_A$ = 25 °C, unless otherwise noted



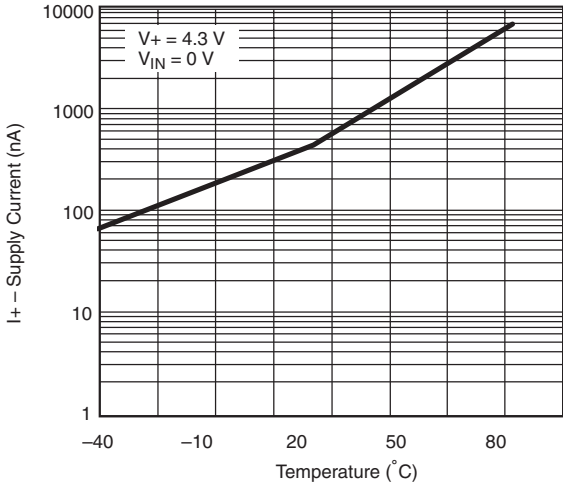

**$r_{ON}$ vs. $V_{COM}$ and Supply Voltage**



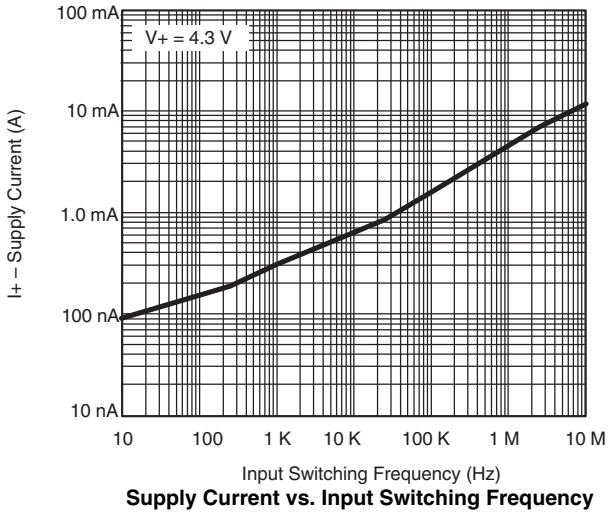

**$r_{ON}$ vs. Analog Voltage and Temperature**



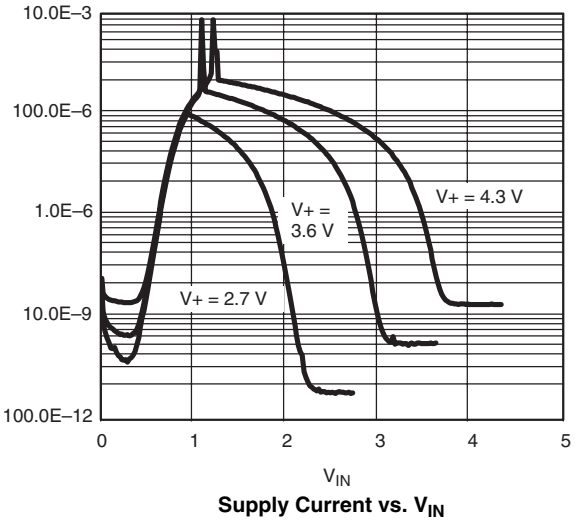

**$r_{ON}$ vs. Analog Voltage and Temperature**




**Supply Current vs. Temperature**

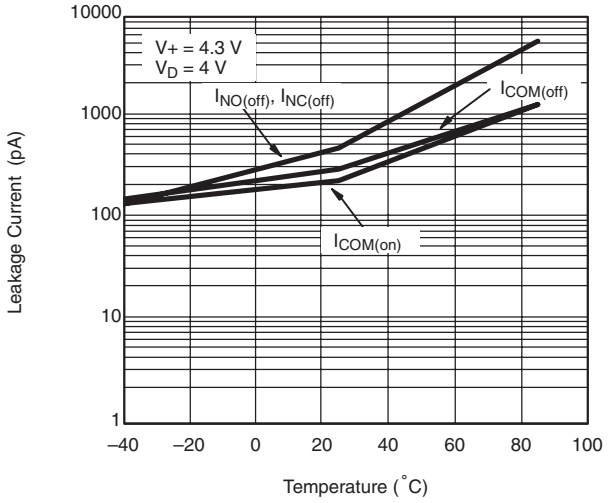



**Supply Current vs. Input Switching Frequency**

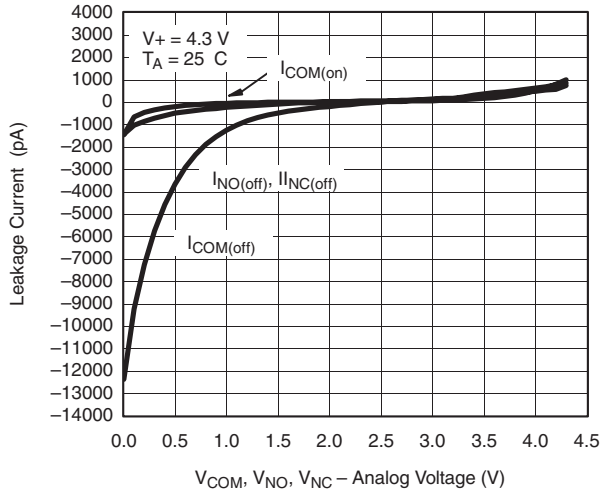



**Supply Current vs. $V_{IN}$**

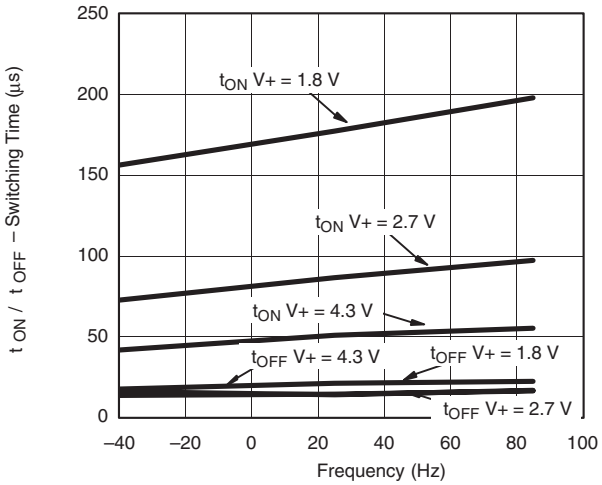
## TYPICAL CHARACTERISTICS $T_A$ = 25 °C, unless otherwise noted



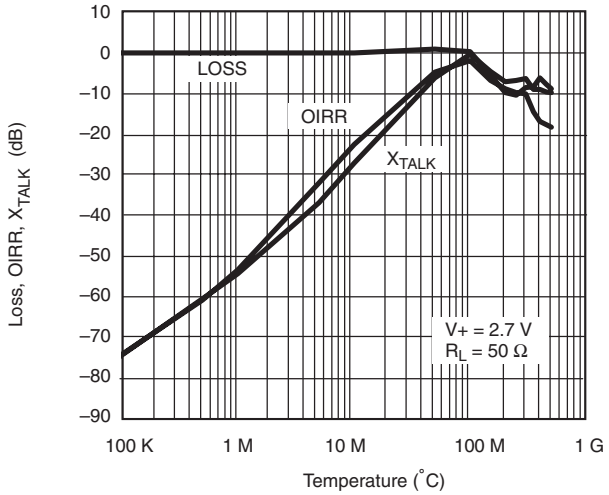

**Leakage Current vs. Temperature**



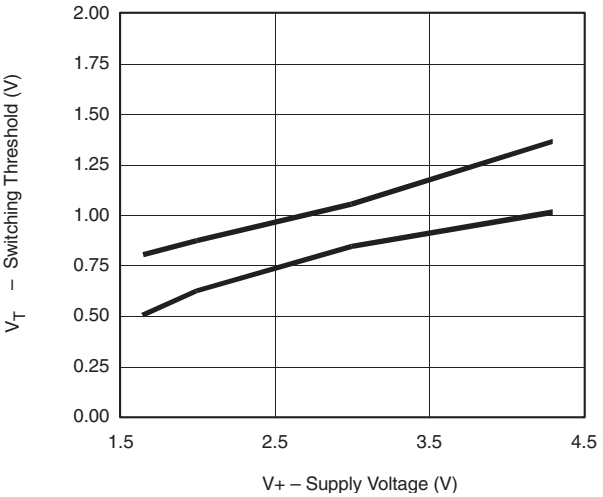

**Leakage vs. Analog Voltage**



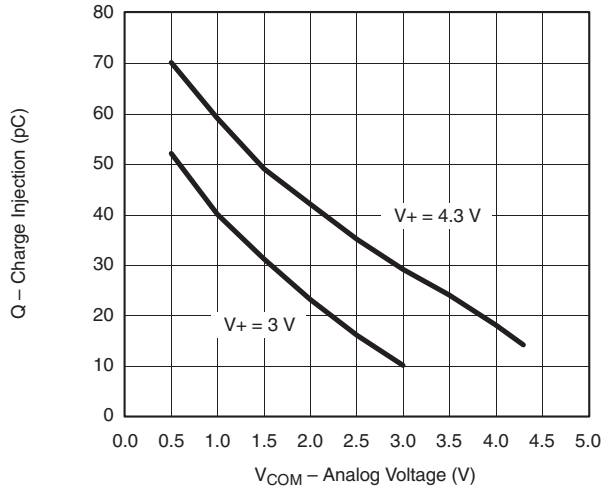

**Switching Time vs. Temperature**




**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

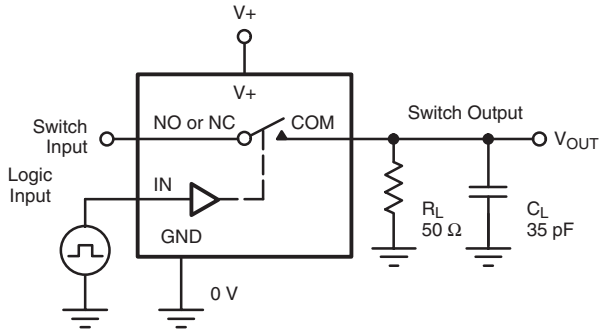



**Switching Threshold vs. Supply Voltage**



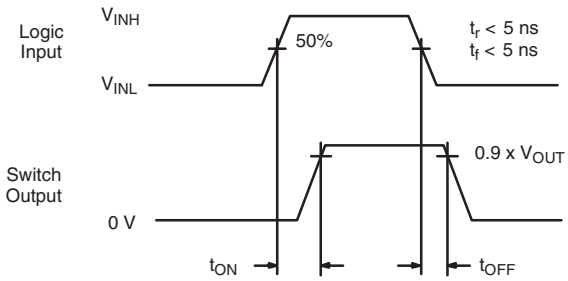

**Charge Injection vs. Analog Voltage**

## TEST CIRCUITS



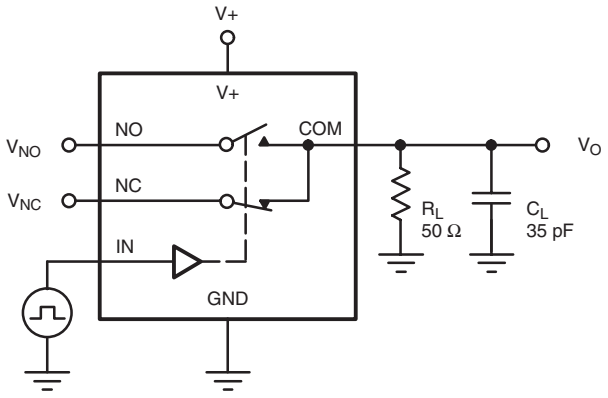

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Figure 1. Switching Time**




$C_L$ (includes fixture and stray capacitance)

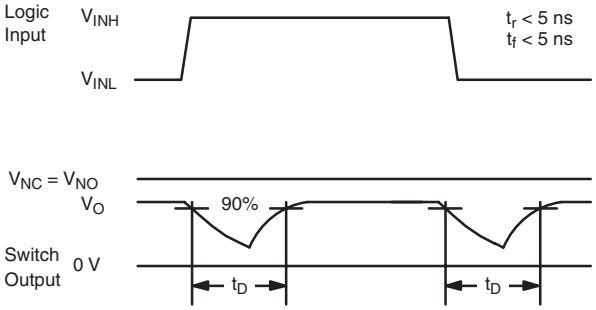
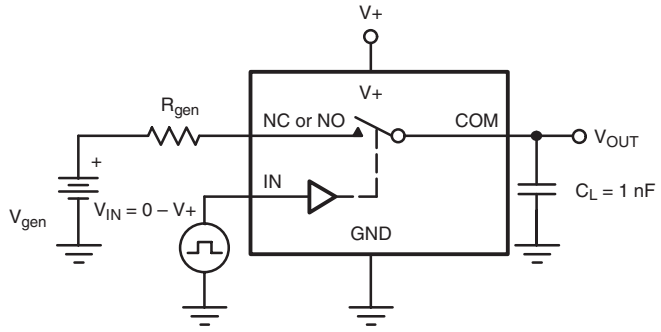
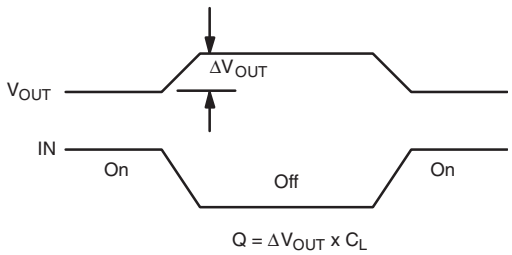



**Figure 2. Break-Before-Make Interval**




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

**Figure 3. Charge Injection**

## TEST CIRCUITS

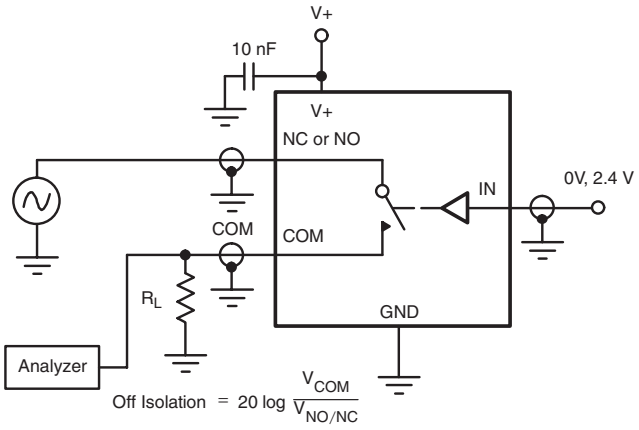



**Figure 4. Off-Isolation**

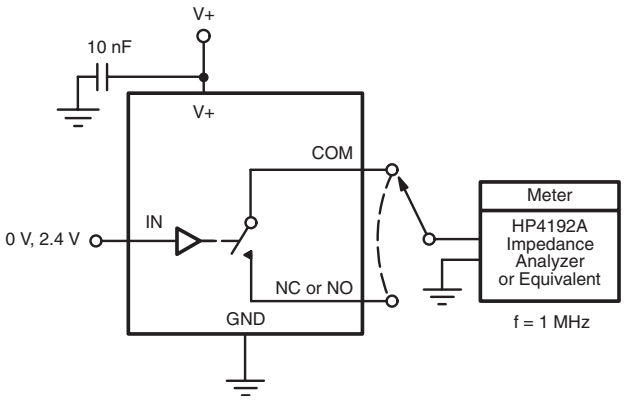



**Figure 5. Channel Off/On Capacitance**

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