300-MHz, 2.5-Ω, Dual SPDT Analog Switches

DESCRIPTION

The DG3516/DG3517 are dual SPDT analog switches which operate from 1.8 V to 5.5 V single rail power supply. They are design for audio, video, and USB switching applications.

The devices have 2.5 Ω on-resistance and 300 MHz 3dB bandwidth. 0.2 Ω on-resistance matching and 1 Ω flatness make the device high linearity. The devices are 1.6 V logic compatible within the full operation voltage range.

These switches are built on a sub-micron high density process that brings low power consumption and low voltage performance.

The switches are packaged in MICRO FOOT chip scale package of 4 x 3 bump array.

As a committed partner to the community and environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switch products manufactured with tin/silver/copper (SnAgCu) device termination, the lead (Pb)-free "-E1" suffix is being used as a designator.

FEATURES

- 1.8 V to 5.5 V Operation
- 2.5 Ω at 2.7 V r_{ON}
- 300 MHz - 3 dB Bandwidth
- ESD Method 3015.7 > 2 kV
- Latch-Up Current 200 mA (JESD 78)
- 1.6 V Logic Compatible

Pb-free

RoHS COMPLIANT

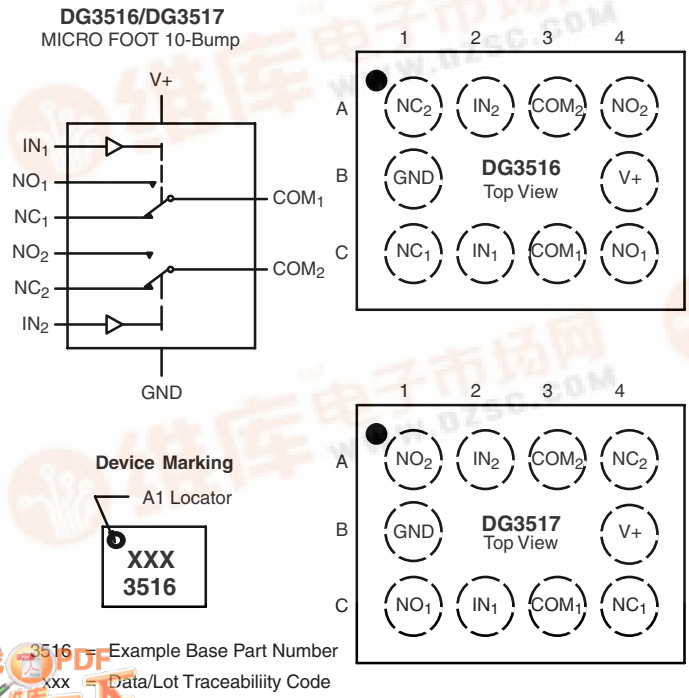
BENEFITS

- Space Saving MICRO FOOT® Package
- High Linearity
- Low Power Consumption
- High Bandwidth
- Full Rail Signal Swing Range

APPLICATIONS

- Cellular Phones
- MP3
- Media Players
- Modems
- Hard Drives
- PCMCIA

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking

A1 Locator

XXX
3516

3516 = Example Base Part Number
xxx = Data/Lot Traceabiliity Code

TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	MICRO FOOT: 10 Bump (4 x 3, 0.5 mm Pitch, 238 µm Bump Height)	DG3516DB-T5-E1 DG3517DB-T5-E1

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC, COM)		± 100	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Package Solder Reflow Conditions[b]	IR/Convection	250	
ESD per Method 3015.7		> 2	kV
Power Dissipation (Packages)[c]	MICRO FOOT: 10 Bump (4 x 3 mm)[d]	457	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020B)
c. All bumps welded or soldered to PC Board.
d. Derate 5.7 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.7 to 3.6 V, V_{IN} = 0.5 V or 1.4 V[e]		Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance[d]	r_{ON}	V+ = 2.7 V, I_{NO}, I_{NC} = 10 mA	V_{COM} = 1.5 V	Room Full		2.5	3.5 3.8	Ω
r_{ON} Flatness[d]	r_{ON} Flatness		V_{COM} = 1, 1.5, 2 V	Room		0.52	1.0	
On-Resistance Match Between Channels[d]	$\Delta r_{DS(on)}$		V_{COM} = 1.5 V	Room			0.25	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V		Room Full	- 2 - 20		2 20	nA
	$I_{COM(off)}$			Room Full	- 2 - 20		2 20	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V		Room Full	- 2 - 20		2 20	
Digital Control								
Input High Voltage[d]	V_{INH}			Full	1.4			V
Input Low Voltage	V_{INL}			Full			0.5	
Input Capacitance	C_{in}			Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	1		1	µA

SPECIFICATIONS (V+ = 3 V)

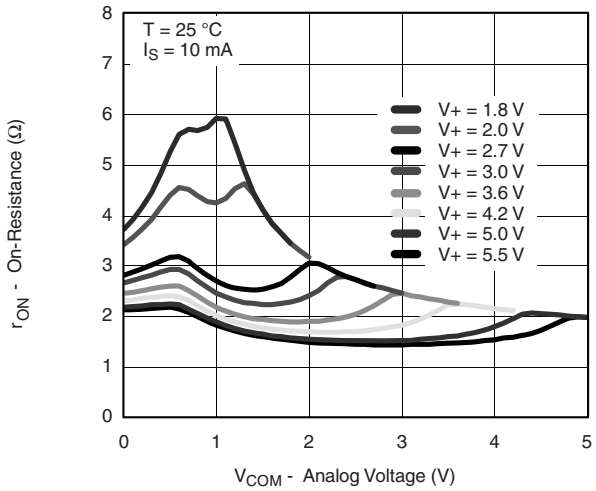
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.7 to 3.6 V, V_{IN} = 0.5 V or 1.4 V[e]		Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Dynamic Characteristics								
Turn-On Time	t_{ON}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V R_L = 300 Ω, C_L = 35 pF		Room Full		21	51 52	ns
Turn-Off Time	t_{OFF}			Room Full		15	45 46	
Break-Before-Make Time	t_d			Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2.0 V, R_{GEN} = 0 Ω		Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 74		dB
			f = 10 MHz	Room		- 54		
Crosstalk[d]	X_{TALK}		f = 1 MHz	Room		- 76		
			f = 10 MHz	Room		- 56		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		12		pF
	$C_{NC(off)}$			Room		12		
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		40		
	$C_{NC(on)}$			Room		40		
Power Supply								
Power Supply Current	I+	V_{IN} = 0 or V+		Room Full			1.0 1.0	µA

SPECIFICATIONS (V+ = 5 V)

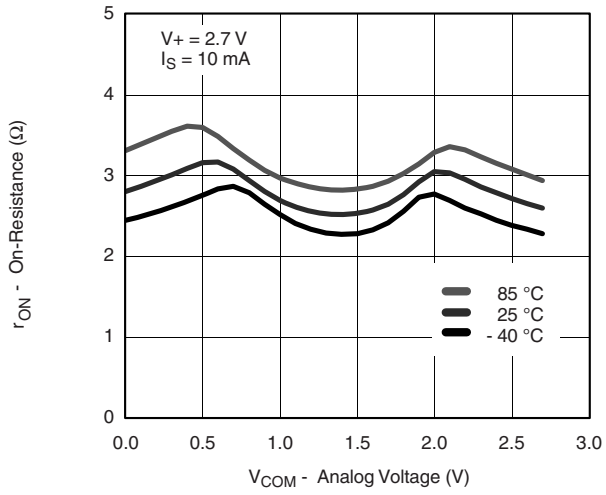
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 4.2 to 5.5 V, V_{IN} = 0.8 V or 2.0 V[e]		Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance[d]	r_{ON}	V+ = 4.2 V, I_{NO}, I_{NC} = 10 mA	V_{COM} = 3.5 V	Room Full		2.2	2.9 3.1	Ω
r_{ON} Flatness[d]	r_{ON} Flatness		V_{COM} = 1, 2, 3.5 V	Room		0.53	1.0	
On-Resistance Match Between Channels[d]	$\Delta r_{DS(on)}$		V_{COM} = 3.5 V	Room			0.25	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V, V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V		Room Full	- 2 - 20		2 20	nA
	$I_{COM(off)}$			Room Full	- 2 - 20		2 20	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V		Room Full	- 2 - 20		2 20	
Digital Control								
Input High Voltage[d]	V_{INH}			Full	2.0			V
Input Low Voltage	V_{INL}			Full			0.8	
Input Capacitance	C_{in}			Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	1		1	µA
Dynamic Characteristics								
Turn-On Time	t_{ON}	V+ = 4.2 V, V_{NO} or V_{NC} = 3.0 V, R_L = 300 Ω, C_L = 35 pF		Room Full		15	45 46	ns
Turn-Off Time	t_{OFF}			Room Full		12	42 43	
Break-Before-Make Time	t_d			Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2.0 V, R_{GEN} = 0 Ω		Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 74		dB
			f = 10 MHz	Room		- 54		
Crosstalk[d]	X_{TALK}		f = 1 MHz	Room		- 78		
			f = 10 MHz	Room		- 56		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		12		pF
	$C_{NC(off)}$			Room		12		
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		40		
	$C_{NC(on)}$			Room		40		
Power Supply								
Power Supply Current	I+	V_{IN} = 0 or V+		Room Full			1.0 1.0	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V testing, not production tested.

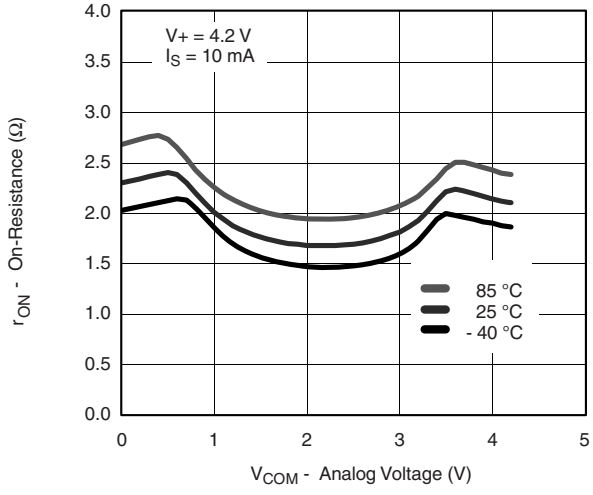
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



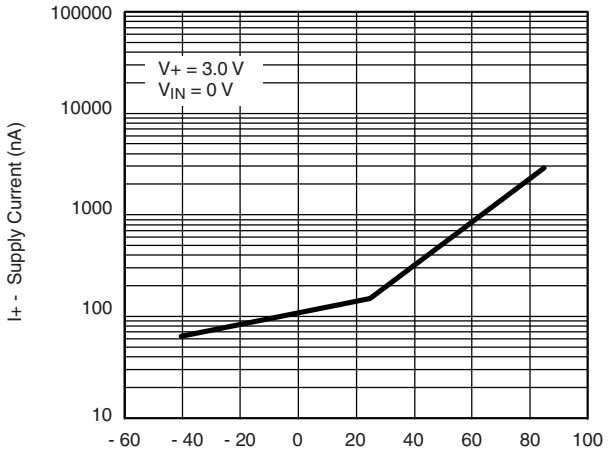
r_{ON} vs. V_{COM} and Single Supply Voltage



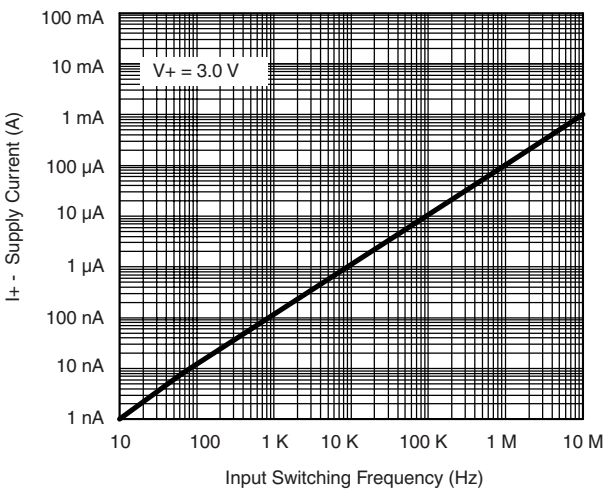
r_{ON} vs. Analog Voltage and Temperature



r_{ON} vs. Analog Voltage and Temperature

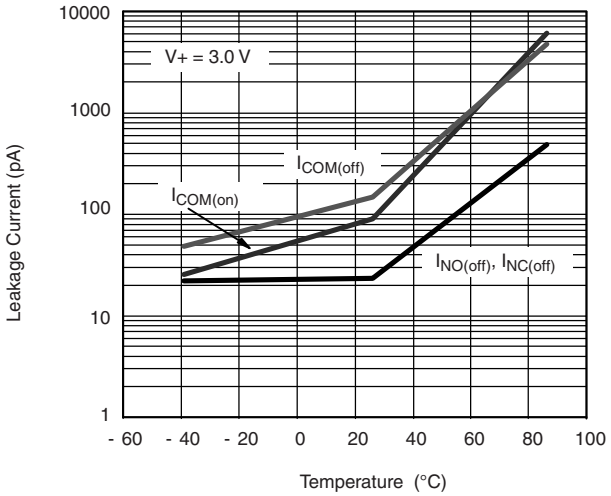


Supply Current vs. Temperature

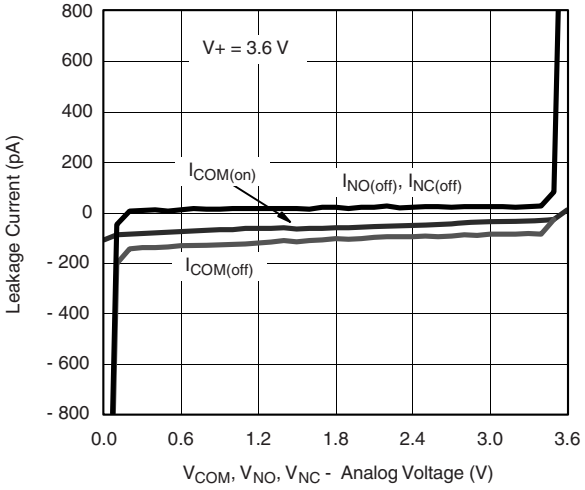


Supply Current vs. Input Switching Frequency

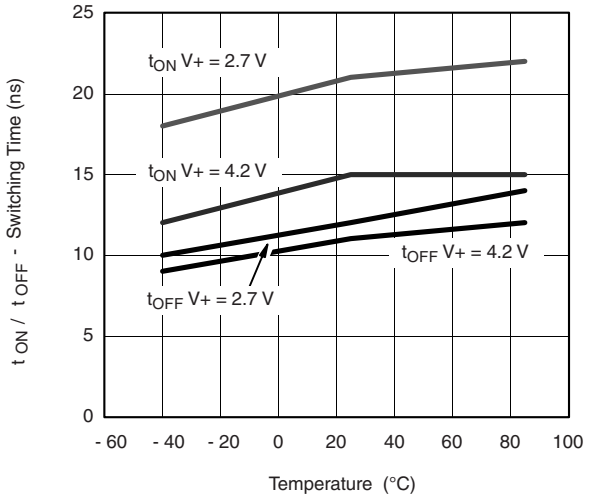
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



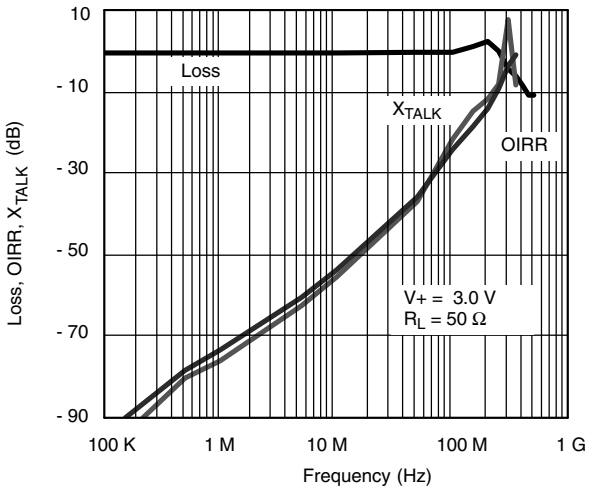
Leakage Current vs. Temperature



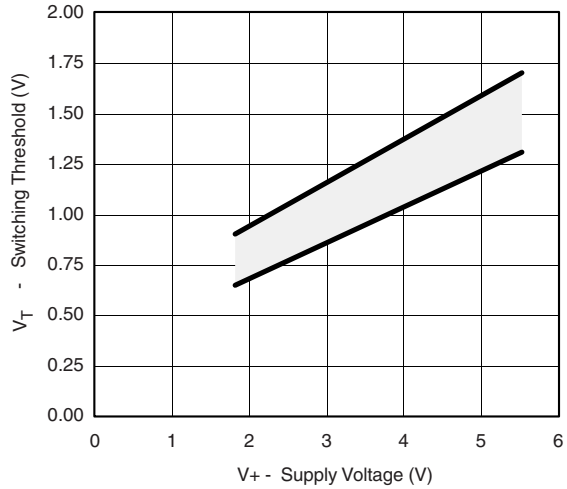
Leakage vs. Analog Voltage



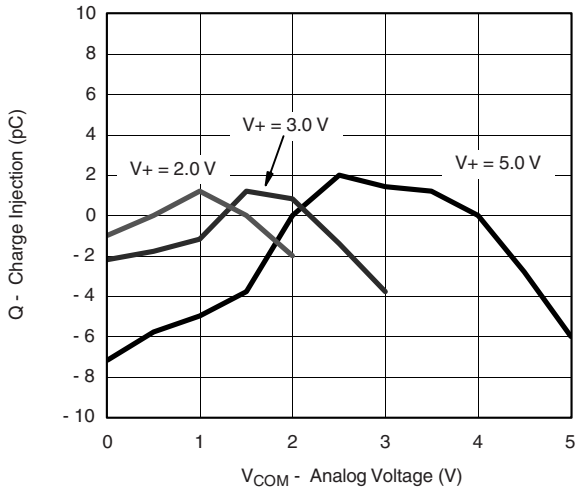
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

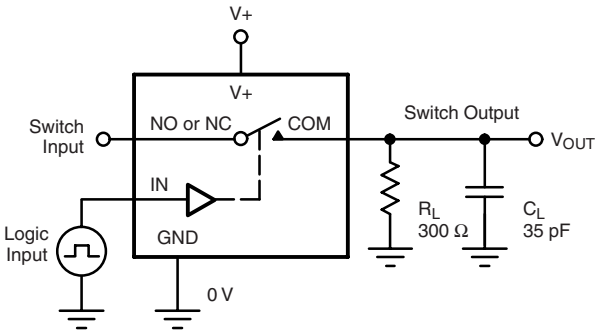


Switching Threshold vs. Supply Voltage



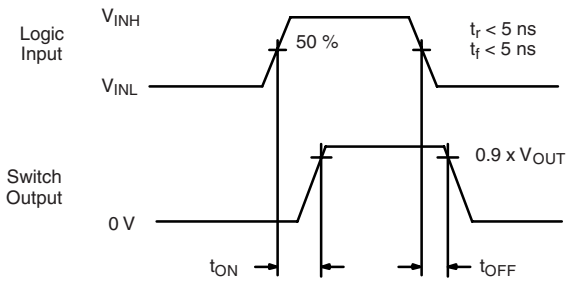
Charge Injection vs. Analog Voltage

TEST CIRCUITS



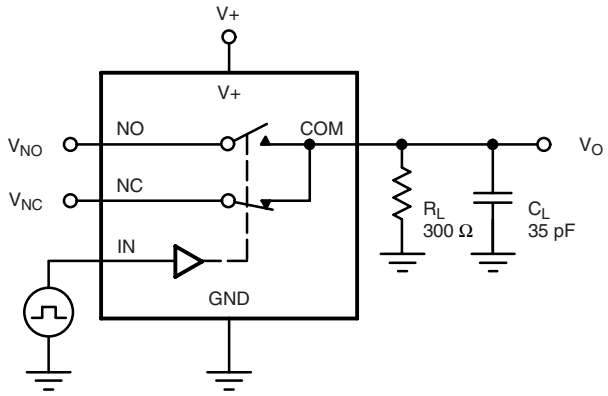
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

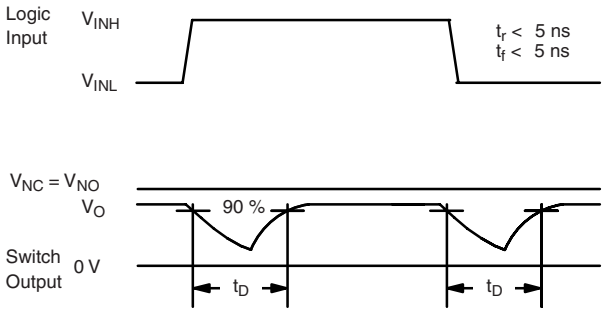
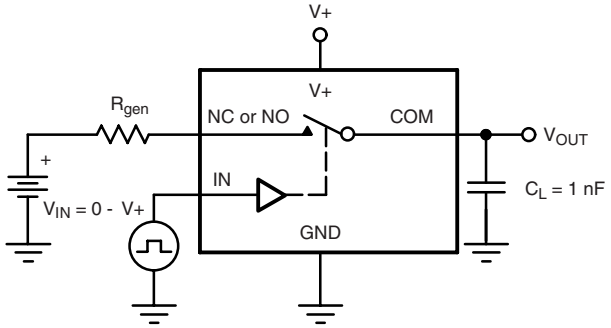
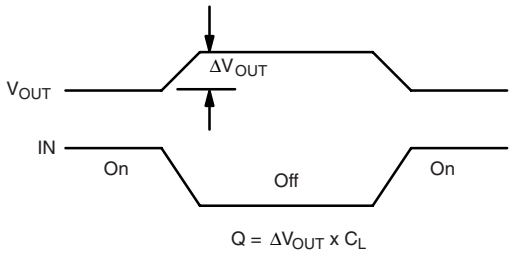


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

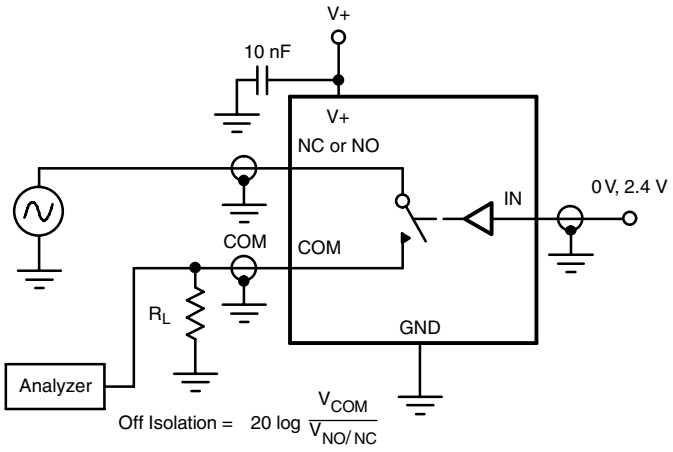


Figure 4. Off-Isolation

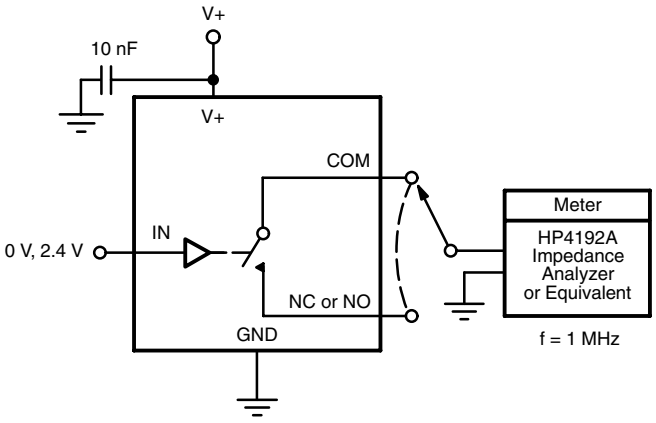
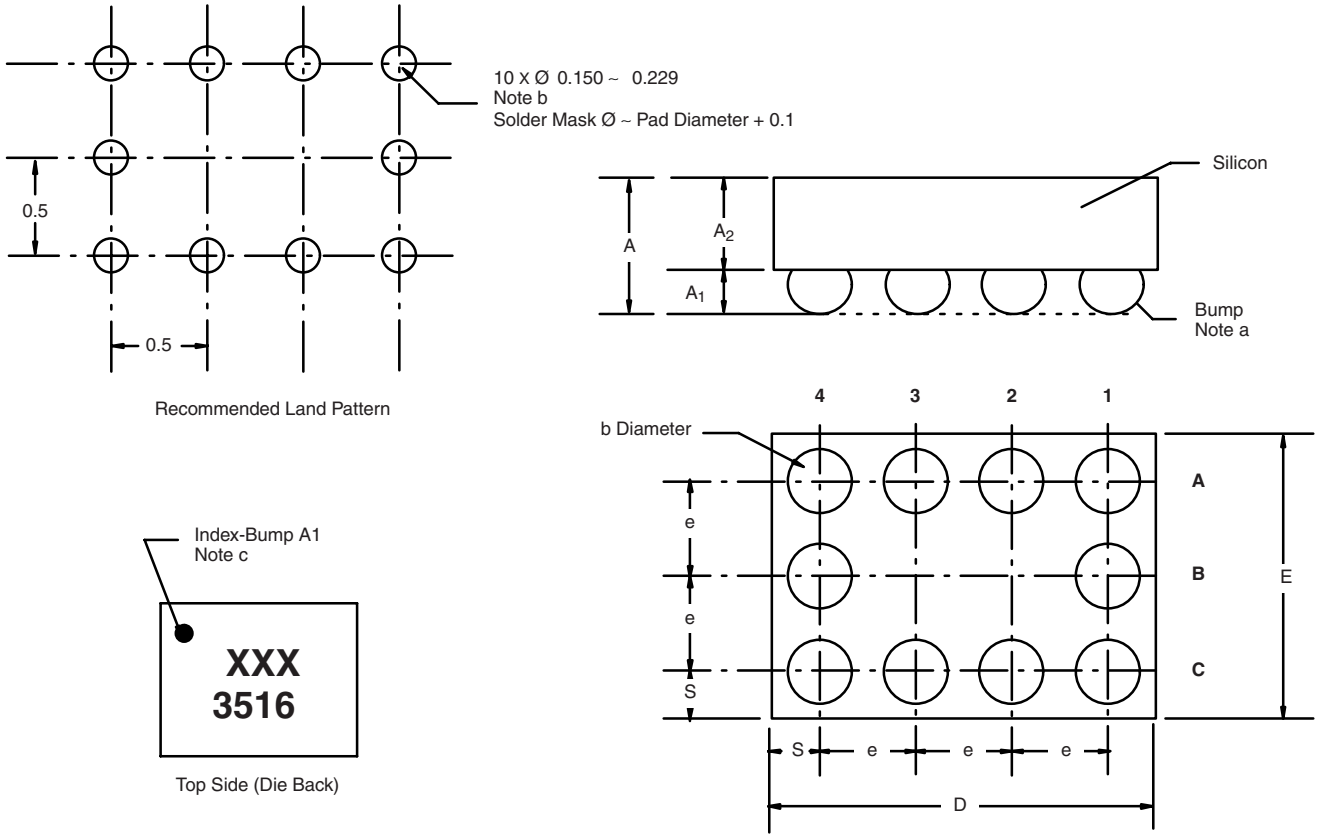


Figure 5. Channel Off/On Capacitance

PACKAGE OUTLINE

MICRO FOOT: 10 BUMP (4 x 3, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes (Unless Otherwise Specified):
a. Bump is Lead (Pb)-free Sn/Ag/Cu.
b. Non-solder mask defined copper landing pad.
c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

Dim	Millimeters[a]		Inches	
	Min	Max	Min	Max
A	0.688	0.753	0.0271	0.0296
A_1	0.218	0.258	0.0086	0.0102
A_2	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:

a. Use millimeters as the primary measurement.

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