

April 2007

DS25BR100 3.125 Gbps LVDS Buffer with PE and EQ



DS25BR100

3.125 Gbps LVDS Buffer with Transmit Pre-Emphasis and Receive Equalization

General Description

The DS25BR100 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR100 features transmit pre-emphasis (PE) and receive equalization (EQ), making it ideal for use as a repeater device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR110 features four levels of equalization for use as an optimized receiver device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

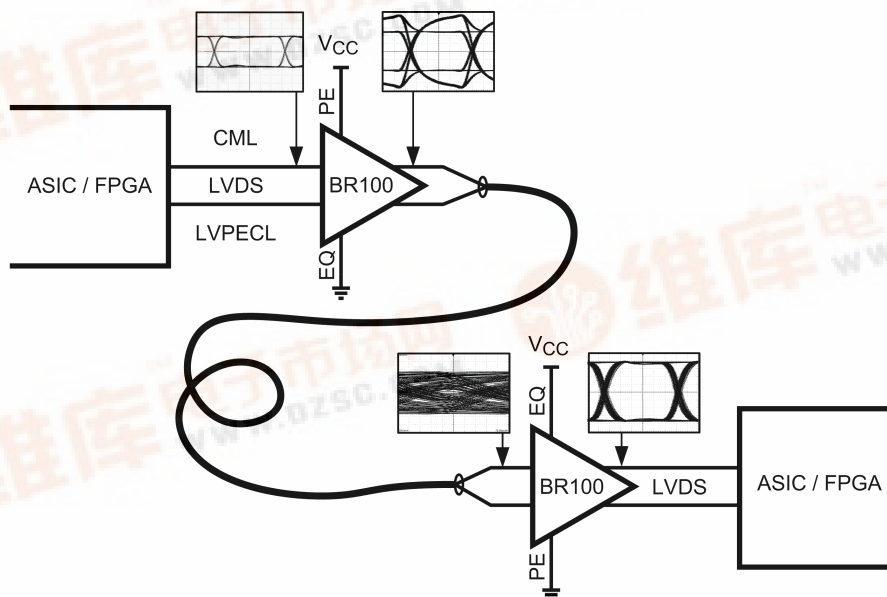
Features

- DC - 3.125 Gbps low jitter, high noise immunity, low power operation
- Receive equalization reduces ISI jitter due to media loss
- Transmit pre-emphasis drives lossy backplanes and cables
- On-chip 100Ω input and output termination minimizes insertion and return losses, reduces component count and minimizes board space
- 7 kV ESD on LVDS I/O pins protects adjoining components
- Small 3 mm x 3 mm 8-LLP space saving package

Applications

- Clock and data buffering
- Metallic cable driving and equalization
- FR-4 equalization

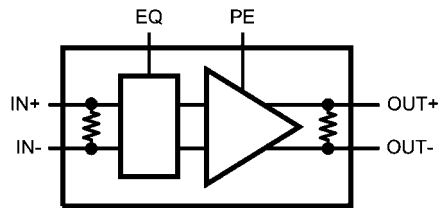
Typical Application



20179110

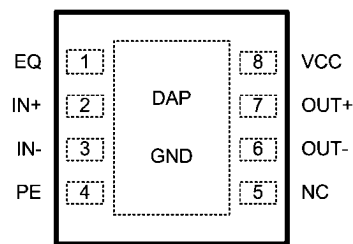


Block Diagram



20179101

Pin Diagram



20179104

Pin Descriptions

| Pin Name | Pin Name | Pin Type | Pin Description |
|----------|----------|----------|------------------------------------|
| EQ | 1 | Input | Equalizer select pin. |
| IN+ | 2 | Input | Non-inverting LVDS input pin. |
| IN- | 3 | Input | Inverting LVDS input pin. |
| PE | 4 | Input | Pre-emphasis select pin. |
| NC | 5 | NA | "NO CONNECT" pin. |
| OUT- | 6 | Output | Inverting LVDS output pin. |
| OUT+ | 7 | Output | Non-inverting LVDS Output pin. |
| VCC | 8 | Power | Power supply pin. |
| GND | DAP | Power | Ground pad (DAP - die attach pad). |

Control Pins (PE and EQ) Truth Table

| EQ | PE | Equalization Level | Pre-emphasis Level |
|----|----|-----------------------------------|-----------------------------------|
| 0 | 0 | Low (Approx. 4 dB at 1.56 GHz) | Off |
| 0 | 1 | Low (Approx. 4 dB at 1.56 GHz) | Medium (Approx. 6 dB at 1.56 GHz) |
| 1 | 0 | Medium (Approx. 8 dB at 1.56 GHz) | Off |
| 1 | 1 | Medium (Approx. 8 dB at 1.56 GHz) | Medium (Approx. 6 dB at 1.56 GHz) |

Ordering Codes and Configurations

| NSID | Function | Available Equalization Levels | Available Pre-emphasis Levels |
|--------------|-----------------|-------------------------------|-------------------------------|
| DS25BR100TSD | Buffer/Repeater | Low / Medium | Off / Medium |
| DS25BR110TSD | Receiver | Off / Low / Medium / High | NA |
| DS25BR120TSD | Driver | NA | Off / Low / Medium / High |
| DS25BR150TSD | Buffer/Repeater | NA | NA |

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| | |
|----------------------------------------------------|------------------------------|
| Supply Voltage (V_{CC}) | -0.3V to +4V |
| LVC MOS Input Voltage (EQ, PE) | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Input Voltage (IN+, IN-) | -0.3V to +4V |
| LVDS Differential Input Voltage ((IN+) - (IN-)) | 0V to 1V |
| LVDS Output Voltage (OUT+, OUT-) | -0.3V to +4V |
| LVDS Differential Output Voltage ((OUT+) - (OUT-)) | 0V to 1V |
| LVDS Output Short Circuit Current Duration | 5 ms |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature Range | |
| Soldering (4 sec.) | +260°C |
| Maximum Package Power Dissipation at 25°C | |
| SDA Package | 2.08W |
| Derate SDA Package | 16.7 mW/°C above +25°C |

Package Thermal Resistance

| | |
|---------------|-----------|
| θ_{JA} | +60.0°C/W |
| θ_{JC} | +12.3°C/W |

ESD Susceptibility

| | |
|--------------|--------|
| HBM (Note 1) | ≥7 kV |
| MM (Note 2) | ≥250V |
| CDM (Note 3) | ≥1250V |

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

| | Min | Typ | Max | Units |
|--------------------------------------------------|-----|-----|-----|-------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Receiver Differential Input Voltage (V_{ID}) | | | 1.0 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------------------------------|-----------------------------------------------------------------|-------------------------------------------|------|------|----------|-------|
| LVCMOS INPUT DC SPECIFICATIONS (EQ, PE) | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{CC} | V |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V |
| I_{IH} | High Level Input Current | $V_{IN} = 3.6V$ $V_{CC} = 3.6V$ | | 0 | ±10 | µA |
| I_{IL} | Low Level Input Current | $V_{IN} = GND$ $V_{CC} = 3.6V$ | | 0 | ±10 | µA |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18 \text{ mA}$, $V_{CC} = 0V$ | | -0.9 | -1.5 | V |
| LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-) | | | | | | |
| V_{OD} | Differential Output Voltage | $R_L = 100\Omega$ | 250 | 350 | 450 | mV |
| ΔV_{OD} | Change in Magnitude of V_{OD} for Complimentary Output States | | -35 | | 35 | mV |
| V_{OS} | Offset Voltage | $R_L = 100\Omega$ | 1.05 | 1.2 | 1.375 | V |
| ΔV_{OS} | Change in Magnitude of V_{OS} for Complimentary Output States | | -35 | | 35 | mV |
| I_{OS} | Output Short Circuit Current (Note 8) | OUT to GND, PE = 0 | | -35 | -55 | mA |
| | | OUT to V_{CC} , PE = 0 | | 7 | 55 | mA |
| C_{OUT} | Output Capacitance | Any LVDS Output Pin to GND | | 1.2 | | pF |
| R_{OUT} | Output Termination Resistor | Between OUT+ and OUT- | | 100 | | Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------------------------|-----------------------------------|--------------------------------------------------------------------|------|---------|-----------------|----------|
| LVDS INPUT DC SPECIFICATIONS (IN+, IN-) | | | | | | |
| V_{ID} | Input Differential Voltage | $V_{CM} = +0.05V \text{ or } V_{CC} - 0.05V$ | 0 | | 1 | V |
| V_{TH} | Differential Input High Threshold | | | 0 | +100 | mV |
| V_{TL} | Differential Input Low Threshold | | -100 | 0 | | mV |
| V_{CMR} | Common Mode Voltage Range | $V_{ID} = 100 \text{ mV}$ | 0.05 | | $V_{CC} - 0.05$ | V |
| I_{IN} | Input Current | $V_{IN} = \text{GND or } 3.6V$ $V_{CC} = 3.6V \text{ or } 0.0V$ | | ± 1 | ± 10 | μA |
| C_{IN} | Input Capacitance | Any LVDS Input Pin to GND | | 1.7 | | pF |
| R_{IN} | Input Termination Resistor | Between IN+ and IN- | | 100 | | Ω |
| SUPPLY CURRENT | | | | | | |
| I_{CC} | Supply Current | $EQ = 0, PE = 0$ | | 35 | 43 | mA |

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .

Note 7: Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics (Note 11)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 9, 10)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|------------|-----|------|-------|-------------------|
| LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-) | | | | | | | |
| t _{PHLD} | Differential Propagation Delay High to Low | R _L = 100Ω | | 350 | 465 | ps | |
| t _{PLHD} | Differential Propagation Delay Low to High | | | 350 | 465 | ps | |
| t _{SKD1} | Pulse Skew t _{PLHD} – t _{PHLD} (Note 12) | | | 45 | 100 | ps | |
| t _{SKD2} | Part to Part Skew (Note 13) | | | 45 | 150 | ps | |
| t _{LHT} | Rise Time | R _L = 100Ω | | 80 | 150 | ps | |
| t _{HLT} | Fall Time | | | 80 | 150 | ps | |
| JITTER PERFORMANCE WITH PE = OFF AND EQ = LOW (Figures 6, 7) | | | | | | | |
| t _{RJ1A} | Random Jitter (RMS Value) Input Test Channel D (Note 14) | V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) PE = 0, EQ = 0 | 2.5 Gbps | | 0.5 | 1 | ps |
| t _{RJ2A} | | | 3.125 Gbps | | 0.5 | 1 | ps |
| t _{DJ1A} | Deterministic Jitter (Peak to Peak) Input Test Channel D (Note 15) | V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) PE = 0, EQ = 0 | 2.5 Gbps | | 1 | 16 | ps |
| t _{DJ2A} | | | 3.125 Gbps | | 11 | 31 | ps |
| t _{TJ1A} | Total Jitter (Peak to Peak) Input Test Channel D (Note 16) | V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) PE = 0, EQ = 0 | 2.5 Gbps | | 0.03 | 0.09 | UI _{P-P} |
| t _{TJ2A} | | | 3.125 Gbps | | 0.06 | 0.14 | UI _{P-P} |
| JITTER PERFORMANCE WITH PE = OFF AND EQ = MEDIUM (Figures 6, 7) | | | | | | | |
| t _{RJ1B} | Random Jitter (RMS Value) Input Test Channel E (Note 14) | V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) PE = 0, EQ = 1 | 2.5 Gbps | | 0.5 | 1 | ps |
| t _{RJ2B} | | | 3.125 Gbps | | 0.5 | 1 | ps |
| t _{DJ1B} | Deterministic Jitter (Peak to Peak) Input Test Channel E (Note 15) | V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) PE = 0, EQ = 1 | 2.5 Gbps | | 10 | 29 | ps |
| t _{DJ2B} | | | 3.125 Gbps | | 27 | 43 | ps |
| t _{TJ1B} | Total Jitter (Peak to Peak) Input Test Channel E (Note 16) | V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) PE = 0, EQ = 1 | 2.5 Gbps | | 0.07 | 0.12 | UI _{P-P} |
| t _{TJ2B} | | | 3.125 Gbps | | 0.12 | 0.17 | UI _{P-P} |
| JITTER PERFORMANCE WITH PE = MEDIUM AND EQ = LOW (Figures 5, 7) | | | | | | | |
| t _{RJ1C} | Random Jitter (RMS Value) Input Test Channel D Output Test Channel B (Note 14) | V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) PE = 1, EQ = 0 | 2.5 Gbps | | 0.5 | 1 | ps |
| t _{RJ2C} | | | 3.125 Gbps | | 0.5 | 1 | ps |
| t _{DJ1C} | Deterministic Jitter (Peak to Peak) Input Test Channel D Output Test Channel B (Note 15) | V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) PE = 1, EQ = 0 | 2.5 Gbps | | 29 | 57 | ps |
| t _{DJ2C} | | | 3.125 Gbps | | 29 | 51 | ps |
| t _{TJ1C} | Total Jitter (Peak to Peak) Input Test Channel D Output Test Channel B (Note 16) | V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) PE = 1, EQ = 0 | 2.5 Gbps | | 0.10 | 0.19 | UI _{P-P} |
| t _{TJ2C} | | | 3.125 Gbps | | 0.13 | 0.22 | UI _{P-P} |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|--------------------------------------------------------------------|------------------------------------------------------------|-----------------------------------------------------------|------------|-----|------|-------|-------------------|
| JITTER PERFORMANCE WITH PE = MEDIUM AND EQ = MEDIUM (Figures 5, 7) | | | | | | | |
| t _{RJ1D} | Random Jitter (RMS Value) | V _{ID} = 350 mV | 2.5 Gbps | | 0.5 | 1.1 | ps |
| t _{RJ2D} | Input Test Channel E Output Test Channel B (Note 14) | V _{CM} = 1.2V Clock (RZ) PE = 1, EQ = 1 | 3.125 Gbps | | 0.5 | 1 | ps |
| t _{DJ1D} | Deterministic Jitter (Peak to Peak) | V _{ID} = 350 mV | 2.5 Gbps | | 41 | 77 | ps |
| t _{DJ2D} | Input Test Channel E Output Test Channel B (Note 15) | V _{CM} = 1.2V K28.5 (NRZ) PE = 1, EQ = 1 | 3.125 Gbps | | 46 | 98 | ps |
| t _{TJ1D} | Total Jitter (Peak to Peak) | V _{ID} = 350 mV | 2.5 Gbps | | 0.13 | 0.20 | UI _{P-P} |
| t _{TJ2D} | Input Test Channel E Output Test Channel B (Note 16) | V _{CM} = 1.2V PRBS-23 (NRZ) PE = 1, EQ = 1 | 3.125 Gbps | | 0.19 | 0.30 | UI _{P-P} |

Note 9: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 10: Typical values represent most likely parametric norms for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: $t_{SKD1}, |t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 13: t_{SKD2} , Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 14: Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

Note 15: Tested with a combination of the 110000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

Note 16: Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

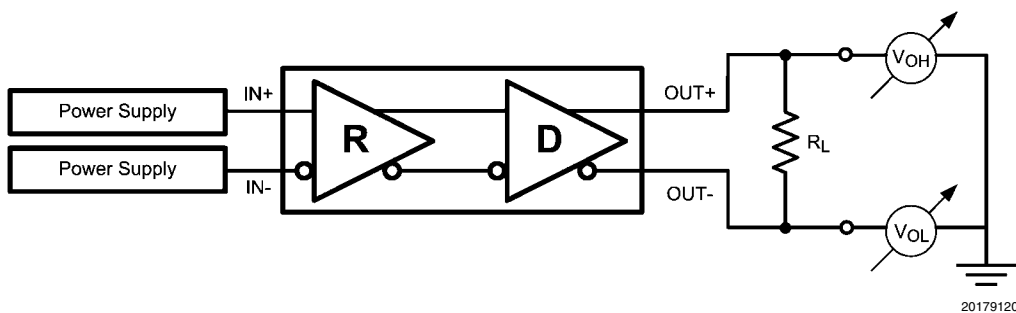


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

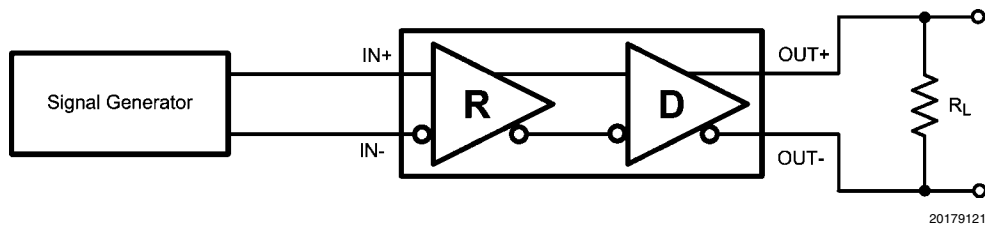


FIGURE 2. Differential Driver AC Test Circuit

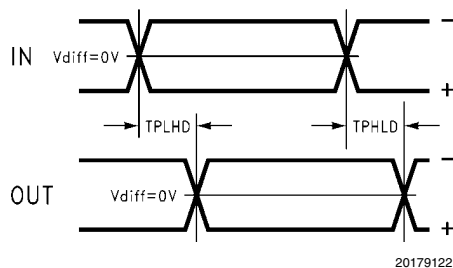


FIGURE 3. Propagation Delay Timing Diagram

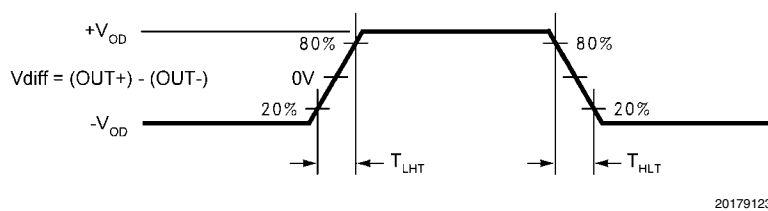
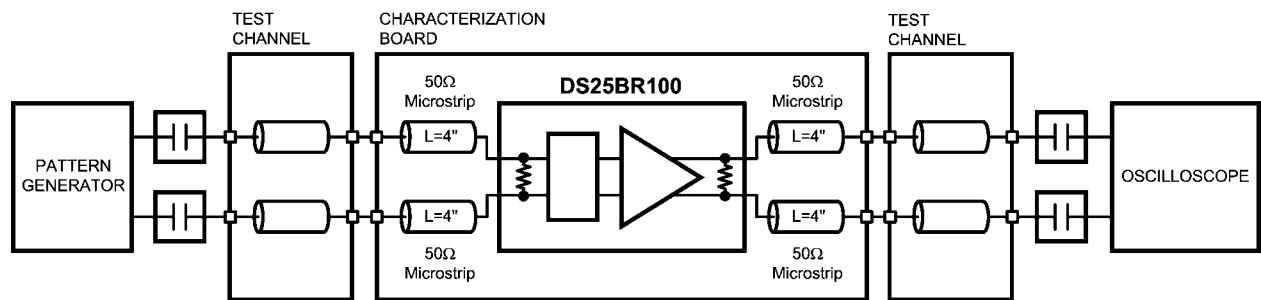


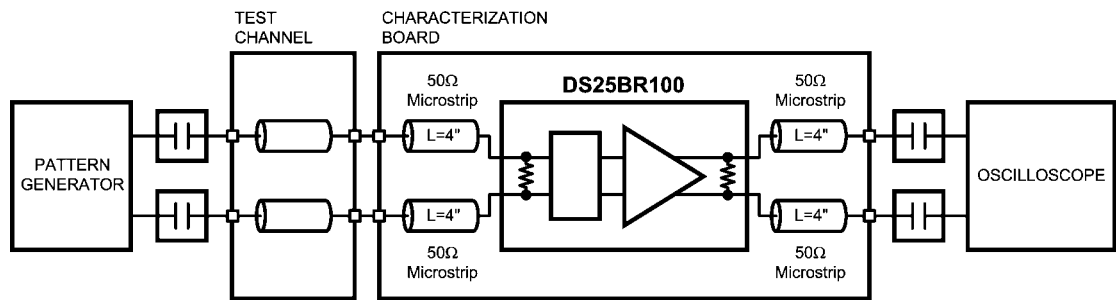
FIGURE 4. LVDS Output Transition Times

Pre-Emphasis and Equalization Test Circuits



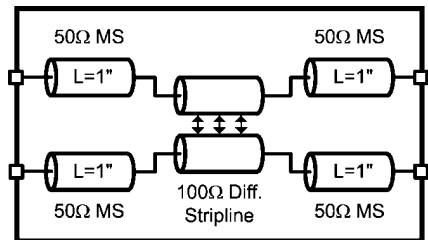
20179127

FIGURE 5. Pre-emphasis and Equalization Performance Test Circuit



20179126

FIGURE 6. Equalization Performance Test Circuit



20179128

FIGURE 7. Test Channel Description

Test Channel Loss Characteristics

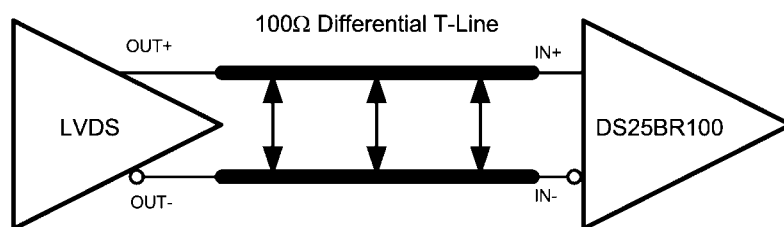
The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

| Test Channel | Length (inches) | Insertion Loss (dB) | | | | | |
|--------------|--------------------|---------------------|---------|----------|----------|----------|----------|
| | | 500 MHz | 750 MHz | 1000 MHz | 1250 MHz | 1500 MHz | 1560 MHz |
| A | 10 | -1.2 | -1.7 | -2.0 | -2.4 | -2.7 | -2.8 |
| B | 20 | -2.6 | -3.5 | -4.1 | -4.8 | -5.5 | -5.6 |
| C | 30 | -4.3 | -5.7 | -7.0 | -8.2 | -9.4 | -9.7 |
| D | 15 | -1.6 | -2.2 | -2.7 | -3.2 | -3.7 | -3.8 |
| E | 30 | -3.4 | -4.5 | -5.6 | -6.6 | -7.7 | -7.9 |
| F | 60 | -7.8 | -10.3 | -12.4 | -14.5 | -16.6 | -17.0 |

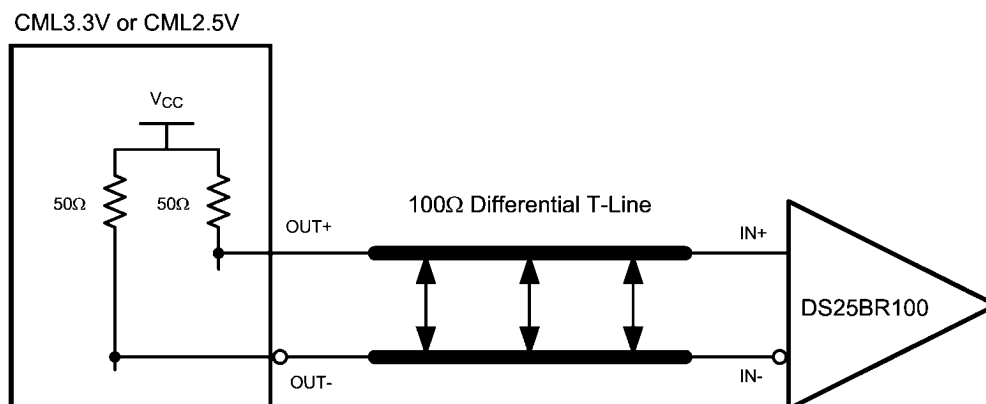
Device Operation

INPUT INTERFACING

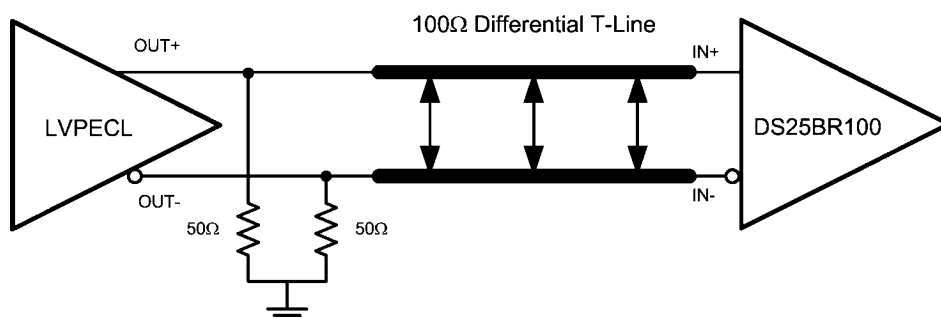
The DS25BR100 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR100 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR100 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to DS25BR100 Input 20179111



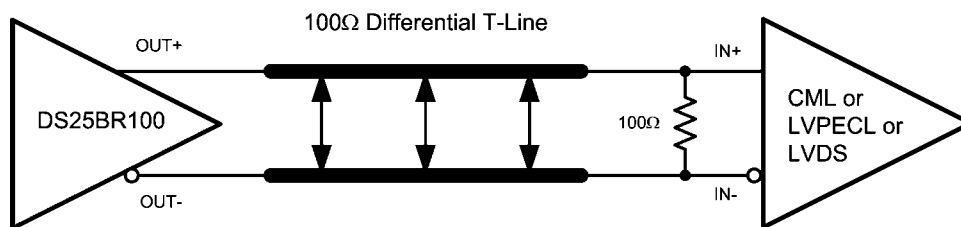
Typical CML Driver DC-Coupled Interface to DS25BR100 Input 20179112



Typical LVPECL Driver DC-Coupled Interface to DS25BR100 Input 20179113

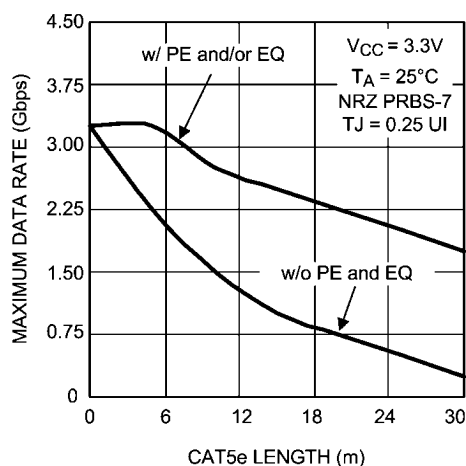
OUTPUT INTERFACING

The DS25BR100 outputs signals compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

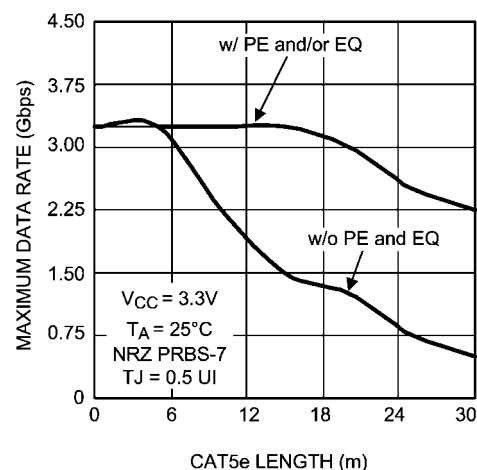


Typical DS25BR100 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver 20179114

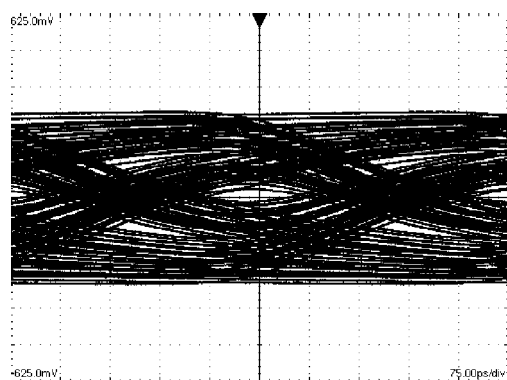
Typical Performance



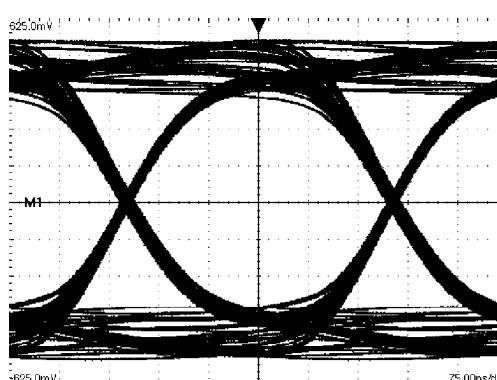
20179134
Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length



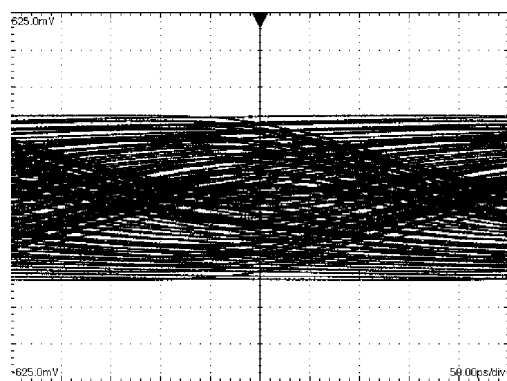
20179135
Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length



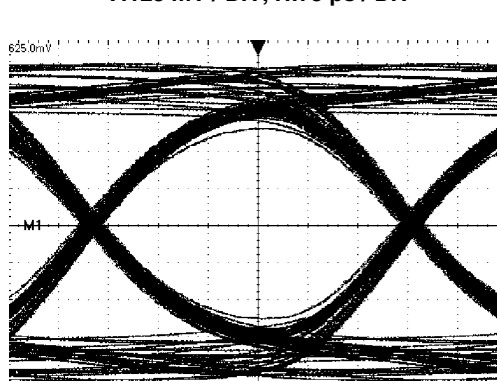
20179130
A 2.5 Gbps NRZ PRBS-7 After 60" Differential FR-4 Stripline
V:125 mV / DIV, H:75 ps / DIV



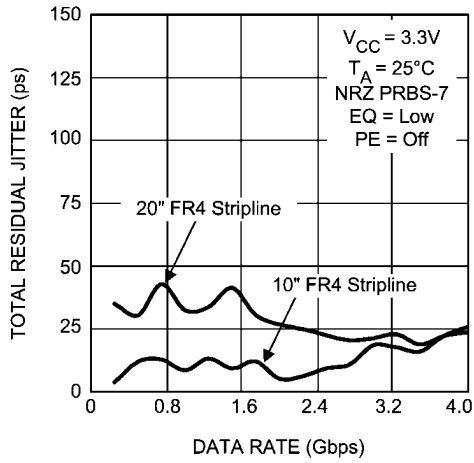
20179131
An Equalized (with PE and EQ) 2.5 Gbps NRZ PRBS-7 After The 40" Input and 20" Output Differential Stripline (Figure 5)
V:125 mV / DIV, H:75 ps / DIV



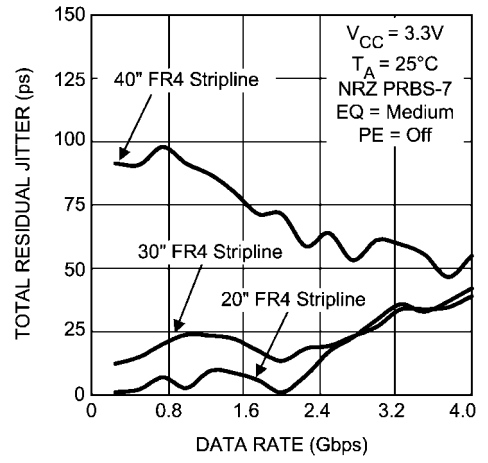
20179132
A 3.125 Gbps NRZ PRBS-7 After 60" Differential FR-4 Stripline
V:125 mV / DIV, H:50 ps / DIV



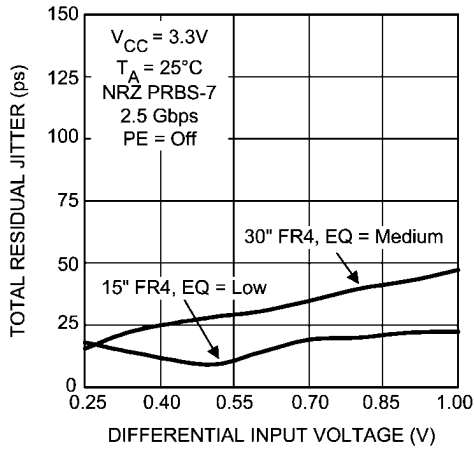
20179133
An Equalized (with PE and EQ) 3.125 Gbps NRZ PRBS-7 After The 40" Input and 20" Output Differential Stripline (Figure 5)
V:125 mV / DIV, H:50 ps / DIV



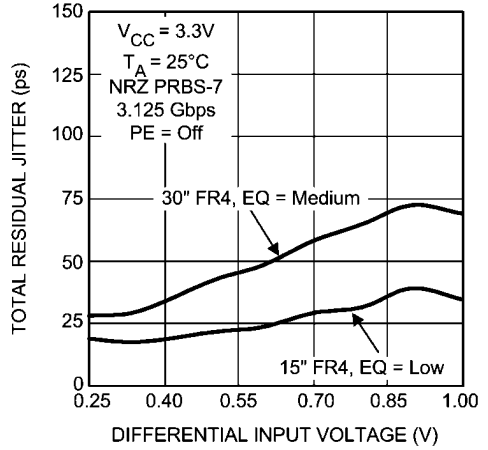
Total Jitter as a Function of Data Rate



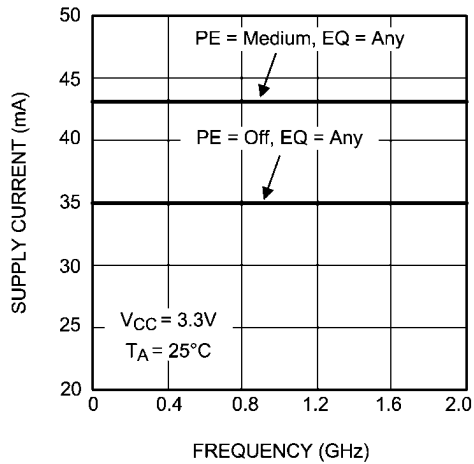
Total Jitter as a Function of Data Rate



Total Jitter as a Function of Input Amplitude

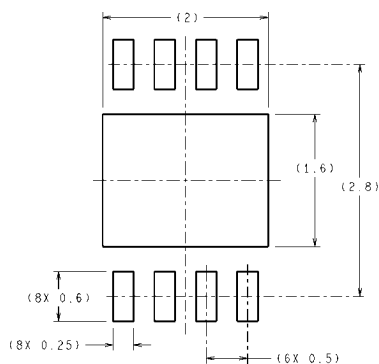


Total Jitter as a Function of Input Amplitude

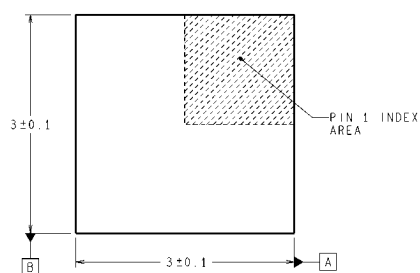


Power Supply Current as a Function of Frequency

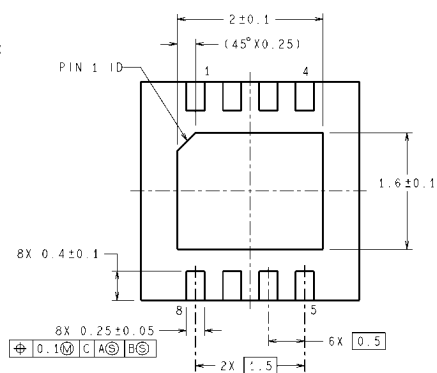
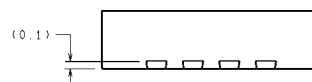
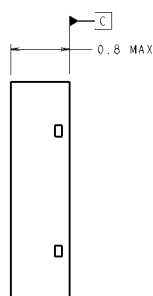
Physical Dimensions inches (millimeters) unless otherwise noted



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDA08A (Rev A)

Order Number DS25BR100TSD
NS Package Number SDA08A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

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