



February 2006

# DS90CF384A/DS90CF364A +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link—65 MHz, +3.3V LVDS Receiver 18-Bit Flat Panel Display (FPD) Link—65 MHz

## General Description

The DS90CF384A receiver converts the four LVDS data streams (Up to 1.8 Gbps throughput or 227 Megabytes/sec bandwidth) back into parallel 28 bits of CMOS/TTL data (24 bits of RGB and 4 bits of Hsync, Vsync, DE and CNTL). Also available is the DS90CF364A that converts the three LVDS data streams (Up to 1.3 Gbps throughput or 170 Megabytes/sec bandwidth) back into parallel 21 bits of CMOS/TTL data (18 bits of RGB and 3 bits of Hsync, Vsync and DE). Both Receivers' outputs are Falling edge strobe. A Rising edge or Falling edge strobe transmitter (DS90C383A/DS90C363A) will interoperate with a Falling edge strobe Receiver without any translation logic.

The DS90CF384A / DS90CF364A devices are enhanced over prior generation receivers and provided a wider data valid time on the receiver output.

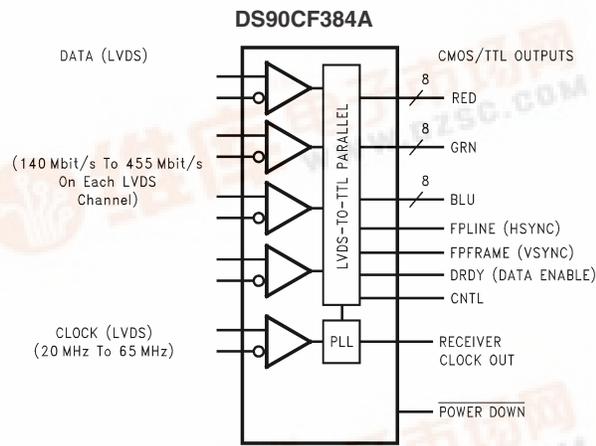
The DS90CF384A is also offered in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package which provides a 44 % reduction in PCB footprint compared to the 56L TSSOP package.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

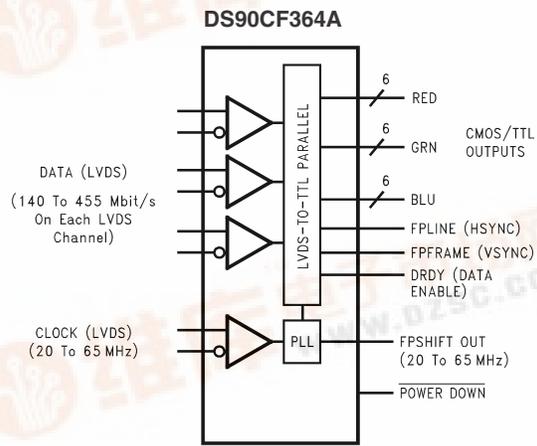
## Features

- 20 to 65 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best-in-Class Set & Hold Times on RxOUTPUTs
- Rx power consumption <142 mW (typ) @65MHz Grayscale
- Rx Power-down mode <200µW (max)
- ESD rating >7 kV (HBM), >700V (EIAJ)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead or 48-lead TSSOP package
- DS90CF384A is also available in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package

## Block Diagrams



Order Number DS90CF384AMTD or DS90CF384ASLC  
See NS Package Number MTD56 or SLC64A



Order Number DS90CF364AMTD  
See NS Package Number MTD48

DS90CF384A/DS90CF364A +3.3V LVDS Receiver 24-Bit-Color Flat Panel Display (FPD) Link—65 MHz, +3.3V LVDS Receiver 18-Bit-Color Flat Panel Display (FPD) Link—65 MHz



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
CMOS/TTL Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Receiver Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C
Solder Reflow Temperature (20 sec for FBGA)	+220°C
Maximum Package Power	
Dissipation Capacity @ 25°C	
MTD56 (TSSOP) Package:	
DS90CF384A	1.61 W
MTD48 (TSSOP) Package:	
DS90CF364A	1.89 W

SLC (FBGA) Package:

DS90CF384A 2.0 W

Package Derating:

DS90CF384AMTD 12.4 mW/°C above +25°C

DS90CF364AMTD 15 mW/°C above +25°C

DS90CF384ASLC 10.2 mW/°C above +25°C

ESD Rating

(HBM, 1.5 kΩ, 100 pF) > 7 kV

(EIAJ, 0Ω, 200 pF) > 700V

## Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Operating Free Air Temperature ( $T_A$ )	-10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage ( $V_{CC}$ )			100	mV <sub>PP</sub>

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>CMOS/TTL DC SPECIFICATIONS (For Power Down Pin)</b>							
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V	
$V_{IL}$	Low Level Input Voltage		GND		0.8	V	
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V	
$I_{IN}$	Input Current	$V_{IN} = 0.4V, 2.5V$ or $V_{CC}$		+1.8	+10	μA	
		$V_{IN} = GND$	-10	0		μA	
<b>CMOS/TTL DC SPECIFICATIONS</b>							
$V_{OH}$	High Level Output Voltage	$I_{OH} = -0.4$ mA	2.7	3.3		V	
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 2$ mA		0.06	0.3	V	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$		-60	-120	mA	
<b>LVDS RECEIVER DC SPECIFICATIONS</b>							
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +1.2V$			+100	mV	
$V_{TL}$	Differential Input Low Threshold		-100			mV	
$I_{IN}$	Input Current	$V_{IN} = +2.4V, V_{CC} = 3.6V$			±10	μA	
		$V_{IN} = 0V, V_{CC} = 3.6V$			±10	μA	
<b>RECEIVER SUPPLY CURRENT</b>							
ICCRW	Receiver Supply Current Worst Case	$C_L = 8$ pF, Worst Case Pattern, DS90CF384A (Figures 1, 4)	f = 32.5 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 65 MHz		81	105	mA
ICCRW	Receiver Supply Current Worst Case	$C_L = 8$ pF, Worst Case Pattern, DS90CF364A (Figures 1, 4)	f = 32.5 MHz		49	55	mA
			f = 37.5 MHz		53	60	mA
			f = 65 MHz		78	90	mA
ICCRG	Receiver Supply Current, 16 Grayscale	$C_L = 8$ pF, 16 Grayscale Pattern, (Figures 2, 3, 4)	f = 32.5 MHz		28	45	mA
			f = 37.5 MHz		30	47	mA
			f = 65 MHz		43	60	mA

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>RECEIVER SUPPLY CURRENT</b>						
ICCRZ	Receiver Supply Current Power Down	Power Down = Low Receiver Outputs Stay Low during Power Down Mode		10	55	μA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

**Note 2:** Typical values are given for  $V_{CC} = 3.3V$  and  $T_A = +25C$ .

**Note 3:** Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except  $V_{OD}$  and  $\Delta V_{OD}$ ).

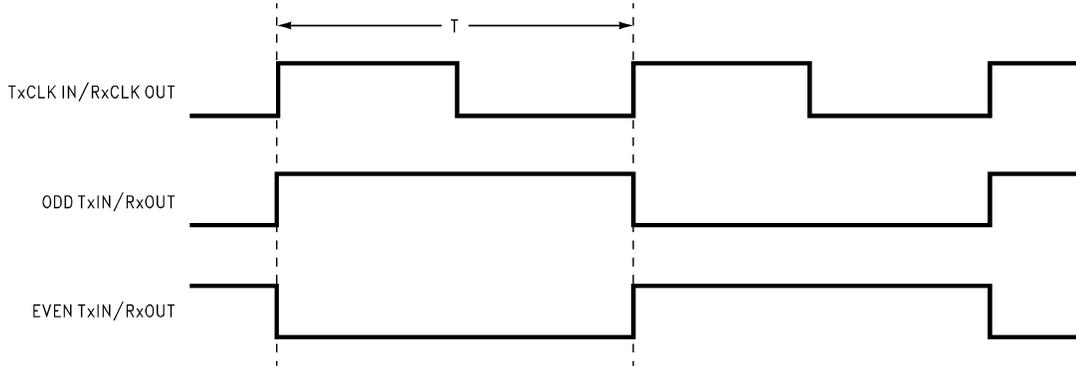
## Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 4)		2	5	ns	
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 4)		1.8	5	ns	
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 11, Figure 12)	f = 65 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin (Note 4) (Figure 13)	f = 65 MHz	400			ps
RCOP	RxCLK OUT Period (Figure 5)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 5)	f = 65 MHz	5.0	7.6	9.0	ns
RCOL	RxCLK OUT Low Time (Figure 5)		5.0	6.3	9.0	ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 5)		4.5	7.3		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 5)		4.0	6.3		ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, $V_{CC} = 3.3V$ (Figure 6)		3.5	5.0	7.5	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 7)			10		ms
RPDD	Receiver Power Down Delay (Figure 10)			1		μs

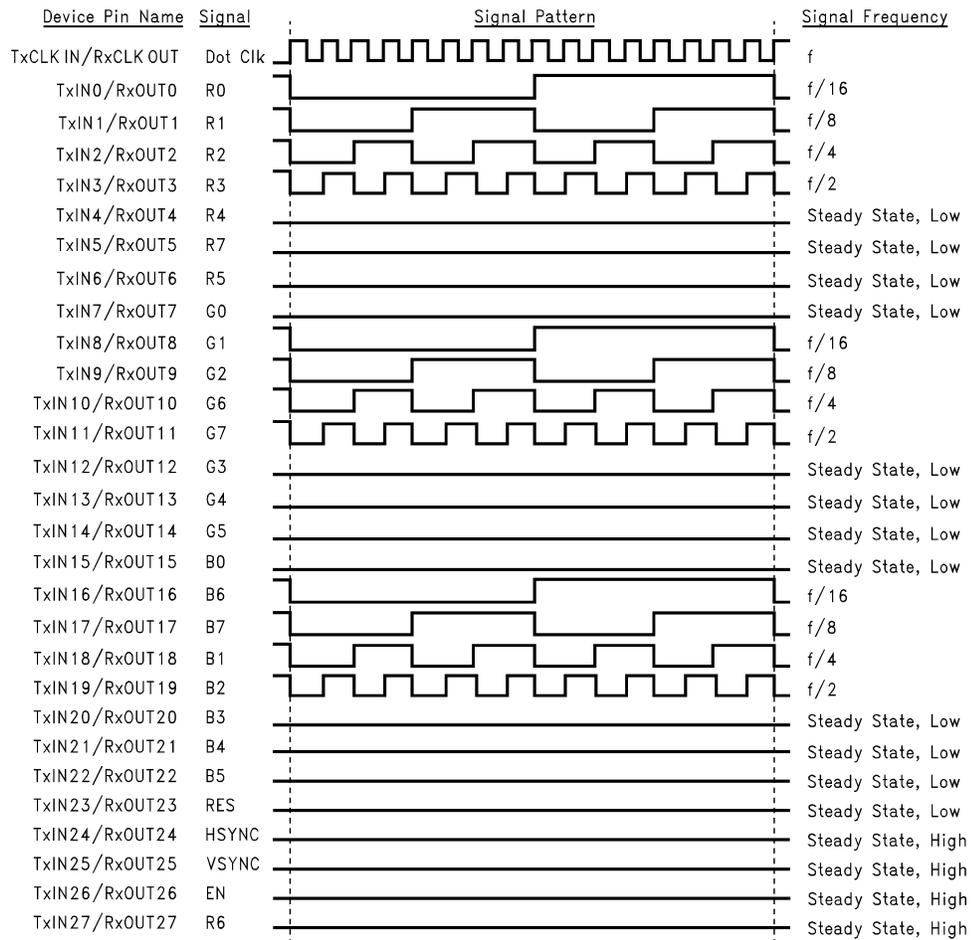
**Note 4:** Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the DS90C383A transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). The RSKM will change when different transmitters are used. This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

## AC Timing Diagrams



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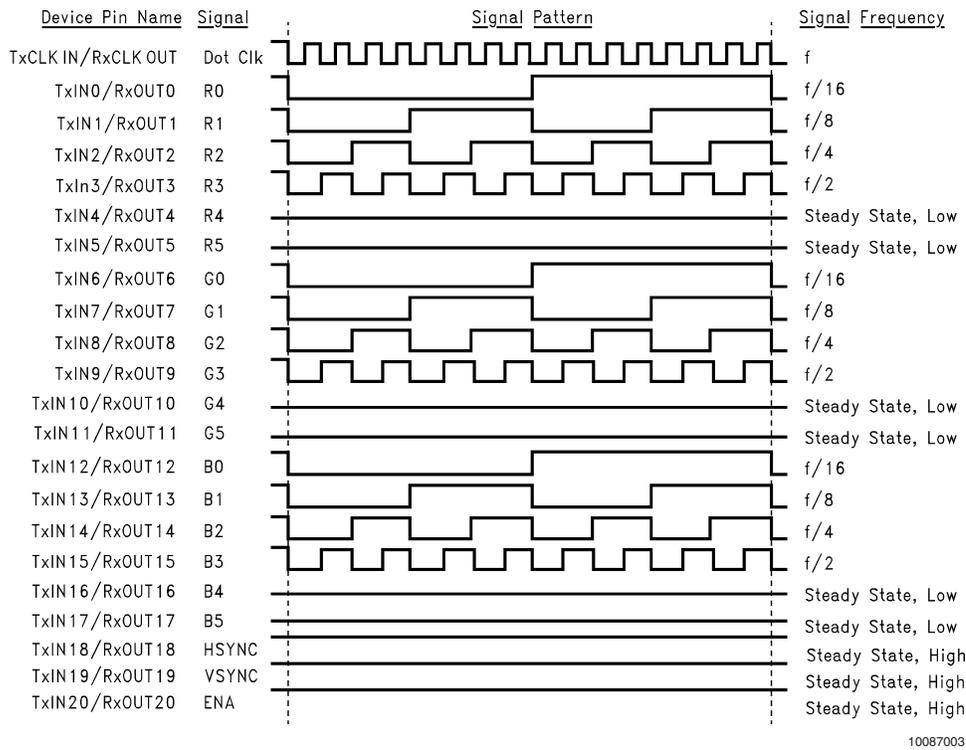
FIGURE 1. "Worst Case" Test Pattern



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FIGURE 2. "16 Grayscale" Test Pattern (DS90CF384A)(Notes 5, 6, 7, 8)

## AC Timing Diagrams (Continued)



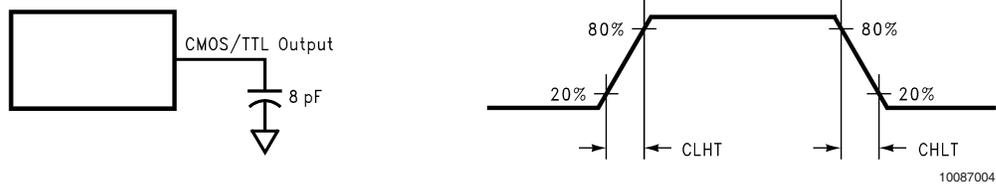
**FIGURE 3. "16 Grayscale" Test Pattern (DS90CF364A)(Notes 5, 6, 7, 8)**

**Note 5:** The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

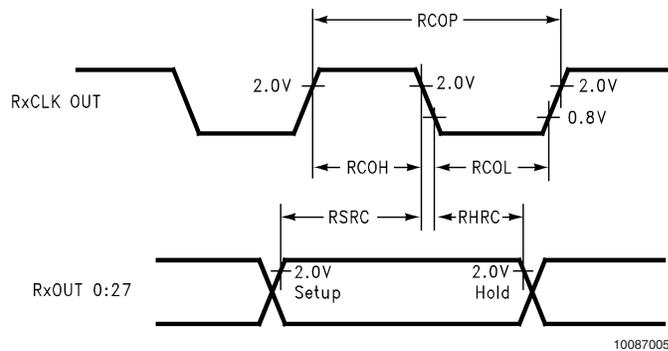
**Note 6:** The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

**Note 7:** Figures 1, 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

**Note 8:** Recommended pin to signal mapping. Customer may choose to define differently.



**FIGURE 4. DS90CF384A/DS90CF364A (Receiver) CMOS/TTL Output Load and Transition Times**



**FIGURE 5. DS90CF384A/DS90CF364A (Receiver) Setup/Hold and High/Low Times**

AC Timing Diagrams (Continued)

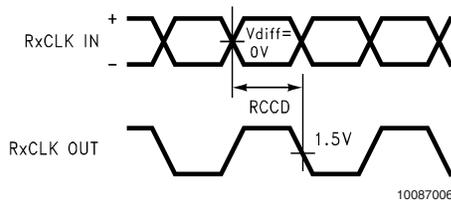


FIGURE 6. DS90CF384A/DS90CF364A (Receiver) Clock In to Clock Out Delay

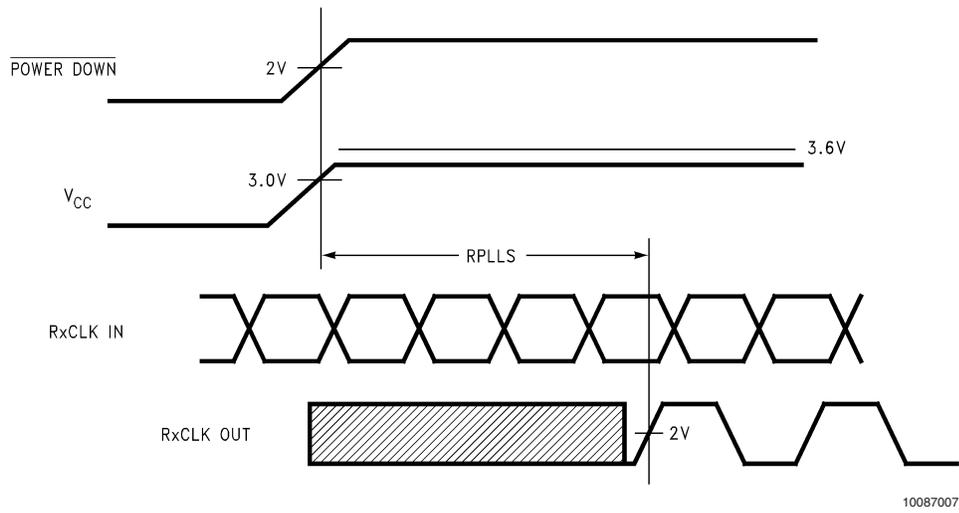


FIGURE 7. DS90CF384A/DS90CF364A (Receiver) Phase Lock Loop Set Time

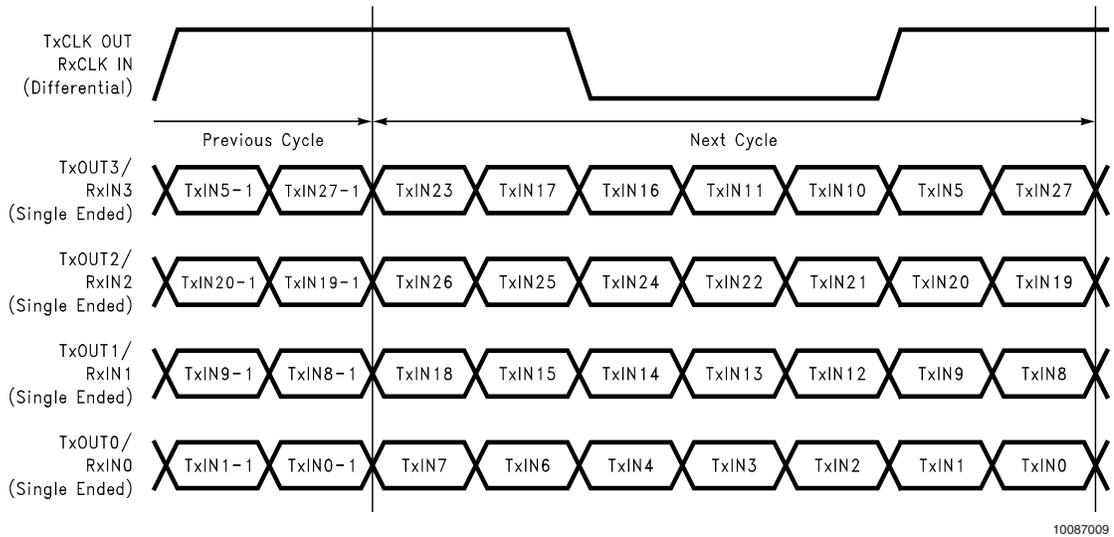
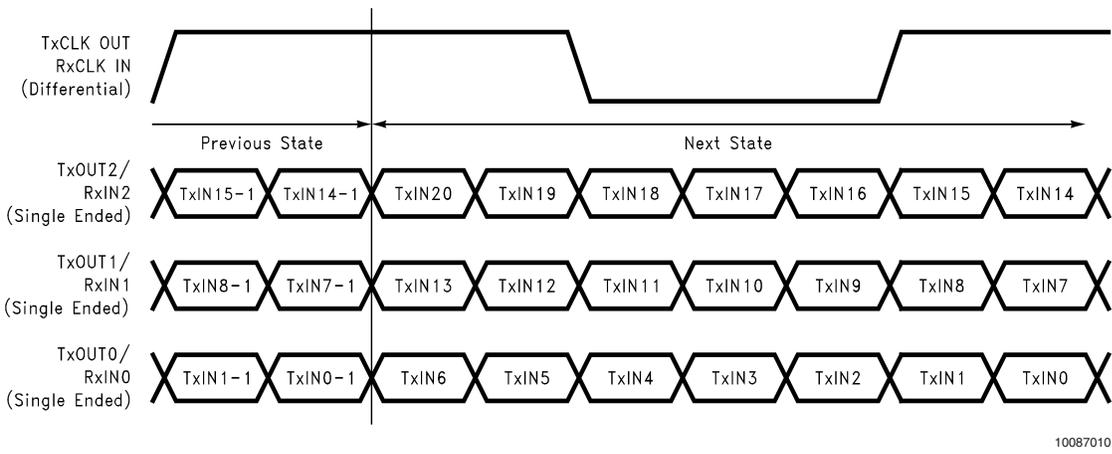
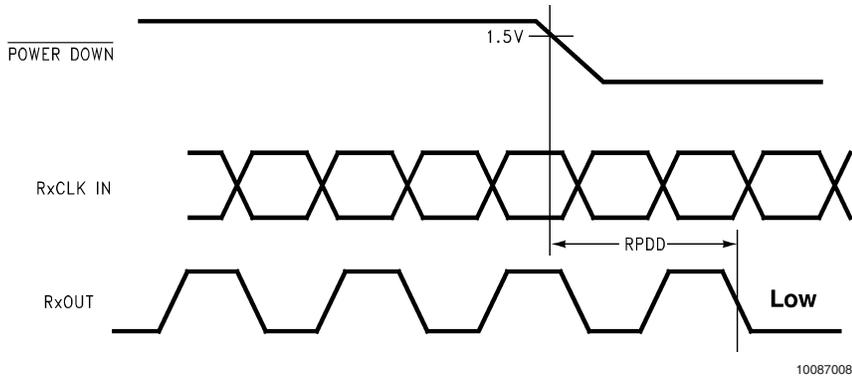


FIGURE 8. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF384A

**AC Timing Diagrams** (Continued)

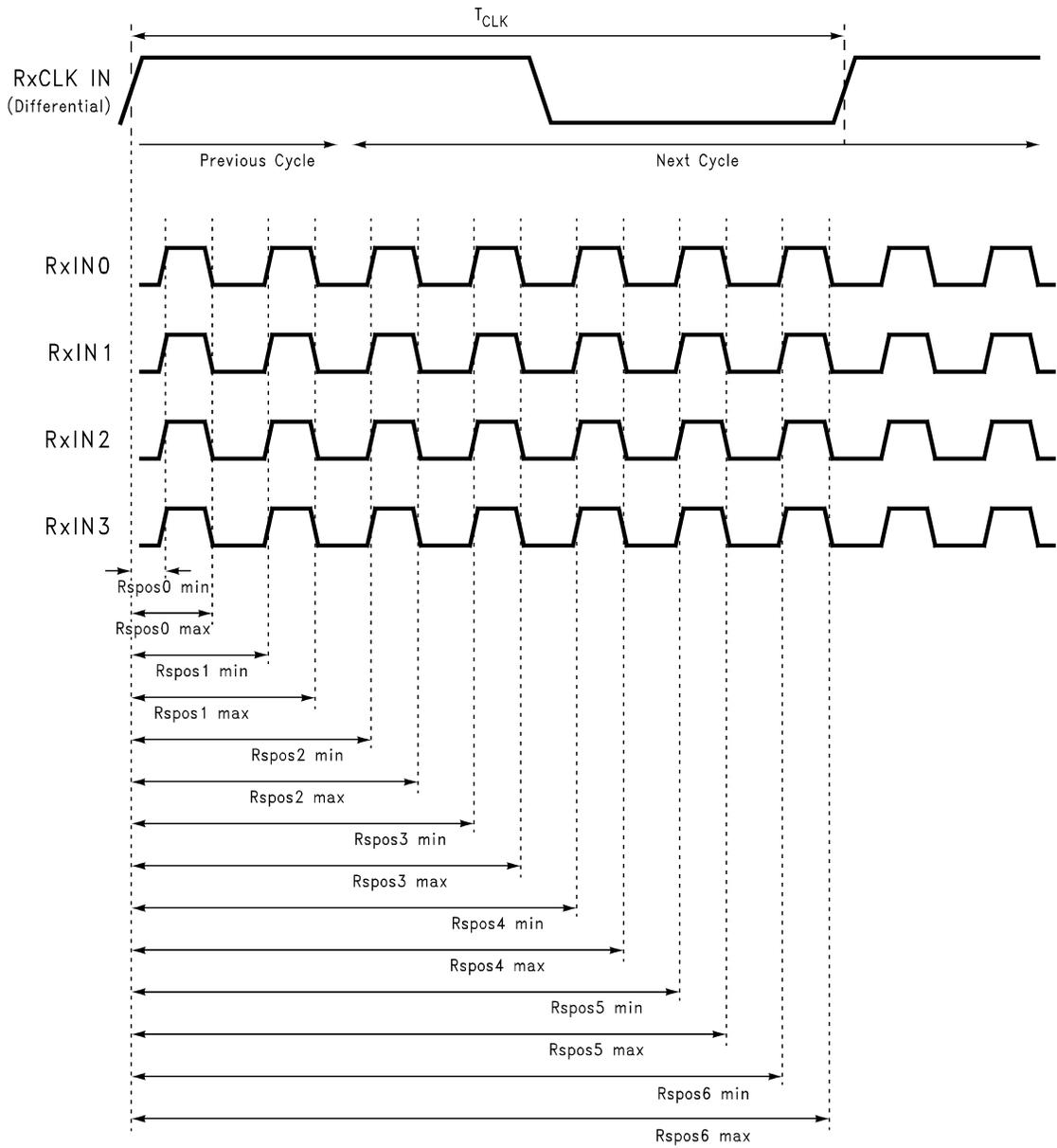


**FIGURE 9. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF364A**



**FIGURE 10. DS90CF384A/DS90CF364A (Receiver) Power Down Delay**

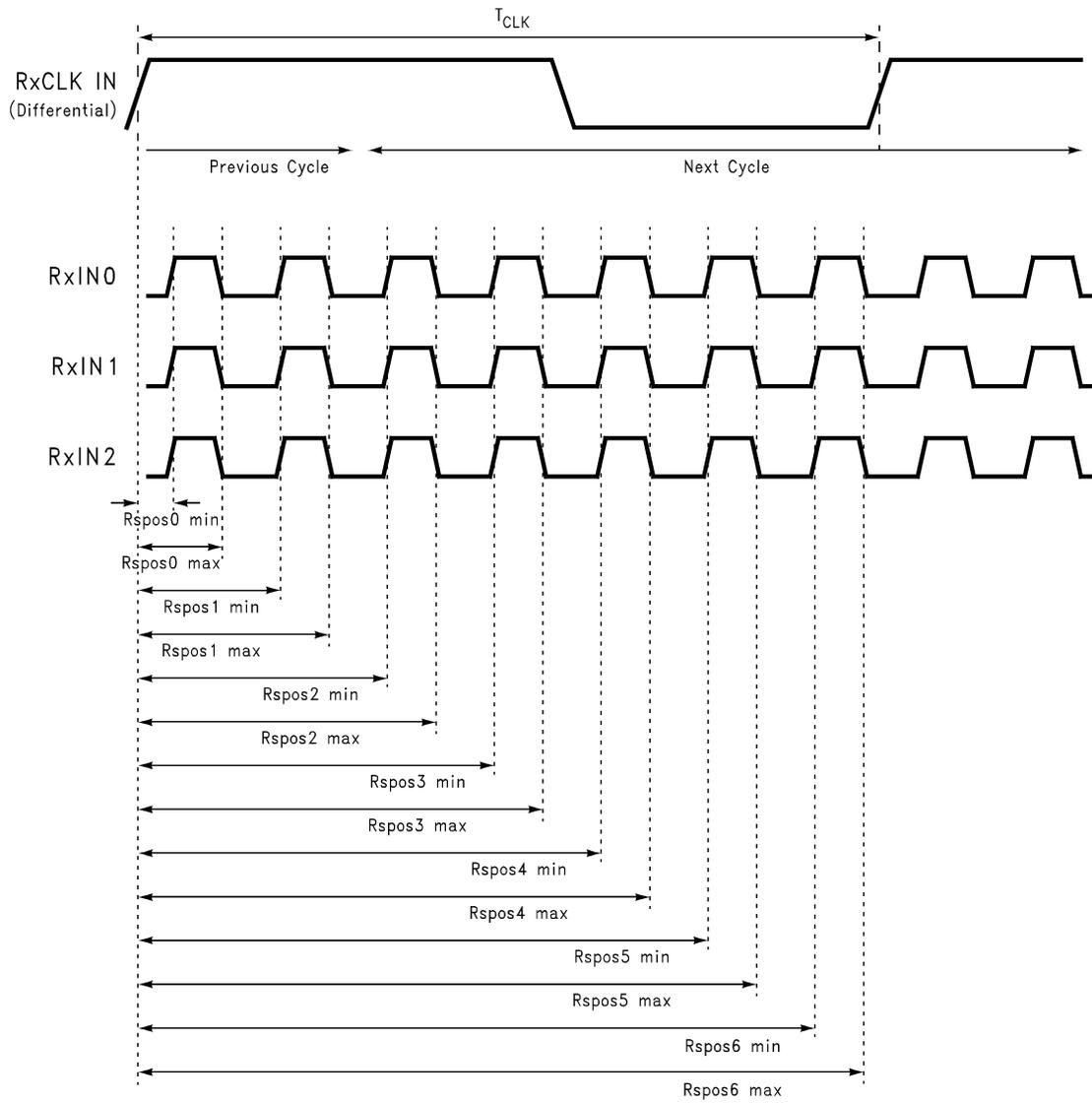
### AC Timing Diagrams (Continued)



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FIGURE 11. DS90CF384A (Receiver) LVDS Input Strobe Position

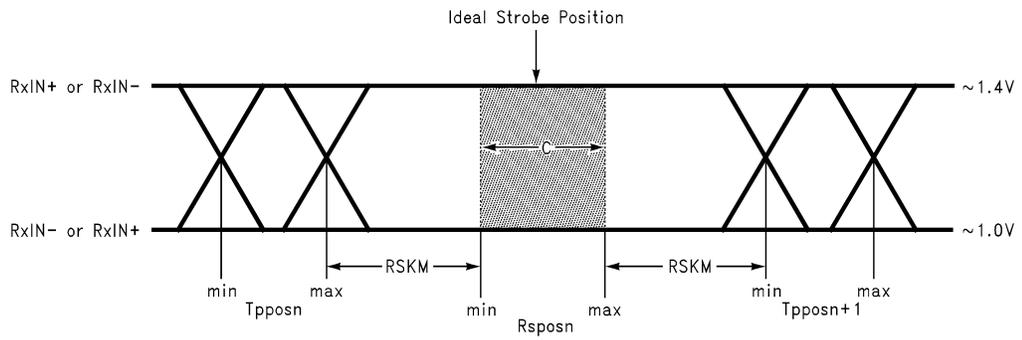
AC Timing Diagrams (Continued)



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FIGURE 12. DS90CF364A (Receiver) LVDS Input Strobe Position

## AC Timing Diagrams (Continued)



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C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max  
 Tppos—Transmitter output pulse position (min and max)  
 RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 9) + ISI (Inter-symbol interference) (Note 10)  
 Cable Skew—typically 10 ps–40 ps per foot, media dependent  
**Note 9:** Cycle-to-cycle jitter is less than 250 ps at 65 MHz.  
**Note 10:** ISI is dependent on interconnect length; may be zero.

**FIGURE 13. Receiver LVDS Input Skew Margin**

## DS90CF384A Pin Descriptions — 56L TSSOP Package — 24-Bit FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
PWR DOWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V <sub>CC</sub>	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

## DS90CF364A Pin Descriptions — 48L TSSOP Package — 18-Bit FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs.
RxIN-	I	3	Negative LVDS differential data inputs.
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
PWR DOWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V <sub>CC</sub>	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

## DS90CF384A Pin Summary — 64 ball FBGA Package — FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Also known as FPSHIFT OUT
PWR DOWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V <sub>CC</sub>	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.
NC		6	Pins not connected.

## DS90CF384A Pin Descriptions — 64 ball FBGA Package — FPD Link Receiver

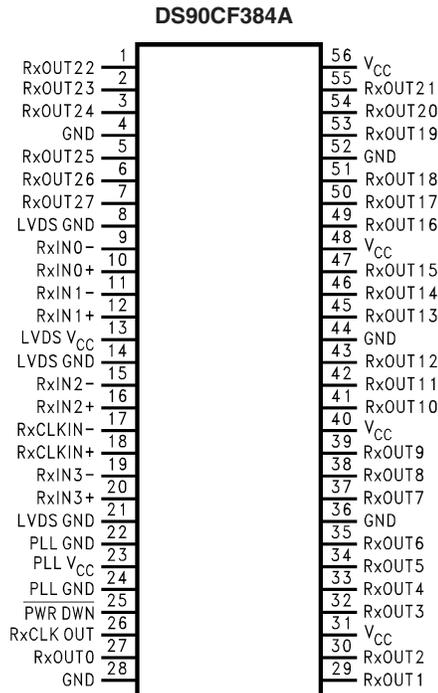
By Pin			By Pin Type		
Pin	Pin Name	Type	Pin	Pin Name	Type
A1	RxOUT17	O	A4	GND	G
A2	VCC	P	B1	GND	G
A3	RxOUT15	O	B6	GND	G
A4	GND	G	D8	GND	G
A5	RxOUT12	O	E3	GND	G
A6	RxOUT8	O	E5	LVDS GND	G
A7	RxOUT7	O	G3	LVDS GND	G
A8	RxOUT6	O	G7	LVDS GND	G
B1	GND	G	H5	LVDS GND	G
B2	NC		F6	PLL GND	G
B3	RxOUT16	O	G8	PLL GND	G
B4	RxOUT11	O	E6	PWR DWN	I
B5	VCC	P	H6	RxCLKIN-	I
B6	GND	G	H7	RxCLKIN+	I
B7	RxOUT5	O	H2	RxIN0-	I
B8	RxOUT3	O	H3	RxIN0+	I
C1	RxOUT21	O	F4	RxIN1-	I
C2	NC		G4	RxIN1+	I
C3	RxOUT18	O	G5	RxIN2-	I
C4	RxOUT14	O	F5	RxIN2+	I
C5	RxOUT9	O	G6	RxIN3-	I
C6	RxOUT4	O	H8	RxIN3+	I
C7	NC		E7	RxCLKOUT	O
C8	RxOUT1	O	E8	RxOUT0	O
D1	VCC	P	C8	RxOUT1	O
D2	RxOUT20	O	D5	RxOUT10	O
D3	RxOUT19	O	B4	RxOUT11	O

## DS90CF384A Pin Descriptions — 64 ball FBGA Package — FPD Link Receiver (Continued)

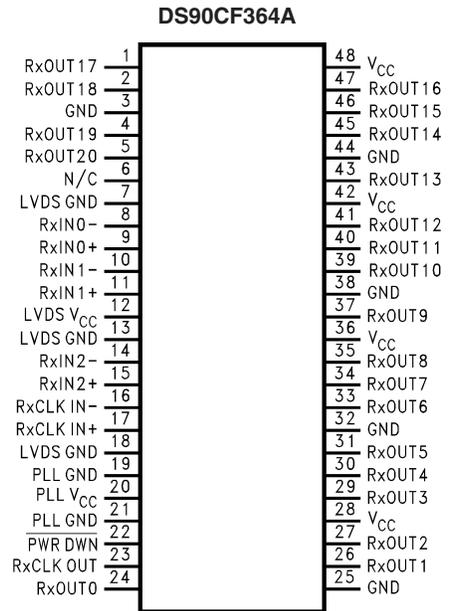
By Pin			By Pin Type		
D4	RxOUT13	O	A5	RxOUT12	O
D5	RxOUT10	O	D4	RxOUT13	O
D6	VCC	P	C4	RxOUT14	O
D7	RxOUT2	O	A3	RxOUT15	O
D8	GND	G	B3	RxOUT16	O
E1	RxOUT22	O	A1	RxOUT17	O
E2	RxOUT24	O	C3	RxOUT18	O
E3	GND	G	D3	RxOUT19	O
E4	LVDS VCC	P	D7	RxOUT2	O
E5	LVDS GND	G	D2	RxOUT20	O
E6	PWR DWN	I	C1	RxOUT21	O
E7	RxCLKOUT	O	E1	RxOUT22	O
E8	RxOUT0	O	F1	RxOUT23	O
F1	RxOUT23	O	E2	RxOUT24	O
F2	RxOUT26	O	G1	RxOUT25	O
F3	NC		F2	RxOUT26	O
F4	RxIN1-	I	H1	RxOUT27	O
F5	RxIN2+	I	B8	RxOUT3	O
F6	PLL GND	G	C6	RxOUT4	O
F7	PLL VCC	P	B7	RxOUT5	O
F8	NC		A8	RxOUT6	O
G1	RxOUT25	O	A7	RxOUT7	O
G2	NC		A6	RxOUT8	O
G3	LVDS GND	G	C5	RxOUT9	O
G4	RxIN1+	I	E4	LVDS VCC	P
G5	RxIN2-	I	H4	LVDS VCC	P
G6	RxIN3-	I	F7	PLL VCC	P
G7	LVDS GND	G	A2	VCC	P
G8	PLL GND	G	B5	VCC	P
H1	RxOUT27	O	D1	VCC	P
H2	RxIN0-	I	D6	VCC	P
H3	RxIN0+	I	B2	NC	
H4	LVDS VCC	P	C2	NC	
H5	LVDS GND	G	C7	NC	
H6	RxCLKIN-	I	F3	NC	
H7	RxCLKIN+	I	F8	NC	
H8	RxIN3+	I	G2	NC	

G: Ground  
 I : Input  
 O: Output  
 P: Power  
 NC: Not connected

# Pin Diagram for TSSOP Packages



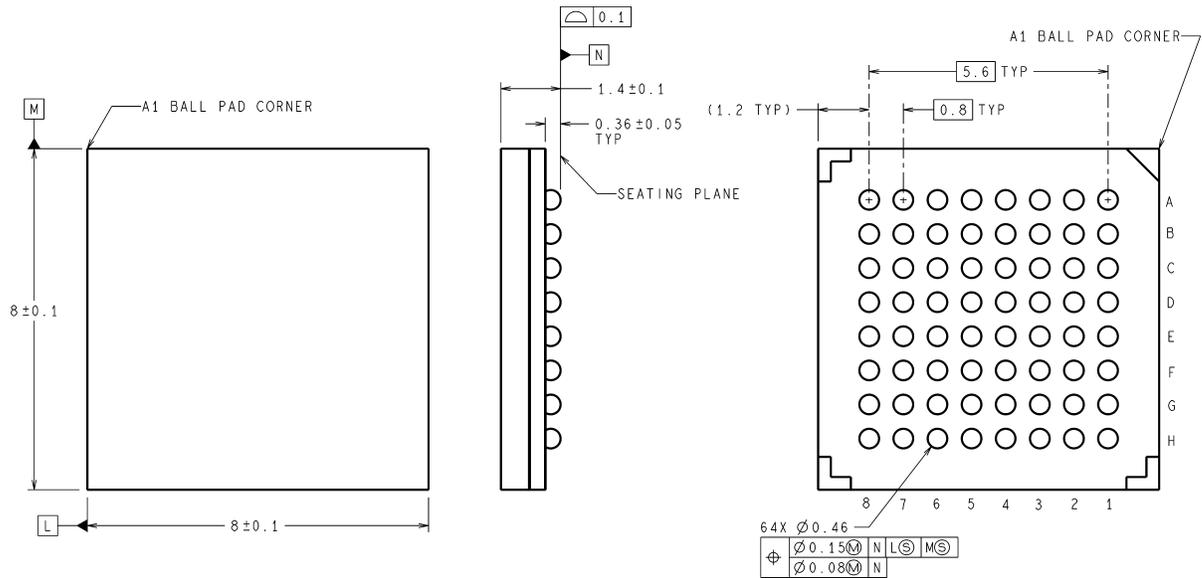
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**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

SLC64A (Rev C)

**64 ball, 0.8mm Fine Pitch Ball Grid Array (FBGA) Package**  
 Dimensions shown in millimeters only  
 Order Number DS90CF384ASLC  
 NS Package Number SLC64A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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