



IPAD™

EMIF03-SIM02F2

3 LINE EMI FILTER INCLUDING ESD PROTECTION

MAIN PRODUCT APPLICATIONS:

EMI filtering and ESD protection for:

- SIM Interface (Subscriber Identify Module)
- UIM Interface (Universal Identify Module)

DESCRIPTION

The EMIF03-SIM02F2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The EMIF03 flip chip packaging means the package size is equal to the die size. This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming:
1.42mm x 1.42mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

Level 4 on external & V_{CC} pins:

15kV (air discharge)
8kV (contact discharge)

Level 1 on internal pins:

2kV (air discharge)
2kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3

Figure 2: Configuration

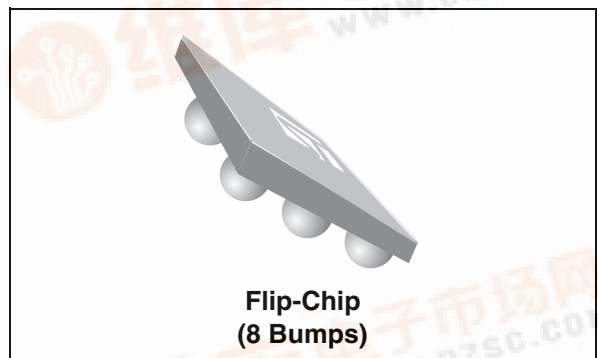
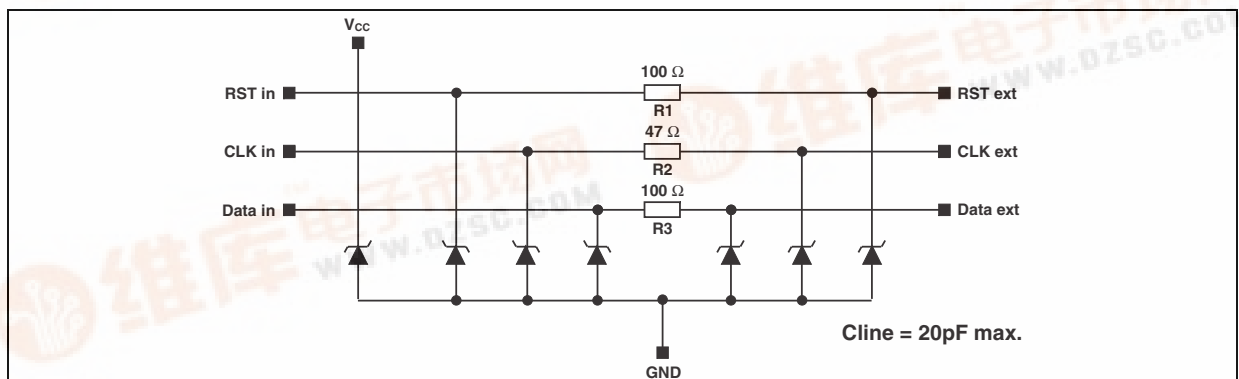
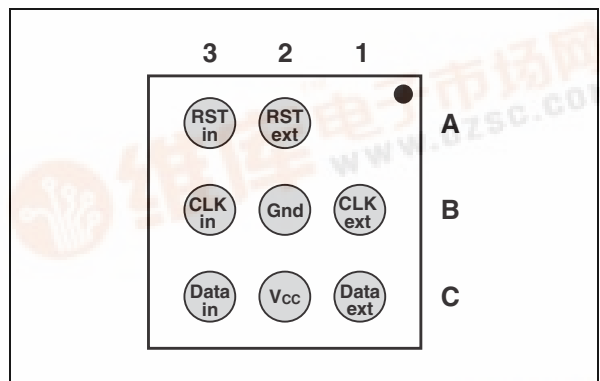


Table 1: Order Code

Part Number	Marking
EMIF03-SIM02F2	GJ

Figure 1: Pin Configuration (Ball side)



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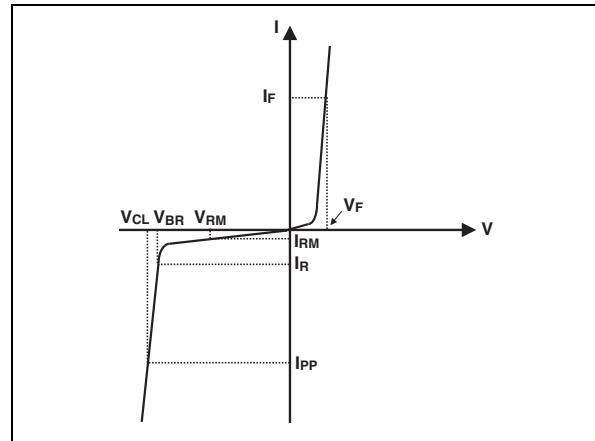
EMIF03-SIM02F2

Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	Internal pins (A3, B3, C3):		
	ESD discharge IEC61000-4-2, air discharge	2	
	ESD discharge IEC61000-4-2, contact discharge	2	
	External pins (A2, B1, C2, C1):		
	ESD discharge IEC61000-4-2, air discharge	15	
	ESD discharge IEC61000-4-2, contact discharge	8	
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	6		20	V
I_{RM}	$V_{RM} = 3\text{V}$			0.2	μA
R_d			1.5		Ω
R_1, R_3	Tolerance $\pm 20\%$		100		Ω
R_2	Tolerance $\pm 20\%$		47		Ω
C_{line}	@ 0V			20	pF

Figure 3: S21 (dB) attenuation measurement (A2-A3 line)

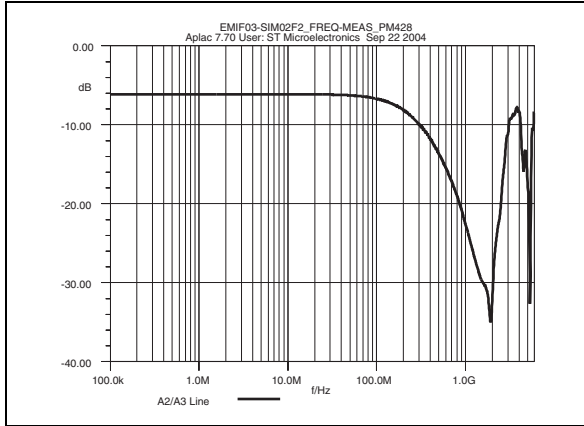


Figure 4: S21 (dB) attenuation measurement (B1-B3 line)

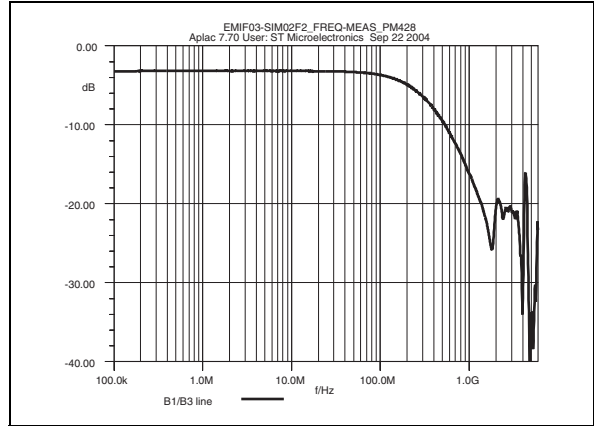


Figure 5: S21 (dB) attenuation measurement (C1-C3 line)

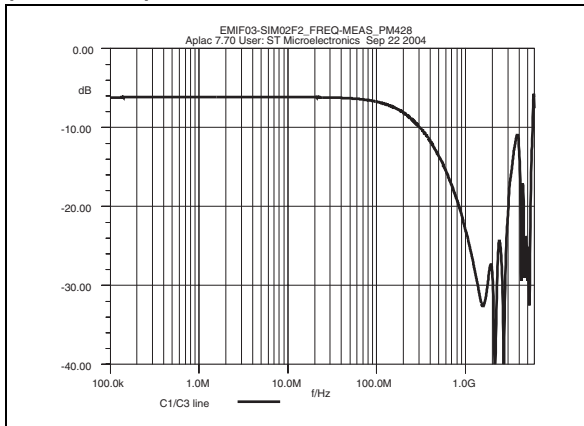


Figure 6: Analog crosstalk measurements

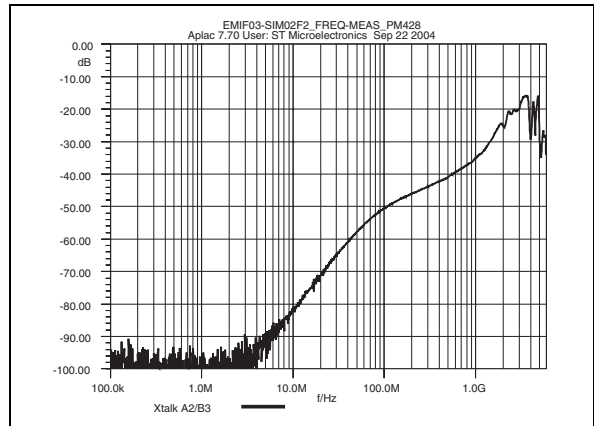


Figure 7: Voltages when IEC61000-4-2 (+15 kV air discharge) applied to external pin

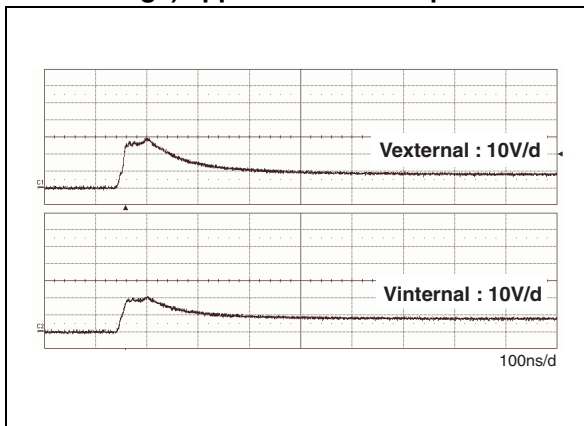


Figure 8: Voltages when IEC61000-4-2 (-15 kV air discharge) applied to external pin

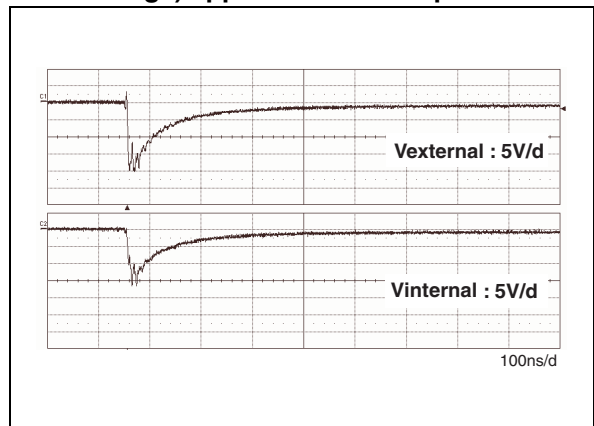


Figure 9: Line capacitance versus reverse applied voltage (typical)

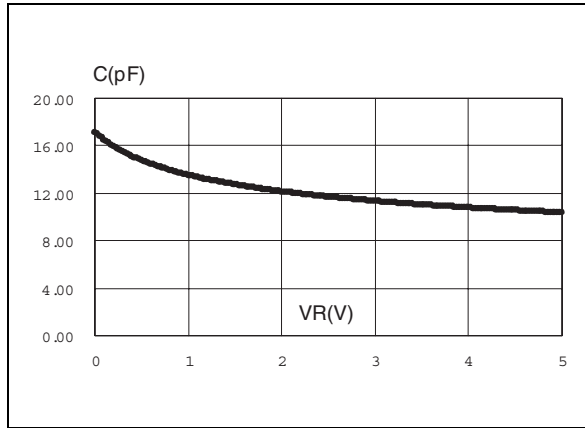


Figure 10: Aplan model

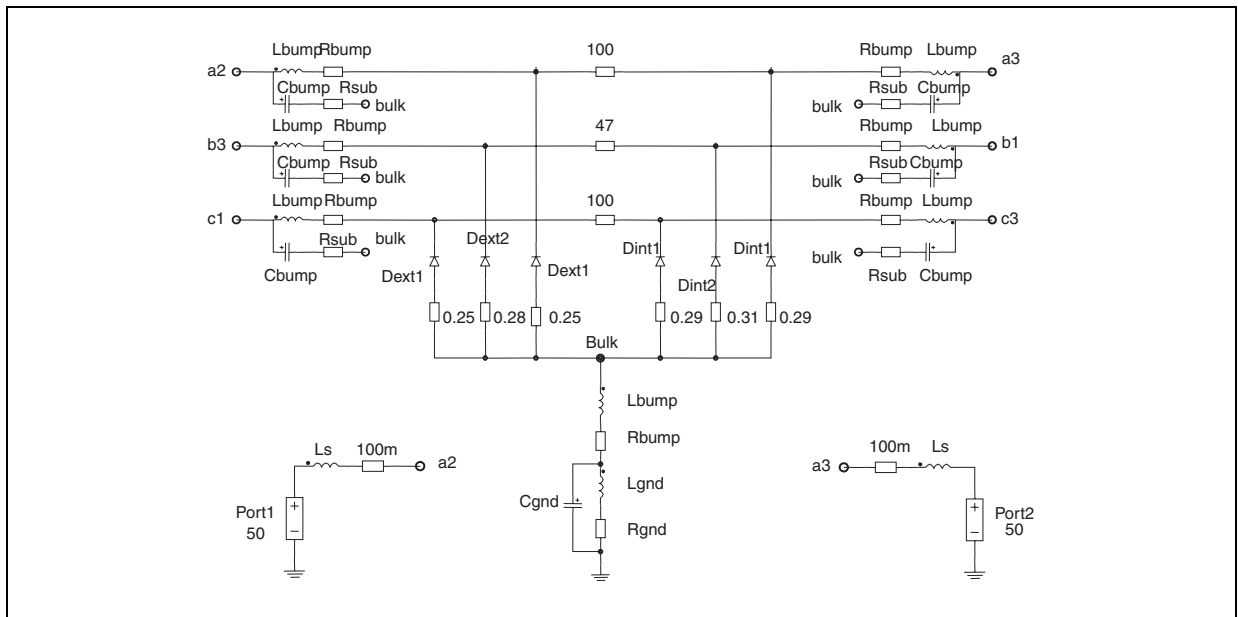


Figure 11: Aplan parameters

Ls 950pH				
Rs 150m	<u>Model Dint1</u>	<u>Model Dext1</u>	<u>Model Dint2</u>	<u>Model Dext2</u>
Cext1 15pF	BV=15	BV=15	BV=15	BV=15
Cint1 4.5pF	CJO=Cint1	CJO=Cext1	CJO=Cint2	CJO=Cext2
Cext2 14pF	IBV=1u	IBV=1u	IBV=1u	IBV=1u
Cint2 4pF	IKF=1000	IKF=1000	IKF=1000	IKF=1000
Rbump 20m	IS=10f	IS=10f	IS=10f	IS=10f
Lbump 50pH	ISR=100p	ISR=100p	ISR=100p	ISR=100p
Cbump 0.15pF	N=1	N=1	N=1	N=1
Rgnd 500m	M=0.3333	M=0.3333	M=0.3333	M=0.3333
Lgnd 50pH	RS=0.001m	RS=0.001m	RS=0.001m	RS=0.001m
Cgnd 0.15pF	VJ=0.6	VJ=0.6	VJ=0.6	VJ=0.6
Rsub 100m	TT=50n	TT=50n	TT=50n	TT=50n

Figure 12: Ordering Information Scheme

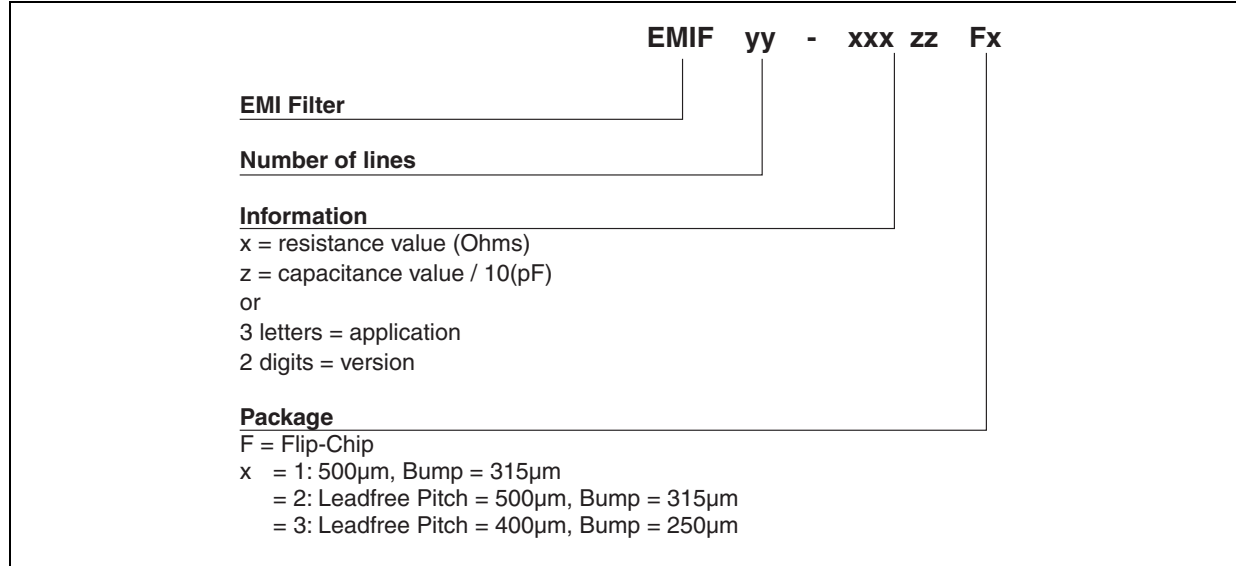


Figure 13: FLIP-CHIP Package Mechanical Data

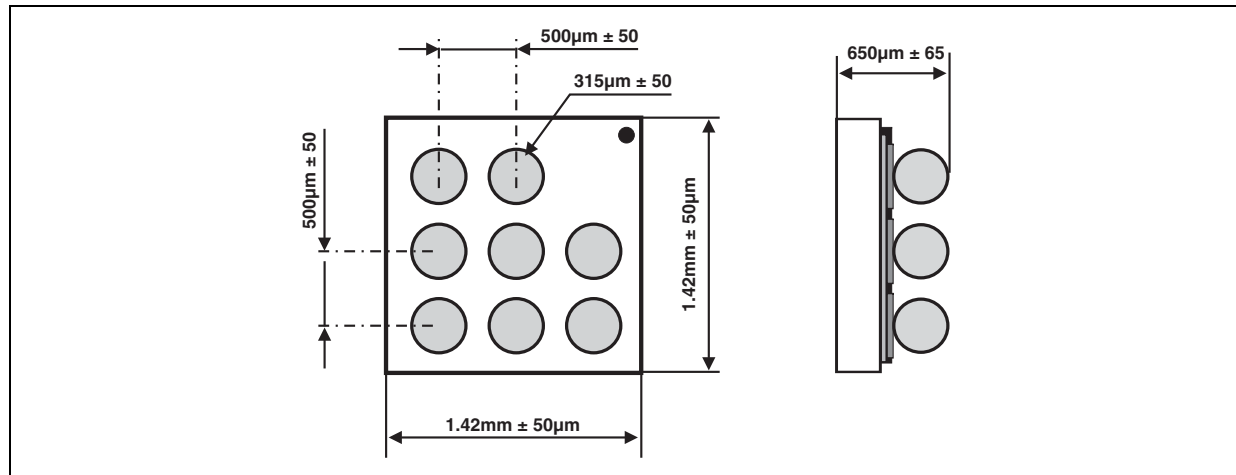


Figure 14: Foot print recommendations

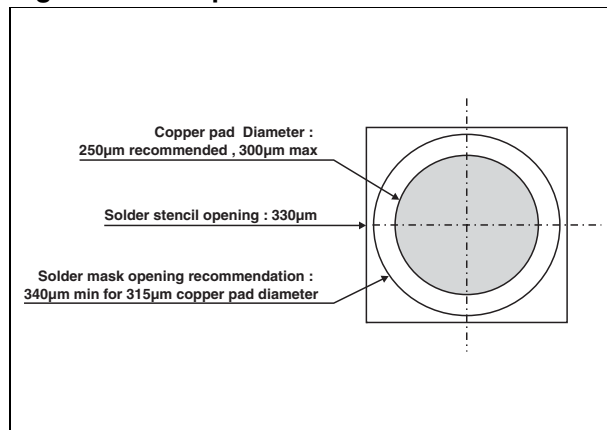
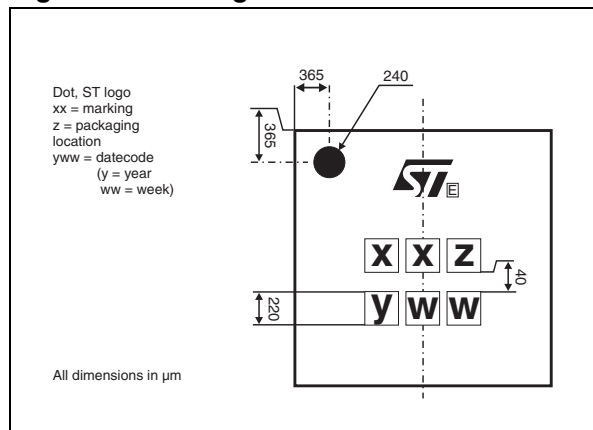


Figure 15: Marking



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