FAIRCHILD SEMICONDUCTOR®

August 2006

FDY4001CZ

Complementary N & P-Channel PowerTrench® MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5Ω at V_{GS} = 4.5V, I_D = 200mA
- Max $r_{DS(on)}$ = 7Ω at V_{GS} = 2.5V, I_D = 175mA
- Max $r_{DS(on)}$ = 9Ω at V_{GS} = 1.8V, I_D = 150mA

Q2: P-Channel

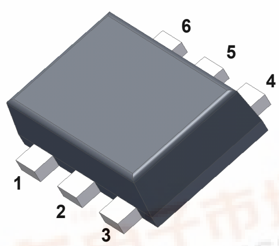
- Max $r_{DS(on)}$ = 8Ω at V_{GS} = -4.5V, I_D = -150mA
- Max $r_{DS(on)}$ = 12Ω at V_{GS} = -2.5V, I_D = -125mA
- Max $r_{DS(on)}$ = 15Ω at V_{GS} = -1.8V, I_D = -100mA
- ESD protection diode (note 3)
- RoHS Compliant

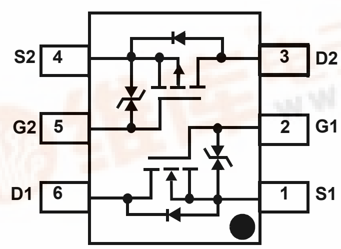
General Description

This Complementary N & P-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench® process to optimize the $r_{DS(ON)}$ @ V_{GS}=2.5V and specify the $r_{DS(ON)}$ @ V_{GS} = 1.8V.

Applications

- Level shifting
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		20	-20	V
V_{GS}	Gate to Source Voltage		±12	±8	V
I_D	Drain Current -Continuous	(Note 1a)	200	-150	mA
	-Pulsed		1000	-1000	
P_D	Power Dissipation (Steady State)	(Note 1a)	625		mW
		(Note 1b)	446		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to 150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
F	FDY4001CZ	SC89-6	7"	8mm	3000units

Electrical Characteristics T_J = 25°C unlessotherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V I_D = -250µA, V_{GS} = 0V	Q1 Q2	20 -20			V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C I_D = -250µA, referenced to 25°C	Q1 Q2		14 -15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{DS} =0V V_{DS} = -16V, V_{DS} =0V	Q1 Q2			1 -3	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±12V, V_{DS} = 0V V_{GS} = ±4.5V, V_{DS} = 0V V_{GS} = ±8V, V_{DS} = 0V	Q1 Q1 Q2			±10 ±1 ±10	µA
On Characteristics (note 2)							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA V_{GS} = V_{DS}, I_D = -250µA	Q1 Q2	0.6 -0.65	 -1.0	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C I_D = -250µA, referenced to 25°C	Q1 Q2		2.8 -3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 200mA V_{GS} = 2.5V, I_D = 175mA V_{GS} = 1.8V, I_D = 150mA V_{GS} = 1.5V, I_D = 20mA V_{GS} = 4.5V, I_D = 200mA,T_J = 125°C	Q1			5 7 9 10 7	Ω
		V_{GS} = -4.5V, I_D = --150mA V_{GS} = -2.5V, I_D = -125mA V_{GS} = -1.8V, I_D = -100mA V_{GS} = -1.5V, I_D = -30mA V_{GS} = -4.5V, I_D = -150mA,T_J =125°C	Q2			8 12 15 20 12	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 200mA V_{DS} = -5V, I_D = -150mA	Q1 Q2		1.1 0.7		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 10V, V_{GS} = 0V, f = 1MHz Q2 V_{DS} = -10V, V_{GS} = 0V, f = 1MHz	Q1 Q2		60 100		pF
C_{oss}	Output Capacitance		Q1 Q2		20 30		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		10 15		pF
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD}= 10V, I_D = 1A, V_{GS}= 4.5V, R_g = 6Ω Q2 V_{DD}= -10V, I_D = -0.5A, V_{GS}= -4.5V, R_g = 6Ω	Q1 Q2		6 6	12 12	ns
t_r	Rise Time		Q1 Q2		8 13	16 23	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		8 8	16 16	ns
t_f	Fall Time		Q1 Q2		2.4 1	4.8 2	ns
Q_g	Total Gate Charge	Q1 V_{DS}= 10V, I_D = 200mA, V_{GS}= 4.5V Q2 V_{DS}= -10V, I_D = -150mA, V_{GS}= -4.5V	Q1 Q2		0.8 1.0	1.1 1.4	nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		0.16 0.2		nC
Q_{gd}	Gate to Drain "Miller"Charge		Q1 Q2		0.26 0.3		nC

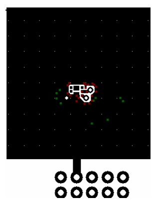
Electrical Characteristics T_J = 25°C unless otherwise noted

Drain-Source Diode Characteristics

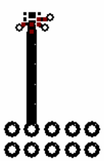
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 150mA (Note 2) V_{GS} = 0V, I_S = -150mA (Note 2)	Q1 Q2		0.7 -0.8	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 200mA, di/dt = 100A/µs Q2 I_F = -150mA, di/dt = 100A/µs	Q1 Q2		12 11		ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2		3 2		nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 200°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 280°C/W when mounted on a minimum pad of 2 oz copper

Scale 1:1 on letter size paper

2: Pulse Test : Pulse Width < 300us, Duty Cycle < 2.0%

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics Q1 (N-Channel)

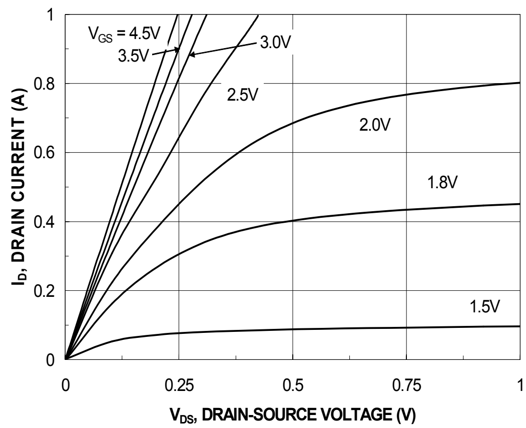


Figure 1. On-Region Characteristics.

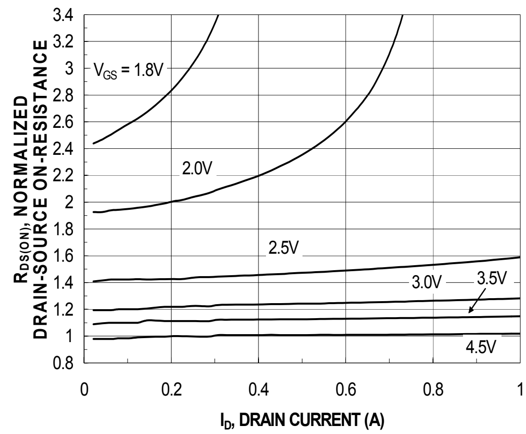


Figure 2. Normalized on-Resistance vs. Drain Current and Gate Voltage.

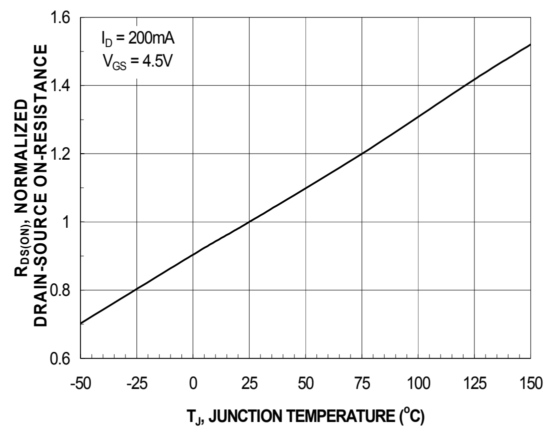


Figure 3. Normalized on-Resistance vs. Temperature.

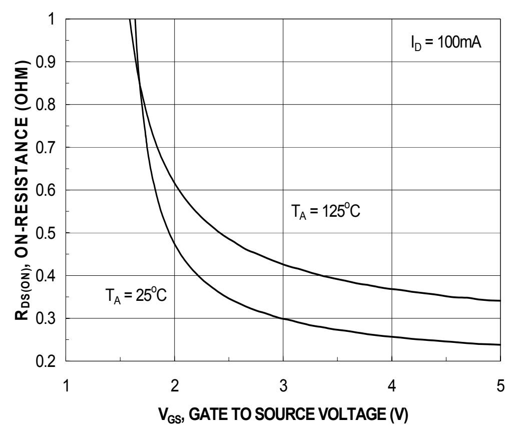


Figure 4. On-Resistance vs. Gate-to-Source Votlage.

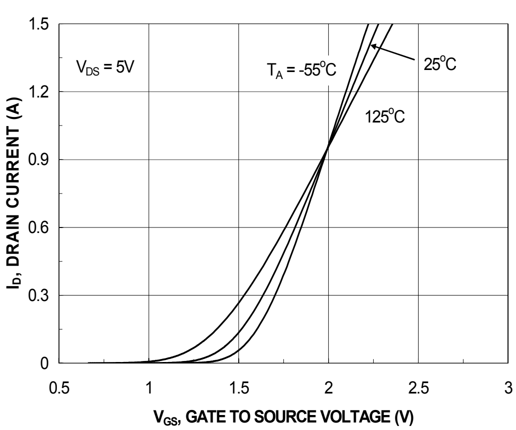


Figure 5. Transfer Characteristics.

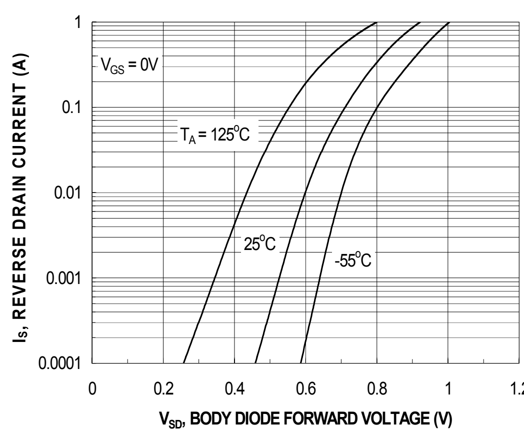


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current and Temperature.

Typical Characteristics Q1 (N-Channel)

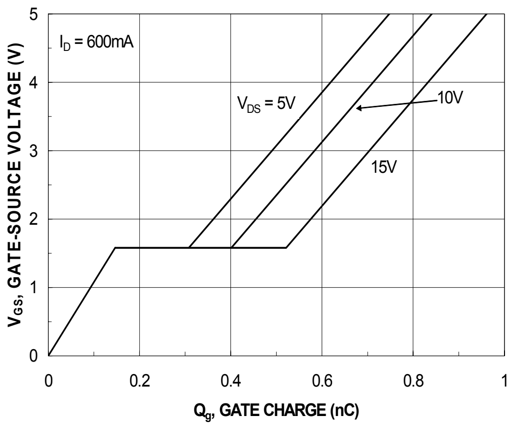


Figure 7. Gate Charge Characteristics.

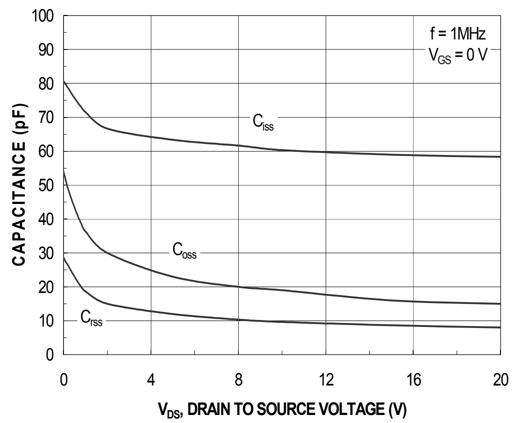


Figure 8. Capacitance vs. Drain to source voltage.

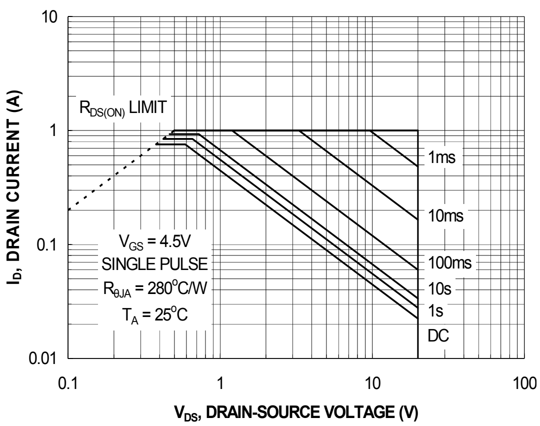


Figure 9. Maximum Safe Operating Area.

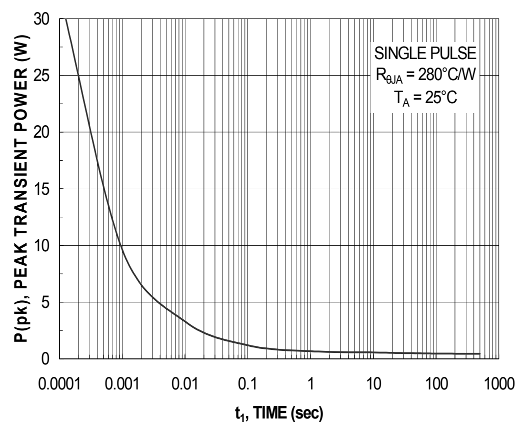


Figure 10. Single Pulse Maximum Power Dissipation.

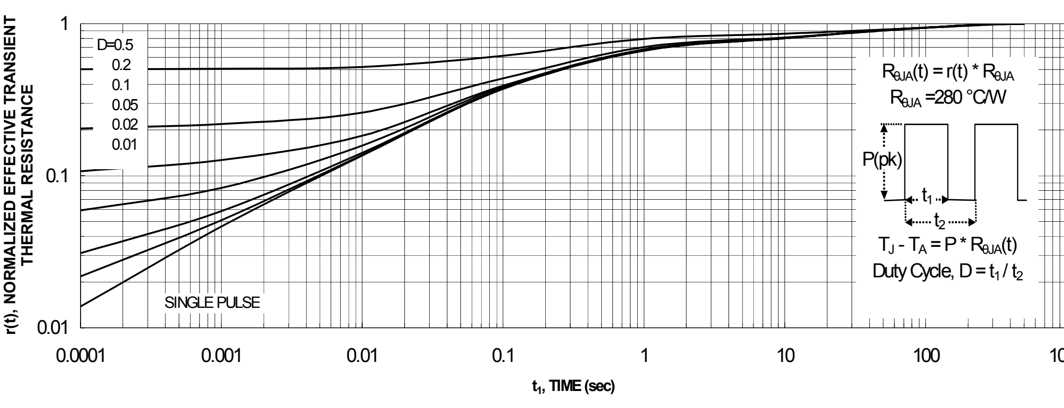
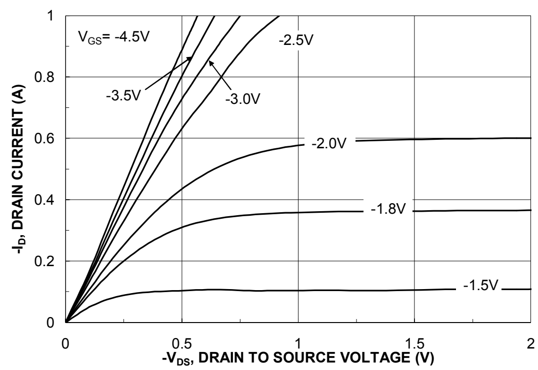


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics Q2 (P-Channel)



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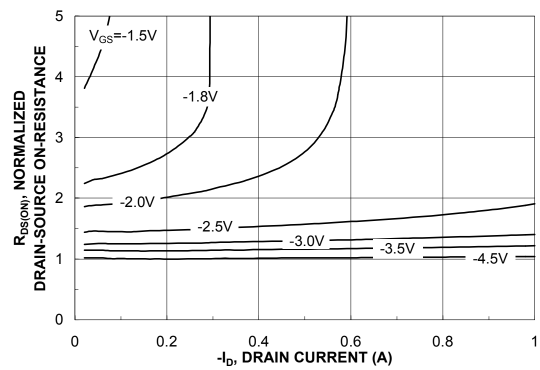


Figure 2. Normalized on-Resistance vs. Drain Current and Gate Voltage.

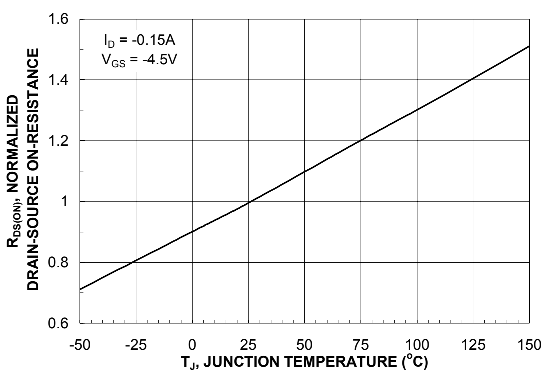


Figure 3. Normalized on-Resistance vs. Temperature.

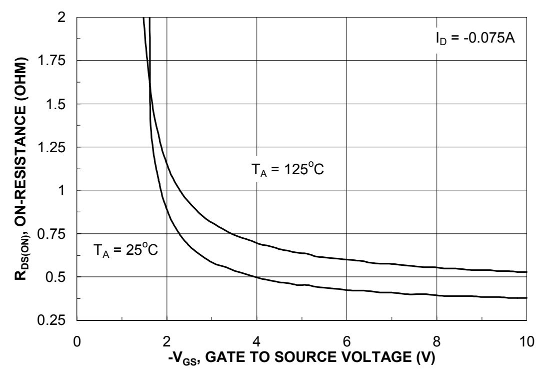


Figure 4. On-Resistance vs. Gate-to-Source Voltage.

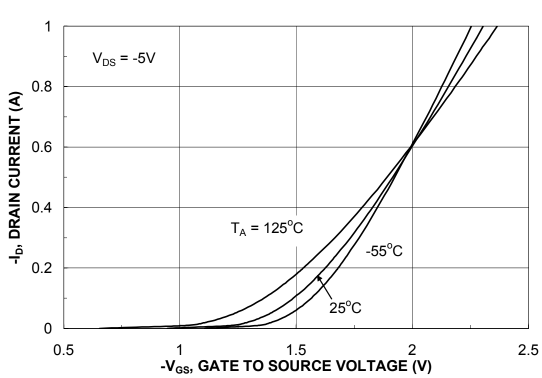


Figure 5. Transfer Characteristics.

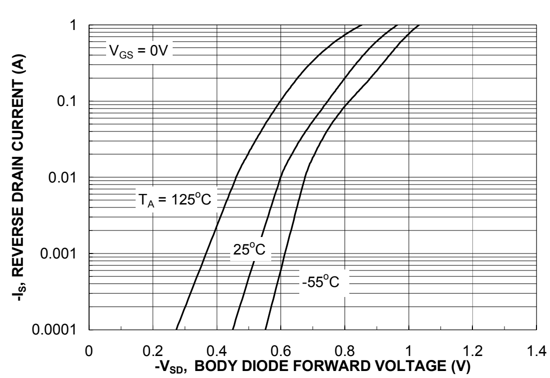


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current and Temperature.

Typical Characteristics Q2 (P-Channel)

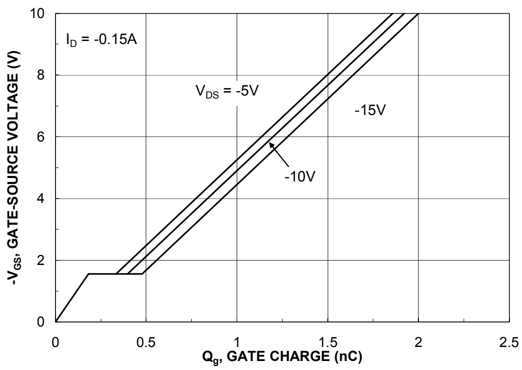
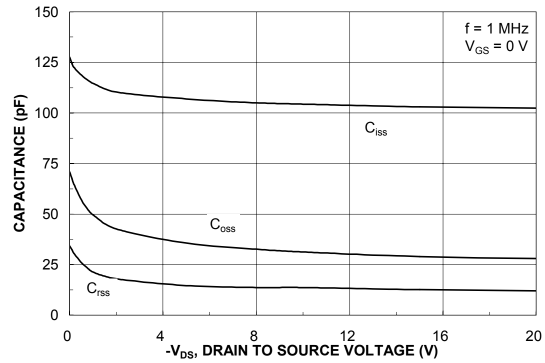


Figure 7. Gate Charge Characteristics.



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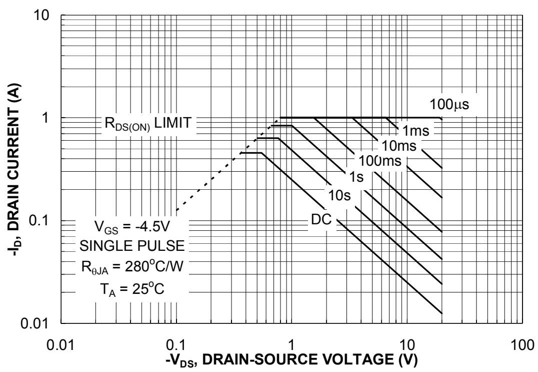

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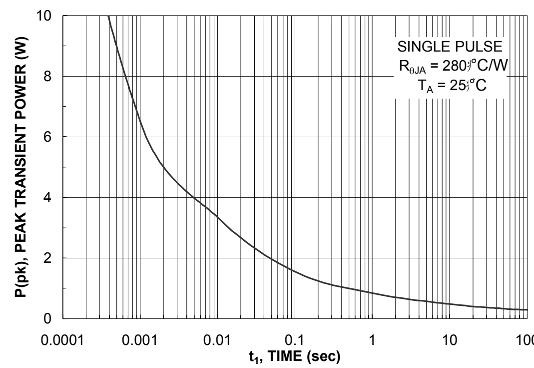


Figure 10. Single Pulse Maximum Power Dissipation.

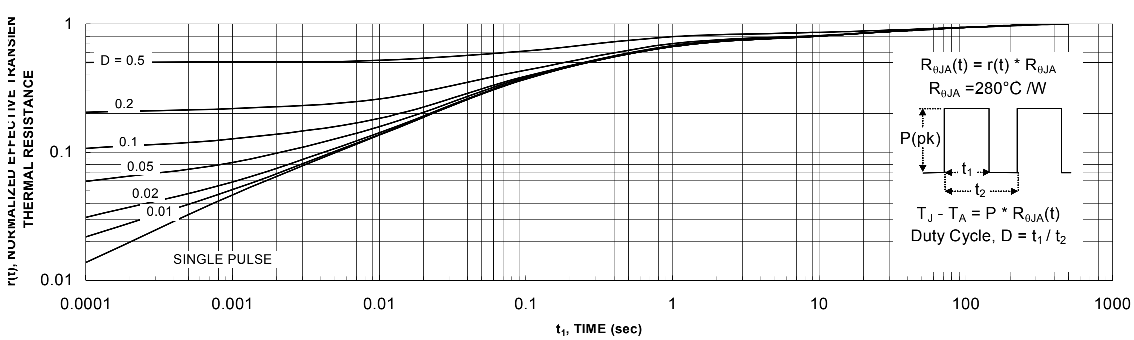
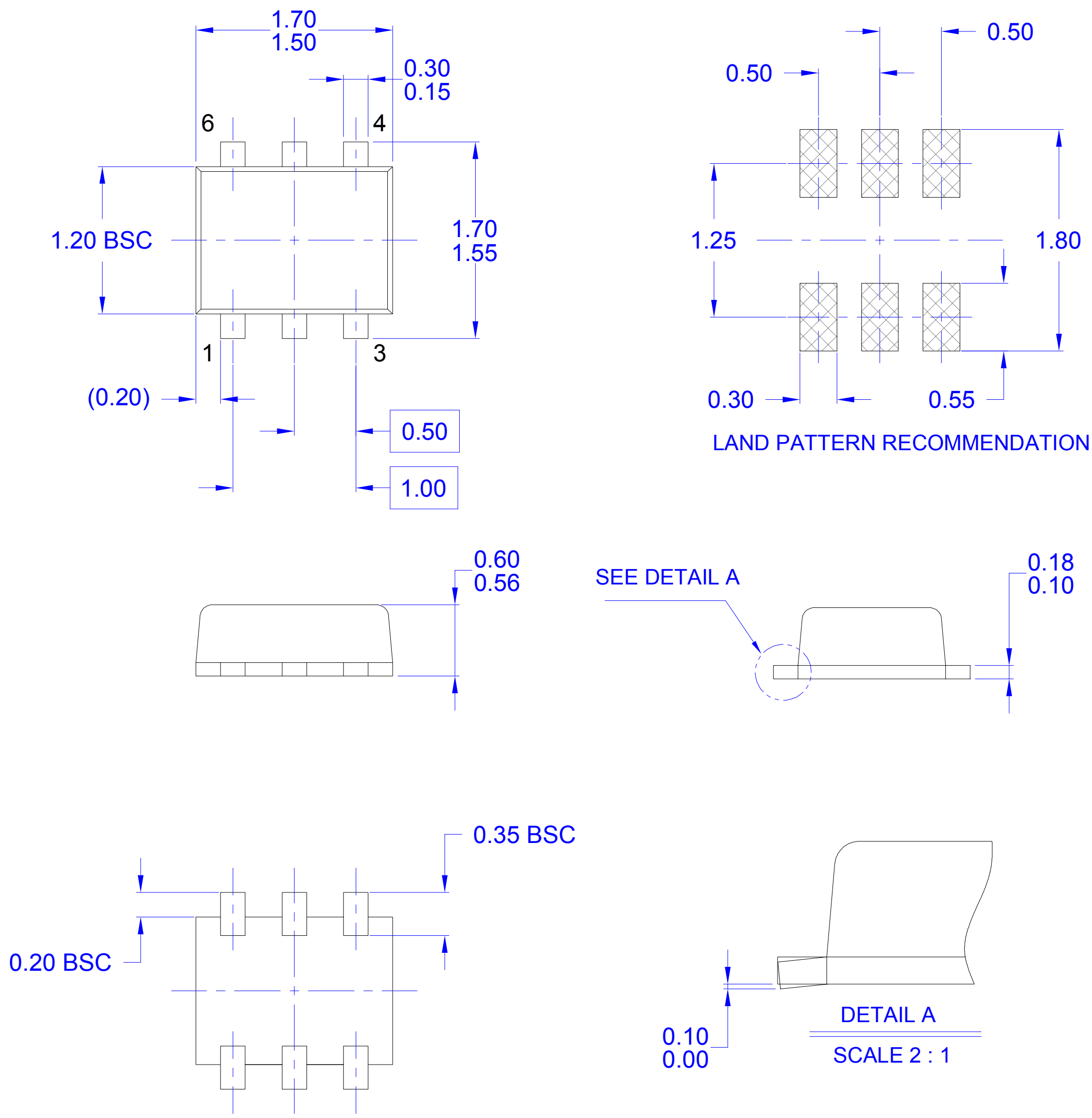


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.