FAIRCHILD SEMICONDUCTOR®

March 2007

µSerDes™ **FIN324C**

24-Bit Ultra-Low Power Serializer Deserializer Supporting Single and Dual Displays

Features

- Ultra-Low Operating Power: ~4mA at 5.44MHz
- Supports Dual-Display Implementations with RGB or Microcontroller Interface
- No External Timing Reference Needed
- SPI Mode Support
- Single Device Operates as a Serializer or Deserializer
- Direct Support for Motorola®-Style R/W Microcontroller Interface
- Direct Support for Intel®-Style /WE, /RE Microcontroller Interface
- 15MHz Maximum Strobe Frequency
- Utilizes Fairchild's Proprietary CTL Serial I/O Technology
- Available in BGA and MLP packages
- Wide Parallel Supply Voltage Range: 1.60 to 3.0V
- Low Power Core Operation: $V_{DDS/A}$=2.5 to 3.0V
- Voltage Translation Capability Across Pair with No External Components
- High ESD protection: >14.5kV HBM
- Power-Saving Burst-Mode Operation

Applications

- Single or Dual 16/18-Bit RGB Cell Phone Displays
- Single or Dual 16/18-Bit Cell Phone Displays with Microcontroller Interface
- Single or Dual Mobile Display at QVGA or HVGA Resolution

Description

The FIN324C is a 24-bit serializer / deserializer with dual strobe inputs. The device can be configured as a master or slave device through the master/slave select pin (M/S). This allows for the same device to be used as either a serializer or deserializer, minimizing component types in the system. The dual strobe inputs allow implementation of dual-display systems with a single pair of µSerDes. The FIN324C can accommodate RGB, microcontroller, or SPI mode interfaces. Read and write transactions are supported when operating with a Motorola-style microcontroller interface for one or both displays. Unlike other SerDes solutions, no external timing reference is required for operation.

The FIN324C is designed for ultra-low power operation. Reset (/RES) and standby (/STBY) signals put the device in an ultra-low power state. In standby mode, the outputs of the slave device maintain state, allowing the system to resume operation from the last-known state.

The device utilizes Fairchild's proprietary ultra-low power, low-EMI Current Transfer Logic™ (CTL) technology. The serial interface disables between transactions to minimize EMI at the fundamental serial interface and to conserve power. LV-CMOS parallel output buffers have been implemented with slew rate control to adjust for capacitive loading and to minimize EMI.

The serialization bit clock is generated internally to the FIN324C. The minimum bit clock frequency is always great enough to handle the maximum strobe frequency.

Related Application Notes

- *AN-5058 µSerDes™ Family Frequently Asked Questions*
- *AN-5061 µSerDes™ Layout Guidelines*
- *AN-6047 FIN324C Reset and Standby*

Ordering Information

Order Number	Package	Pb-Free	Operating Temperature Range	Package Description	Packing Method
FIN324CMLX	MLP040A	Yes	-30 C to 70 C	40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square	Tape & Reel
FIN324CGFX	BGA42A	Yes	-30 C to 70 C	42-Ball, Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5 x 4.5mm Wide, 0.5mm Ball Pitch	Tape & Reel

Typical Application Diagram

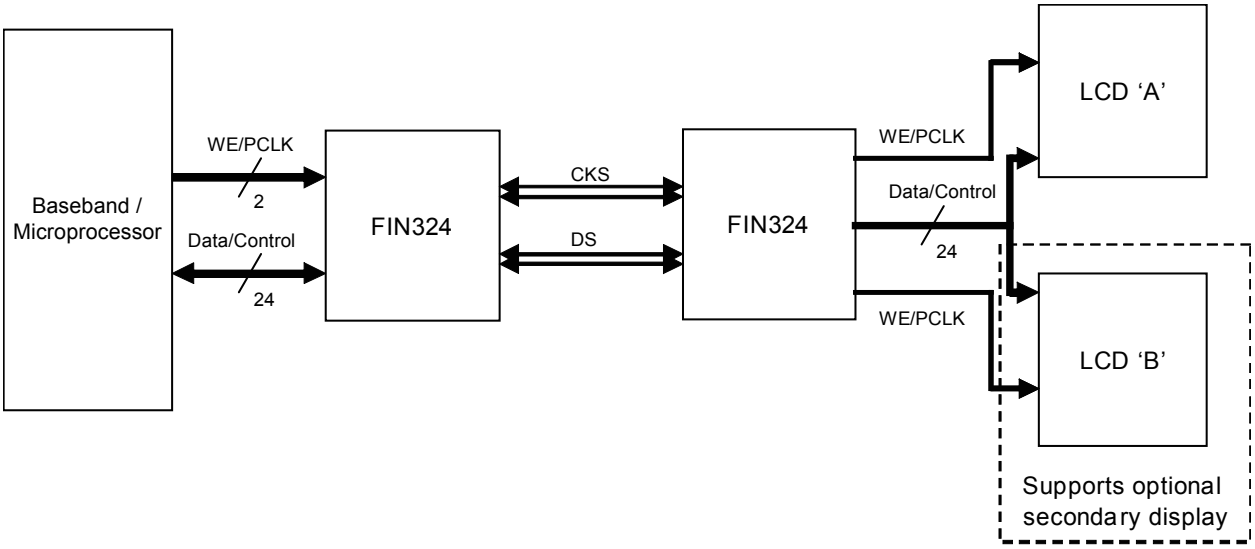


Figure 1. Typical Application Diagram

Pin Definitions

Pin	I/O Type	# Pins	Description of Signals
Chip-Level Control Signals			
M/S	IN	1	LV-CMOS Master/Slave Control Input: M/S=1 MASTER, M/S =0 SLAVE
/RES	IN	1	LV_CMOS RESET signal and power-down signal /RES=0: Resets and powers down all circuitry /RES=1: Device enabled
/STBY(SLEW)	IN	1	LV-CMOS standby signal or output slew rate signal: M/S=1: /STBY M/S=0: RSLEW /STBY=0: Device powered down RSLEW=1: Fast edge rate RSLEW=0: Slow edge rate
PAR/SPI	IN	1	LV-CMOS parallel / SPI display interface Tells the SerDes it is interfacing with a sub-display with a SPI interface PAR/SPI=1: Parallel Interface PAR/SPI=0: SPI Interface using STRB0(WCLK0)
CKSEL(H)	IN	1	LV-CMOS Input: Master clock source select input. When M/S=1: CKSEL (passed in serial stream) CKSEL=1: STRB1(WCLK1) Active CKSEL=0: STRB0(WCLK0) Active When M/S=0: This pin must be tied to VDDP.
Parallel Interface Signals Master Functionality (Slave Functionality)			
DP[17:0] DP[6]({SCLK}) DP[7]({SDAT})	I/O	18	LV-CMOS data I/O. I/O direction controlled by M/S pin and R/W internal state. DP[6] SPI mode SCLK signal pin when PAR/SPI=0 (Slave Only) DP[7] SPI mode SDAT signal pin when PAR/SPI=0(Slave Only)
CNTL[5:0] {SCLK}CNTL[5] {SDAT}CNTL[4]	I/O	6	LV-CMOS data I/O. I/O direction controlled by M/S pin M/S=1: Inputs M/S=0: Outputs In SPI mode, CNTL[5] is SCLK; CNTL[4] is SDAT for master and slave
R/W	I/O	1	LV-CMOS data I/O. I/O direction controlled by M/S pin. M/S=1: Input M/S=0: Output Functional operation: R/W=1: Read R/W=0: Write
STRB0(WCLK0)	I/O	1	LV-CMOS data I/O. Function controlled by M/S pin. M/S=1: STRB0 Input M/S=0: WCLK0 Output
STRB1(WCLK1)	I/O	1	LV-CMOS Data I/O. Function controlled by M/S pin. M/S=1: STRB1 Input M/S=0: WCLK1 Output

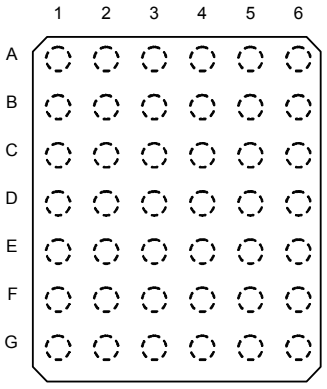
Serial I/O Signals Normal Functionality			
CKS+(DS+) CKS-(DS-)	Diff Serial I/O	2	Bi-directional serial I/O CKS+/CKS- when M/S=1 DS+/DS- when M/S=0
DS+(CKS+) DS-(CKS-)	Diff Serial I/O	2	Bi-directional serial I/O DS+/DS- when M/S=1 CKS+/CKS- when M/S=0
Supply Signals			
VDDP	Supply	1	Power supply for parallel I/O and internal circuitry.
VDDS	Supply	1	Power supply for serial I/O.
VDDA	Supply	1	Power supply for internal bit clock generator.
GND	Supply	2	Ground Pins: BGA - C1, D2, E3; MLP - center pad, 12

Notes:

1. () Indicate the operation of the pin when operating as a slave device. {} Indicate SPI Mode functionality. ({}) Slave Mode and SPI mode functionality except as noted.
2. Serial I/O signals are swapped on the slave so system traces do not have to cross between master and slave.

Pin Assignments

42 FBGA Package
3.5mm x 4.5mm
(.5mm Pitch)
(Top View)



Pin Assignments

	1	2	3	4	5	6
A	R/W	{SDAT} CNTL[4]	CNTL[2]	STRB0 (WCLK0)	DP[17]	DP[16]
B	CKSEL (H)	{SCLK} CNTL[5]	CNTL[3]	STRB1 (WCLK1)	DP[15]	DP[14]
C	GND	VDDP	CNTL[1]	CNTL[0]	DP[13]	DP[12]
D	CKS+ (DS+)	GND	M/S	DP[11]	DP[9]	DP[10]
E	CKS- (DS-)	VDDS	GND	DP[2]	DP[7] ({SDAT})	DP[8]
F	DS- (CKS-)	VDDA	PAR/SPI	DP[0]	DP[4]	DP[6] ({SCLK})
G	DS+ (CKS+)	/RES	/STBY (SLEW)	DP[1]	DP[3]	DP[5]

Figure 2. BGA Pin Assignments

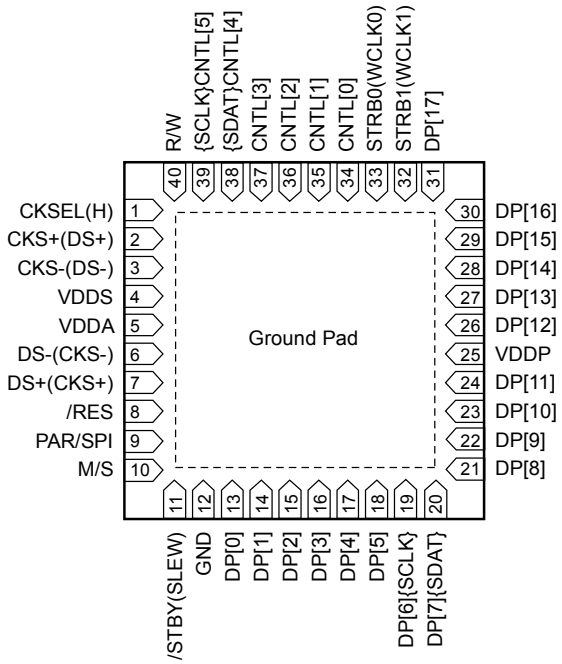


Figure 3. MLP Pin Assignments (40 Pins, 6x6mm, .5mm Pitch, Top View)

System Control Pins

(M/S) Master / Slave Selection: A given device can be configured as a master or slave device based on the state of the M/S pin.

Table 1. Master/Slave

M/S	Configuration
0	Slave Mode
1	Master Mode

(PAR/SPI) SPI Mode Selection: The PAR/SPI signal configures STRB0(WCLK0) for SPI mode write operation. STRB1(WCLK1) always operates in parallel mode. Control signals CNTL[5:0] all pass in SPI mode. In SPI mode, the SCLK signal is used to strobe the serializer. SPI mode supports SPI writes only.

Table 2. Channel 0 PAR/SPI Configuration

PAR /SPI	M/S=1 MASTER	M/S=0 SLAVE
0	SDAT=CNTL[4] SCLK=CNTL[5] /CS=STRB0	SDAT=DP[7] & CNTL[4] SCLK=DP[6] & CNTL[5] /CS=WCLK0
1	Parallel Mode	Parallel Mode

(CKSEL) Strobe Selection Signal: The CKSEL signal exists only on the master device and determines which strobe signal is active. The active strobe signal is selected by CKSEL and PAR/SPI inputs.

Table 3. PAR/SPI

PAR /SPI	CKSEL	Master Strobe Source	Slave Strobe Source
0	0	CNTL[5]	DP[6] & CNTL[5]
0	1	STRB1	WCLK1
1	0	STRB0	WCLK0
1	1	STRB1	WCLK1

(/RES, /STBY) Reset and Standby Mode Functionality: Reset and standby mode functionality is determined by the state of the /RES and /STBY signals for the master device and the /RES and internal standby-detect signal for the slave device. The /RES control signal has a filter that rejects spurious pulses on /RES.

Table 4. Reset and Standby Modes

/RES	/STBY(3)	Master	Slave
0	X	Reset Mode	Reset Mode
1	0	Standby Mode	Standby Mode(3)
1	1	Operating Mode	Operating Mode

Note:

3. The slave device is put into standby mode through control signals sent from the master device.

Table 5. Reset and Standby Mode States

Pin	Master Reset / Standby	Slave Reset	Slave Standby
DP[17:0]	Disabled	Low	Last data
CNTL[5:0]	Disabled	Low	Last data
STRB[0:1] (WCLK[0:1])	Disabled	High	High

(SLEW) Slew Control: The slew control operates only when in slave mode. This signal changes the edge rate of the DP[17:0], CNTL[5:0], R/W, WCLK1, and WCLK0 signals to optimize edge rate for the load being driven. Master read mode outputs have “slow” edge rates.

Table 6. Slew Rate Control

/STBY (SLEW)	Slave M/S=0
0	“Slow”
1	“Fast”

LV-CMOS I/O Signals

System Control Signals

The system control signals consist of M/S, /RES, /STBY(SLEW), PAR/SPI, and CKSEL. For connectivity flexibility, these signals are over-voltage tolerant to the maximum supply voltage connected to the device. This allows these signals to be tied HIGH to either a V_{DDS} or V_{DDP} supply without static current consumption. These signals are all LV-CMOS inputs and should never be allowed to float.

Parallel I/O Signals

The parallel data port signals consist of the DP[17:0], CNTL[5:0], R/W, and STRB1(0)(WCLK1(0)) signals. These signals have built-in voltage translation, allowing the signals of the master and slave to be connected to different V_{DDP} supply voltages.

Serial I/O Signals

CTL I/O Technology

The serial I/O is implemented using Fairchild's proprietary differential CTL I/O technology. During data transfers, the serial I/O are powered up to a normal operating mode around .5V. Upon completion of a data transfer, the serial I/O goes to a lower power mode around V_{DDS}.

Serial I/O Orientation Logic

The serial I/O signal traces should not cross between the master and the slave. The pin locations have been designed to eliminate the need to cross traces. See Table 7, Figure 4 and Figure 5.

Table 7. Serial Pin Orientation

	Master (M/S=1) (Pad/Pin #)				Slave (M/S=0) (Pad/Pin #)			
Package	CKS+	CKS-	DS-	DS+	CKS+	CKS-	DS-	DS+
MLP	2	3	6	7	7	6	3	2
BGA	D1	E1	F1	G1	G1	F1	E1	D1

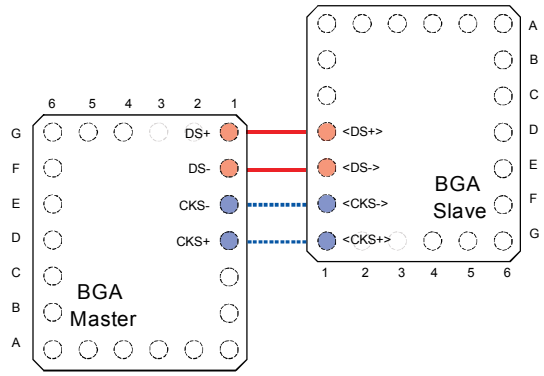


Figure 4. BGA Pair

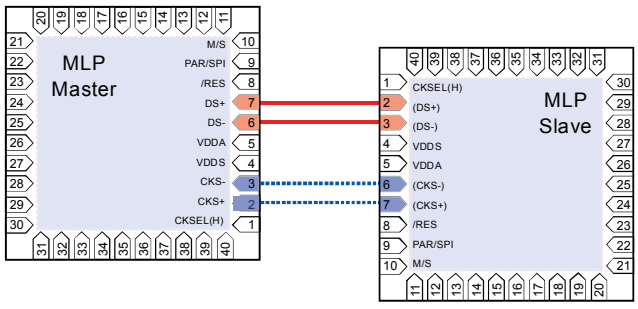


Figure 5. MLP Pair

Master/Slave READ/WRITE transactions

During a write data transfer, DP[17:0], CNTL[5:0], R/W, and CKSEL are serialized and transmitted by the master to the slave. The slave receives the signals, outputs the data and control signals, and generates either a WCLK0 or WCLK1 pulse based on the value of CKSEL. The CKSEL signal must remain stable throughout the transaction.

Read transactions have two phases: The Read-Control Phase, where CNTL[5:0], R/W, CKSEL are transmitted to the deserializer; and the Read-Data Phase, where the DP[17:0] signals of the slave are read and transmitted back to the master device. The slave device generates its own strobe signal for latching in the data. Slave data must be valid prior to the WCLKn signal going HIGH.

Master Serializer Operation (Read Control Phase)
When the R/W signal is asserted HIGH and the STROBE signal transitions LOW, the Read-Control Phase of the read cycle is initiated. The R/W signal must not transition until the READ cycle completes. For a READ transaction, only eight control signals are captured. The 18 DP bits are ignored during the READ operation. The following sequence must occur for data to be serialized properly:

Microcontroller Read Sequence (Read-Control Phase):
1. Selects input strobe source (CKSEL= 0 or 1).
2. CPU sends signals (R/W=1, CKSEL, CNTL[5:0]).
3. STROBE Signal transitions LOW.
4. Captures control bits.
5. Device leaves burst standby mode.
6. Serializes and sends control bits.
7. Serializer turns around serial I/O waiting for data.

Slave Deserializer Operation (Read-Control Phase)
Microcontroller Read Sequence (Read-Control Phase):
1. Deserializer leaves burst standby mode.
2. Begins receiving valid serial stream.
3. Captures data from serial transfer.
4. Turns around serial I/O.
5. Internally decodes that this is a READ transaction and the WCLK to use.
6. Outputs control signals, 3-state DP data bus.
7. Outputs falling edge of WCLK pulse.

Slave Serializer Read Operation (Read-Data Phase)
The slave serializer is enabled on the tail end of the Read-Control Phase of operation. The operation of the serializer is identical to the master serialization except that the strobe signal is generated internally and only the data bits DP[17:0] are captured.

Microcontroller Read Sequence (Read-Data Phase):
1. Display device outputs data onto DP bus on falling edge of WCLK.
2. Captures parallel data on generated rising edge of WCLK signal.
3. Serializes data stream.
4. DP signals are sent.
5. CNTL signals are sent as 0.
6. Turns serial I/O around, awaiting next transaction.

Master Deserializer Read Operation (Read-Data Phase):
Initially the deserializer is in low-power operation. The deserializer wakes up when it detects CKSO+ and CKSO- transition from LOW to normal operating range.

Microcontroller Read Sequence (Read-Data Phase):
1. Master deserializer wakes up when the CKSI+ and CKSI- signals reach valid levels.
2. Begins receiving valid serial stream.
3. Outputs data DP[17:0].
4. Turns serial I/O around and goes to burst standby mode.
5. Processor asserts rising edge of strobe signal to capture data.

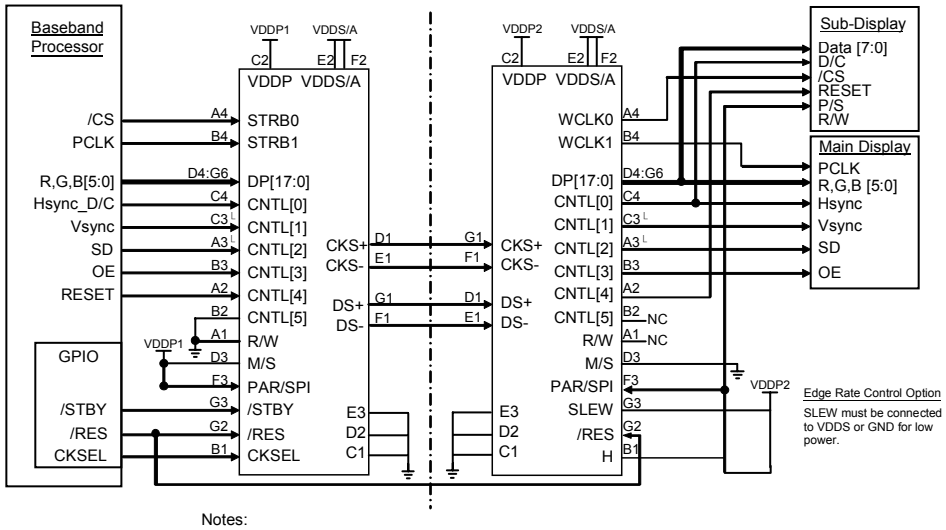
SPI WRITE transaction

SPI mode is activated by asserting the PAR/SPI signal low on both the master and slave device. A SPI write is only performed when CKSEL=0. During a SPI transaction, SCLK must be connected to CNTL[5] and is the strobe source for serialization. SDAT is assumed to be on CNTL[4] and all of the remaining control signals and STRB0 are serialized. STRB0 should be connected to the SPI mode chip select.

On the rising edge of SCLK, all eight control signals (CNTL[5:0], R/W, CKSEL) are captured and serialized. The data signals are not sent. The /CS signal on STRB0 is captured in bit position CNTL[5]. The deserializer captures the serial stream and outputs it to the parallel port.

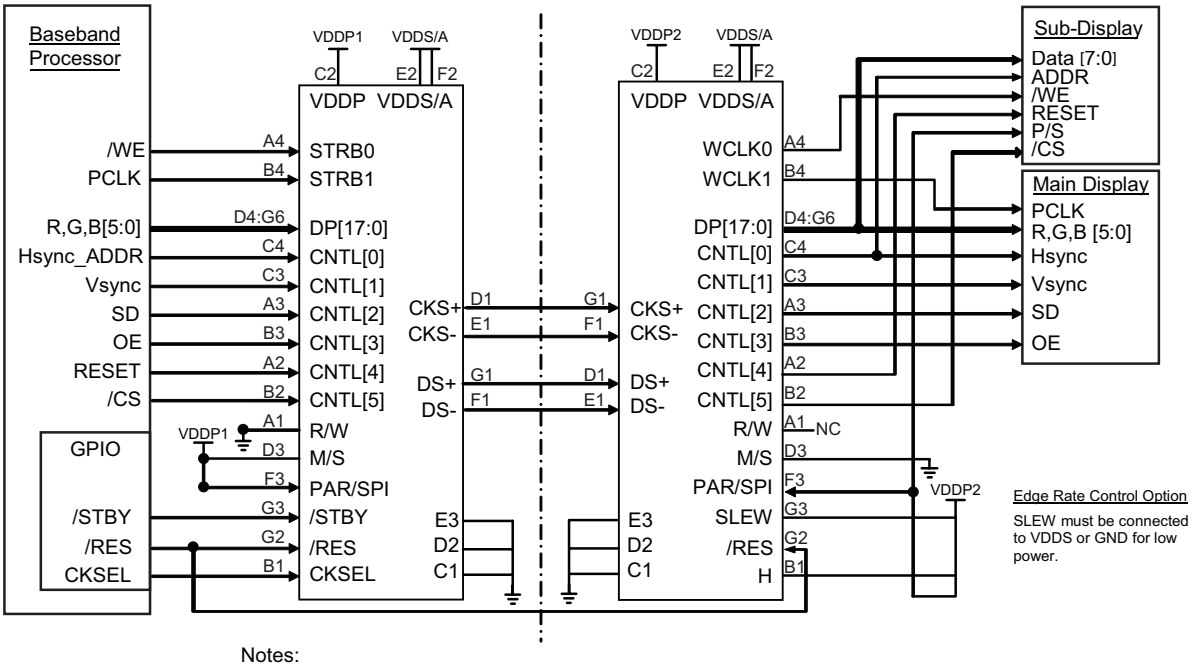
As shown in Table 2, SDAT and SCLK are output on multiple pins. The DP[7] and DP[6] connections can be used for displays with dual-mode operation and the data pins are multiplexed with the SPI signals. CNTL[5] and CNTL[4] signals can be used when the signals are not multiplexed.

Application Diagrams



Notes:
1. Write-only Interface.
2. Assumes BGA die on display.
3. /CS used to strobe sub-display data.
4. PCLK used for RGB mode.
5. Pin numbers for BGA package.

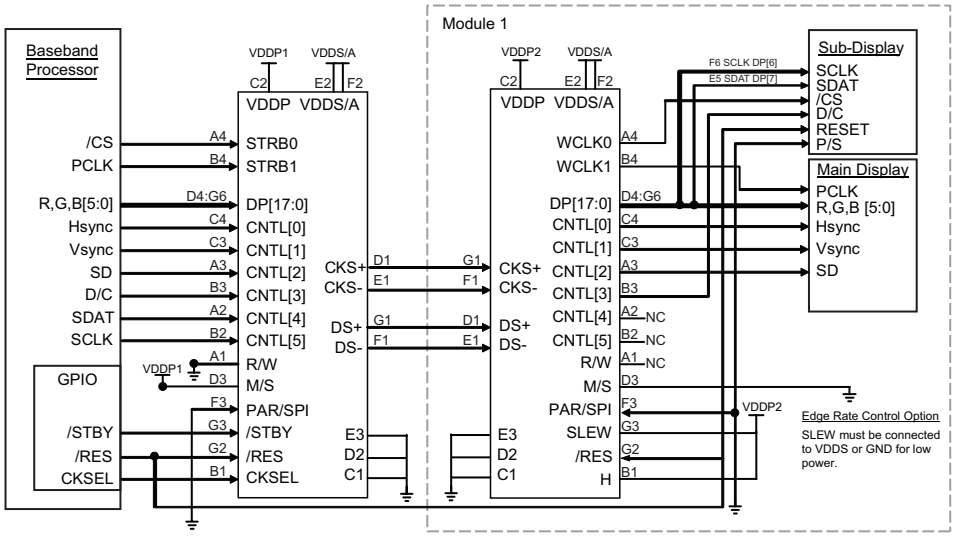
Figure 6. Dual Display with Parallel RGB Main Display and 6800-Style Microcontroller Sub-Display



Notes:
1. Write-only Interface.
2. Assumes BGA die on display.
3. /WE used to strobe sub-display data.
4. PCLK used for RGB mode.
5. Pin numbers for BGA package.

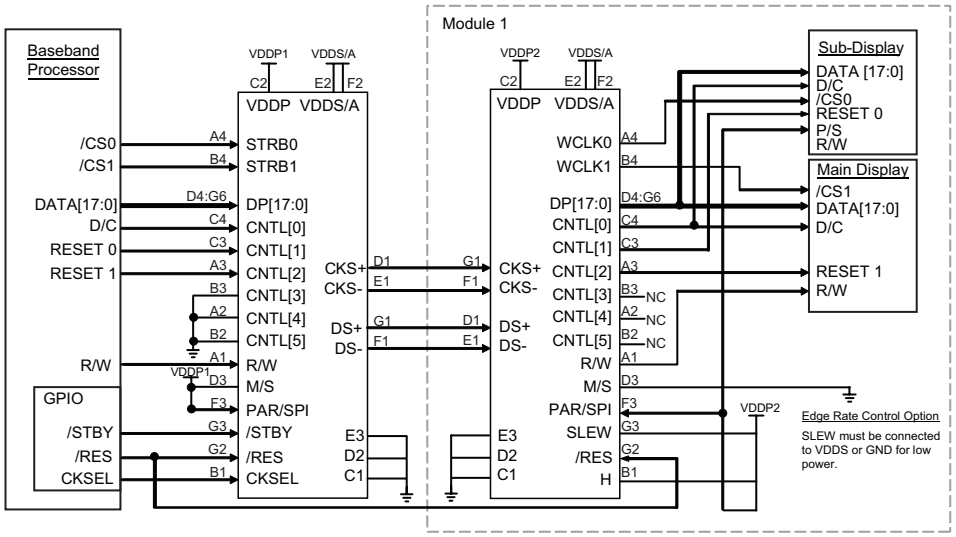
Figure 7. Dual Display with Parallel RGB Main Display and x86-Style Microcontroller Sub-Display

Application Diagrams (Continued)



Notes:
1. Write-only interface (R/W hardwaired LOW).
2. SPI sub-display interface PAR/SPI=LOW for both master and slave.
3. SCLK connected to CNTL[5]; SDAT connected to CNTL[4].
4. Shared data pin SDAT; SCLK connections on sub-display.
5. Assumes BGA die on display.
6. Pin numbers for BGA package.

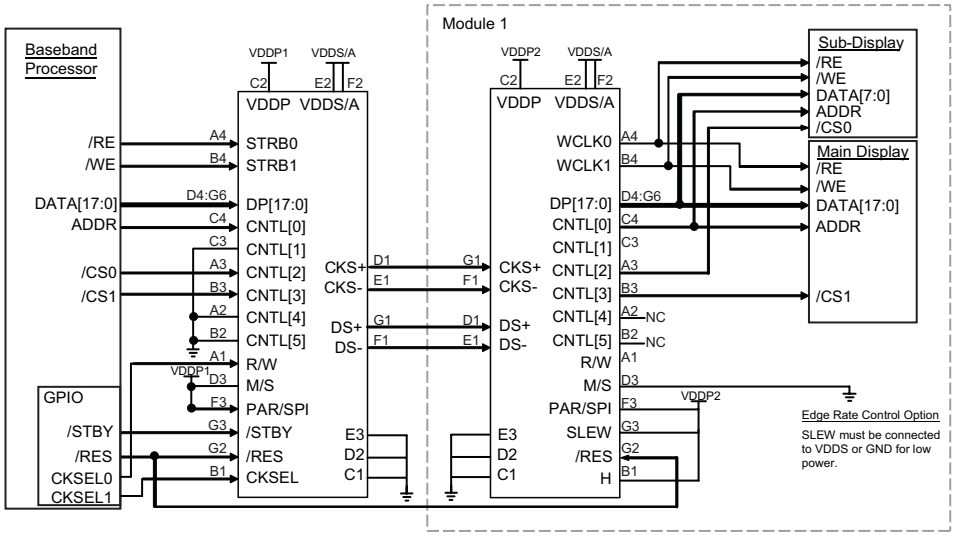
Figure 8. Dual Display with RGB Main Display and SPI Sub-Display Interface



Notes:
1. R/W interface. R/W signal connected to baseband microprocessor.
2. Assumes BGA die on display.
3. PAR/SPI connected HIGH to indicate parallel operation.
4. Pin numbers for BGA package.

Figure 9. R/W Dual Display with Parallel Microcontroller Main Display and Sub-Display

Application Diagrams (Continued)



Notes:
1. Dual display R/W Intel® interface.
2. Assumes BGA die on display.
3. GPIO signal used to select READ or WRITE functionality. Connected to CKSEL and R/W.
4. Displays selected via the chip selects.
5. Pin numbers for BGA package.

Figure 10. Dual R/W x86-Style Microcontroller Display Interface

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential Serial Wires the same length.
- Do not allow noisy signals over or near differential serial wires.
  Example: No LVCMOS traces over differential serial wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Design goal of 100-ohms differential characteristic impedance.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.
- For additional applications notes or flex guidelines see your sales rep or contact Fairchild directly.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	+3.6	V
	All Input/Output Voltage	-0.5	V_{DDP}+0.5	V
T_{STG}	Storage Temperature Range	-65	150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (soldering, 4 seconds)		+260	°C
ESD	IEC 61000 Board Level		15	kV
	HBM, 1.5kΩ, 100pF		8.5	kV
	HBM, 1.5kΩ, 100pF, Serial I/0 pins		14.5	kV
	MM, 0Ω, 200pF		400	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}[4]	Supply Voltage	2.5	3.0	V
V_{DDP}	Supply Voltage	1.6	$V_{DDA/S}$	V
T_A	Operating Temperature	-30	+70	°C

Note:

4. V_{DDA} and V_{DDS} supplies must be hardwired together to the same power supply. V_{DDP} must be less than or equal to V_{DDA}/V_{DDS}.

DC Electrical Characteristics – LV CMOS I/Os

Values are provided for over-supply voltage and operating temperature ranges unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IH}	Input High Voltage		0.7 x V_{DDP}	V_{DDP}	V
V_{IL}	Input Low Voltage		GND	0.3 x V_{DDP}	V
V_{OH}	Output High Voltage	SLEW=0 I_{OH} = -250µA	0.8 x V_{DDP}		V
		SLEW=1 I_{OH} = -1mA			
V_{OL}	Output High Voltage	SLEW=0 I_{OL} = 250µA		0.2 x V_{DDP}	V
		SLEW=1 I_{OL} = 1mA			
I_{IN}	Input Current		-5	5	µA

DC Serial I/O Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{ODH1}	Active Output HIGH Source Current	M/S=1, R/W=0,V_{OS}=0.7V		1.5		mA
I_{ODL1}	Active Output LOW Sink Current	M/S=1, R/W=0, V_{OS}=0.7V		0.8		mA
I_{ODSTBY}	Standby Burst Output HIGH Source Current	M/S=1, R/W=0, V_{OS}=1.0V		130		µA
V_{STBY}	Output Voltage in Standby or Reset	M/S=1, /RST=1, /STBY=0 I_{OH}=-100µA		V_{DDS}		V
V_{GO}	Input Voltage Ground Offset	Relative to Driver		0		V
R_{TERM}	Termination Resistor	M/S=0, /RST=0 Internal R_{TERM} CKS+(DS+)=0.9V CKS-(DS-)=0.8V	125	150	175	Ω

Note:

5. Actual application cable is terminated with 150Ω on both sides.

Power Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
I_{DYN_SER}	Dynamic Current of Master Device	$V_{DDA/S}$=2.75V, M/S=1, V_{DDP}=1.8V, /STBY=1, /RES=1	5.44MHz		4		mA
			12.00MHz		7		
			15.00MHz		8		
I_{DYN_DES}	Dynamic Current of Slave Device	$V_{DDA/S}$=2.75V, M/S=0 V_{DDP}=1.8V, /STBY=1, /RES=1, C_L= 0pF	5.44MHz		5		mA
			12.00MHz		8		
			15.00MHz		10		
I_{BRST_M}	Burst Standby Current of Master	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, M/S=1, /STBY=1, /RST=1, No STROBE Signal, C_L=0pF			1.1		mA
I_{BRST_S}	Burst Standby Current of Slave	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, M/S=0, /STBY=1, /RST=1, No STROBE Signal, C_L=0pF			1.8		mA
I_{STBY}	Standby Current	Serializer or Deserializer $V_{DDS/A}$=V_{DDP}=3.0V, /STBY=0, /RST=1, STRB1=5.44MHz, C_L=0pF				10	µA

AC Operating Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{WSTRB0}	Write Strobe Frequency	CKSEL=0 STRB0 (PRS1)	0		8	MHz
f_{WSTRB1}	Write Strobe Frequency	CKSEL=1 STRB1	0		15	MHz
f_{RSTRB}	Read Strobe Frequency		0		2	MHz
t_R, t_F	Input Edge Rates[6]				40	ns
t_{S1}	Write Mode Setup Time	DP before STRBn ↑, See Figure 11	5			ns
t_{H1}	Write Mode Hold Time	DP after STRBn ↑, See Figure 11	15			ns
t_{S2}	READ Mode Setup Time	R/W, CNTL before STRBn ↓ See Figure 12	0			ns
t_{H2}	READ Mode Hold Time	R/W, CNTL after STRBn ↓ See Figure 12	16			ns
t_{S-STRB}	CKSEL to STRBn Setup Time	CKSEL before active edge STRBn[7] See Figure 13, Figure 14	50			ns
t_{SKEW_DS-CKS}	Allowed DS-CKS Input Signal Skew	Deserializer Mode Max. Internal Oscillator Frequency See Figure 18	-150	0	150	ps

Notes:

6. Characterized, but not production tested.
7. Active edge of strobe is the rising edge for a write transaction and the falling edge for a read transaction.

AC Deserializer Specifications

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{R0}, t_{F0}	Output Edge Rates of WCLK0,WCLK1	SLEW=0, CL=5pF 20% to 80%[8]	8		17	ns
		SLEW=0; C_L=10pF 30% to 70%[8]			12	
		SLEW=1, C_L=5pF 20% to 80%[8]			10	
t_{R1}, t_{F1}	Output Edge Rates of R/W, DP[17:0] CNTL[5:0]	SLEW=0, C_L=5pF 20% to 80%[8]	8		22	ns
		SLEW=0; C_L=10pF 30% to 70%[8]			12	
		SLEW=1, C_L=5pF 20% to 80%[8]			17	
t_{CS}	CNTL[5:0],R/W to Falling Edge of WCLKn	M/S=0[9], See Figure 15	0	4		ns
$t_{PDV-WR0}$	DP, CNTL to WCLK0 ↑	PAR/SPI=1[9], See Figure 15	50	60		ns
$t_{PDV-WR1}$	DP, CNTL to WCLK1 ↑	PAR/SPI=1[9], See Figure 15	18	24		ns
t_{PDV-RD}	CNTL to WCLKn ↑	PAR/SPI=1[9], See Figure 17	200	224		ns
$t_{PDV-SPI}$	Data, CNTL to SCLK ↑	PAR/SPI=0[9], See Figure 16	40	60		ns
$t_{PWL-WR0}$	WCLK0 Pulse Width Low Write Mode	M/S=0, R/W=0, PAR/SPI=1[9,10] See Figure 15	50	56		ns
$t_{PWL-WR1}$	WCLK1 Pulse Width Low Write Mode	M/S=0, R/W=0, PAR/SPI=1[9,10] See Figure 15	18	20		ns
t_{PWL-RD}	Pulse Width Low of WCLK Read Mode	M/S=0, R/W=1, PAR/SPI=1[9,10] See Figure 17	200	220		ns
$t_{PWL-SPI}$	Pulse Width Low of WCLK SPI Mode	M/S=0, R/W=0, PAR/SPI=0[9, 10] See Figure 16	40	56		ns

Notes:

8. Characterized, but not production tested.
9. Indirectly tested through serial clock frequency and serial data bit tests.
10. Pulse width low WCLKn measurements are measured at 30% of VDDP. Measurements apply when SLEW=0 or SLEW=1.

AC Data Latencies

Symbol	Parameter	Test Conditions	Typ.[13]	Max.	Units
t_{PD-WR0}	Write Latency	WRITE Mode, CKSEL=0[11,12] See Figure 15	147		ns
t_{PD-WR1}	Write Latency	WRITE Mode, CKSEL=1[11,12] See Figure 15	111		ns
t_{PD-RD}	Total Read Latency	READ Mode[11,14] See Figure 17	340	480	ns
t_{PD-RDC}	Read Control Latency	READ Mode[11,15] See Figure 17	276		ns
t_{PD-RDD}	Read Data Latency	READ Mode[11,16] See Figure 17	84		ns
t_{PD-SPI}	SPI Write Latency	SPI-WRITE Mode[11,17] See Figure 16	115		ns

Notes:

11. Minimum times occur with maximum oscillator frequency. Maximum times occur with minimum oscillator frequency.
12. Write latency is the sum of the delay through the master serializer and slave deserializer, plus the flight time across the flex cable and I/O propagation delays.
13. Assumes propagation delay across the flex cable and through the I/Os of 20ns.
14. Total read latency t_{PD-RD} is the sum of the Read-Control Phase latency (t_{PD-RDC}) and the Read-Data Phase latency (t_{PD-RDD}). $t_{PD-RD} = t_{PD-RDC} + t_{PD-RDD}$.
15. Read-Control latency is the sum of the delay through the master serializer and slave deserializer, plus flex cable flight times and I/O propagation delays.
16. Read Data latency is the sum of the delay through the slave serializer and master deserializer, plus flex cable flight times and I/O propagation delays.
17. SPI–Write latency is the sum of the delay through the master serializer and slave deserializer, plus the flight time across the flex cable and I/O propagation delays.

AC Oscillator Specifications

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{OSC}	Serial Operating Frequency		240	275	310	MHz
$t_{OSC-STBY}$	Oscillator Stabilization Time After Standby	$V_{DDA}=V_{DDS}=2.75V$ /RES=1, /STBY ↑ Transition		15	30	µs
$t_{OSC-RES}$	Oscillator Stabilization Time After Reset	$V_{DDA}=V_{DDS}=2.75V$ /STBY=1, /RES ↑ Transition		30	50	µs

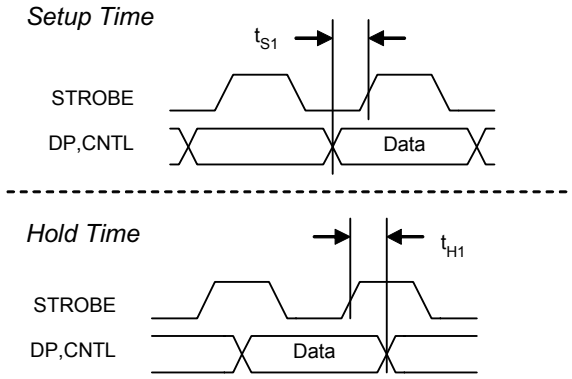
AC Reset and Standby Timing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{VDD-OFF}$	Power Down Relative to /RES[18]	See Figure 20	20			µs
$t_{STRB-RES}$	/RES after last STRBn ↑	M/S=0 or 1, /STBY=1, R/W=0[19] See Figure 20	0			ns
$t_{STRB-STBY}$	Standby time after last strobe	M/S=0 or 1, /STBY=1[20] See Figure 20	200			ns
$t_{RES-OFF}$	Master/Slave Reset Disable Time	M/S=1 /STBY=1, /RES=↓ See Figure 20		15	20	µs
$t_{VDD-SKEW}$	Allowed Skew between V_{DDP} and $V_{DDA/S}$[21]	Figure 19	-∞		+∞	ms
$t_{VDD-RES}$	Minimum Reset Low Time After V_{DD} Stable	M/S=0 /STBY=1, /RES=↑[22] See Figure 19	20			µs
$t_{RES-STBY}$	/STBY Wait Time After /RES ↑	M/S=1 /RES=1, /STBY=↓ See Figure 19	20			µs
t_{DVALID}	/STBY to Active Edge of Strobe	M/S=0 /RES=1[23] See Figure 19	30			µs

Notes:

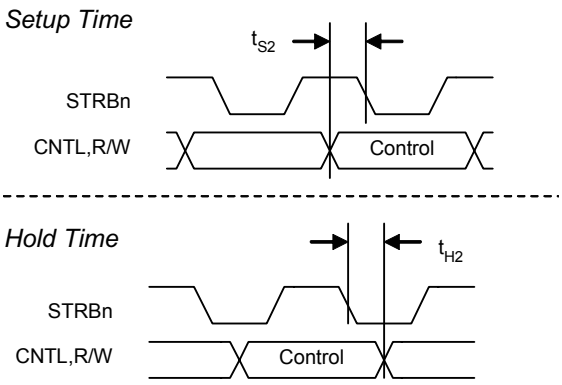
18. Timing allows the device to completely reset prior to powering down.
19. Internal reset on the filter allows assertion prior to completion of read or write date transfer.
20. Timing ensures that last write transaction is complete prior to going into standby.
21. $V_{DDA/S}$ must power up together. V_{DDP} may power-up relative to $V_{DDA/S}$ in any order without static power being consumed. Guaranteed by characterization.
22. /RES signal should be held low for minimum time specified after supplies go HIGH. It is recommended that /RES be held low during the power supply ramp.
23. STRBn must be held off until internal oscillator has stabilized.

Typical Performance Characteristics



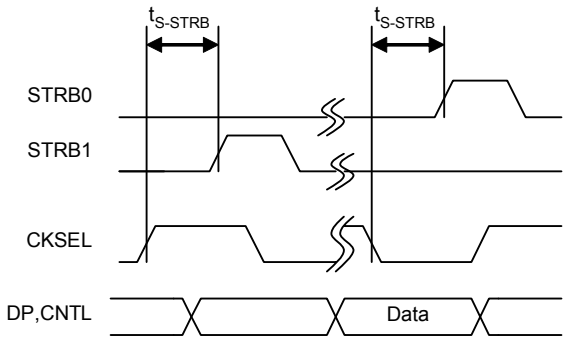
Setup: CKSEL=0 or 1, R/W=0

Figure 11. Master Write Setup and Hold Time



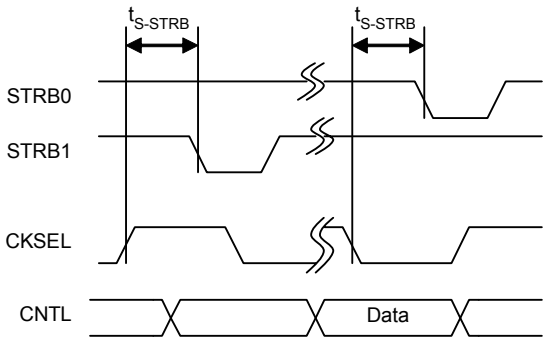
Setup: CKSEL=0 or 1, R/W=1

Figure 12. Master Read Setup and Hold Time



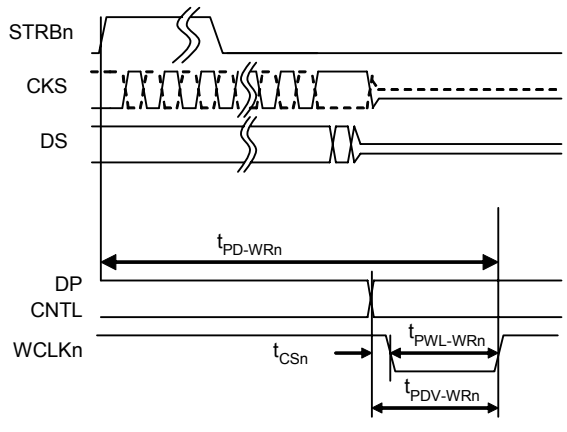
Setup: CKSEL=0 or 1, R/W=0

Figure 13. CKSEL Write Setup Time



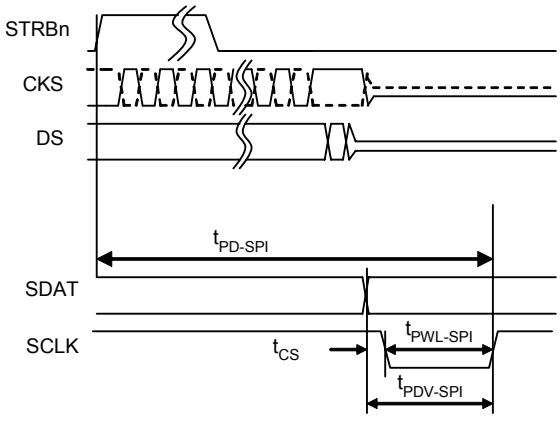
Setup: CKSEL=0 or 1, R/W=1

Figure 14. CKSEL Read Setup Time



Setup: CKSEL=0 or 1, R/W=0, PAR/SPI=1

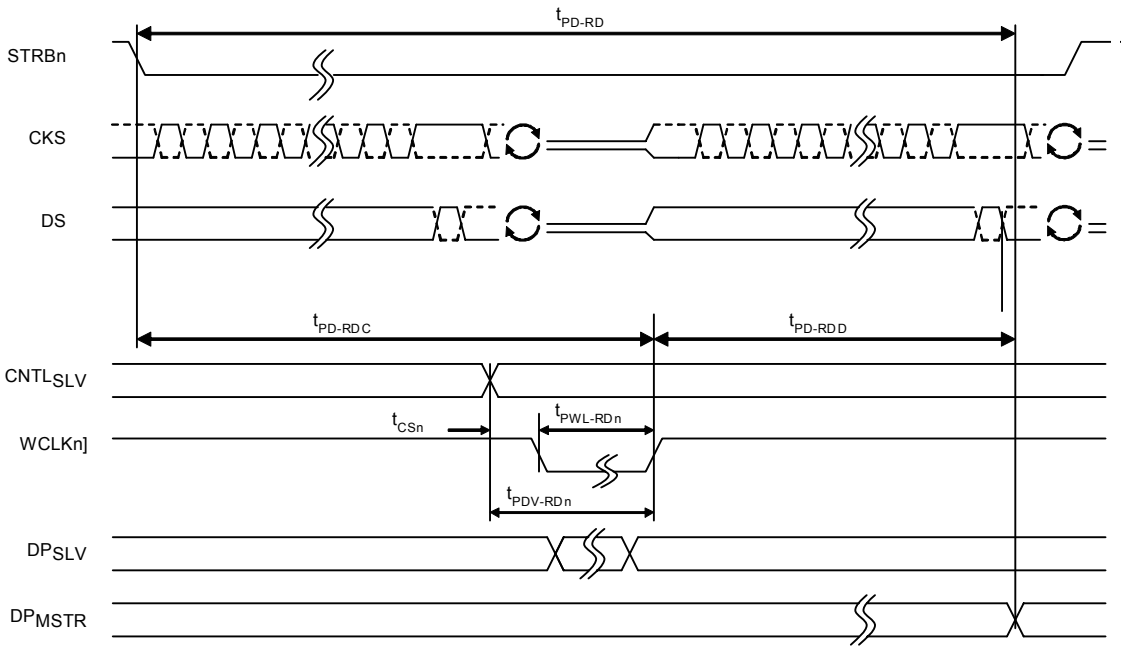
Figure 15. Slave Write Mode Timing



Setup: CKSEL=0, R/W=0, PAR/SPI=0

Figure 16. Slave SPI Mode Timing

Typical Performance Characteristics (Continued)



Setup: CKSEL=0 or 1, R/W=1, PAR/SPI=1

Figure 17. Slave Read Mode Timing

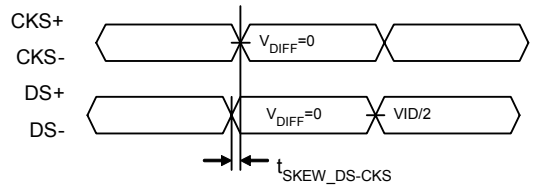


Figure 18. Allowed Differential Input Signal Skew

Typical Performance Characteristics (Continued)

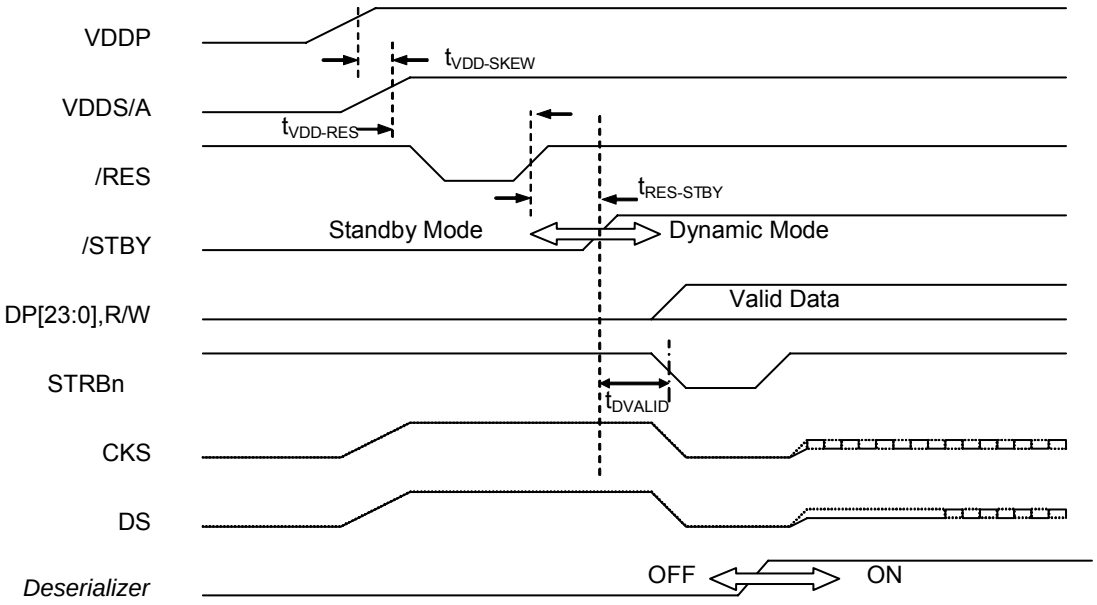


Figure 19. Power-Up Timing

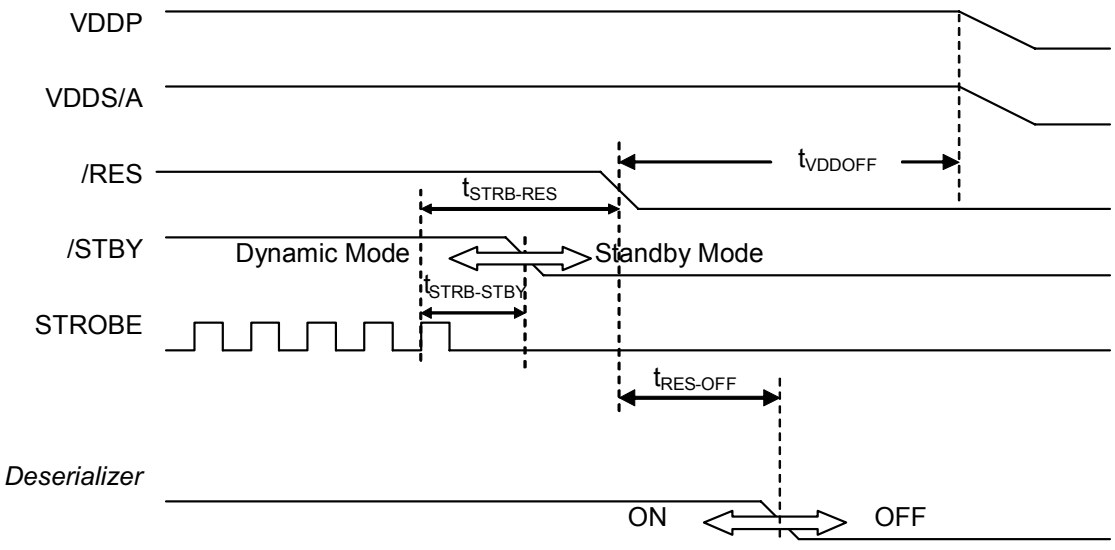
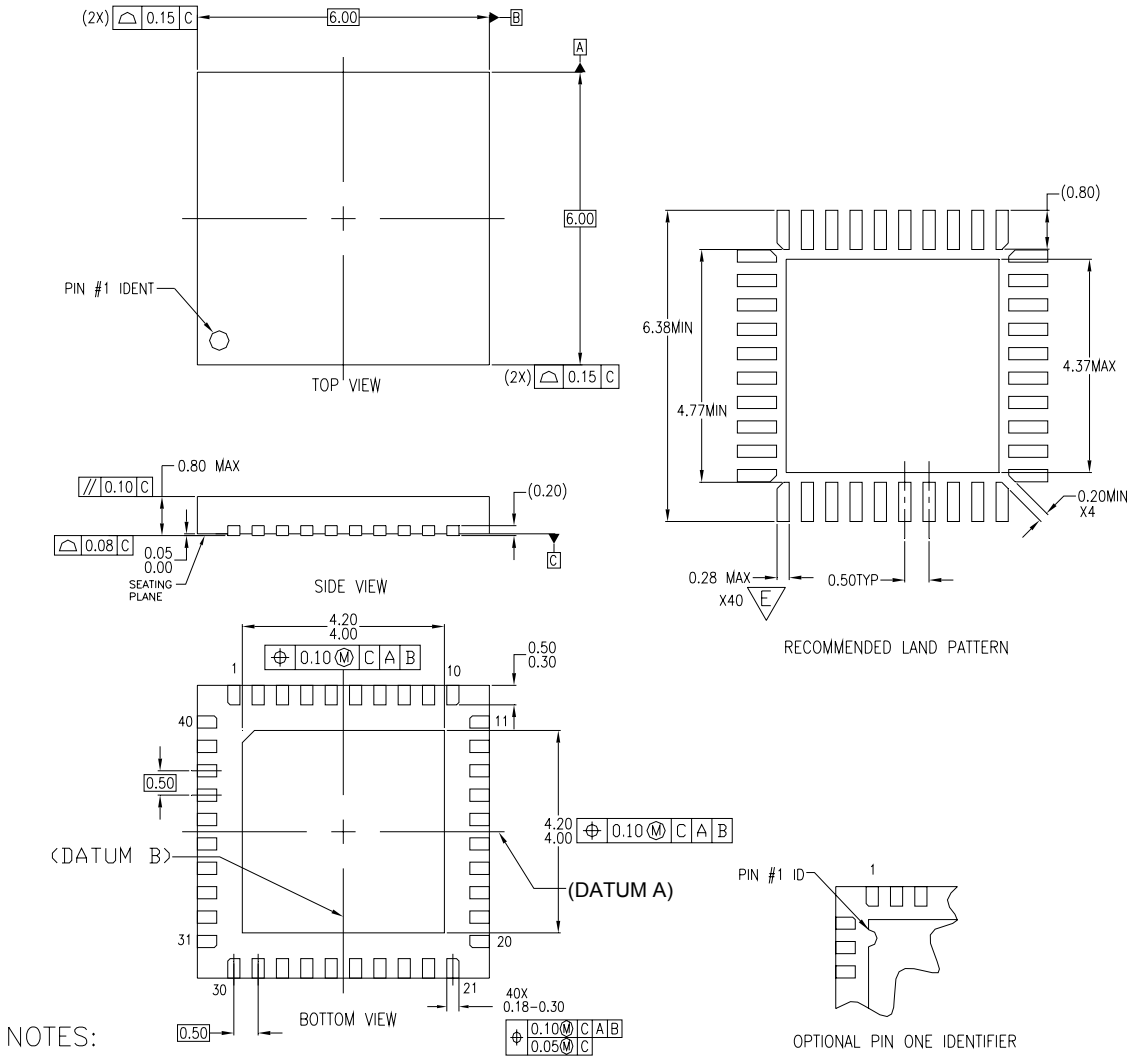


Figure 20. Power-Down Timing

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THIS IS A SAWN VERSION.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

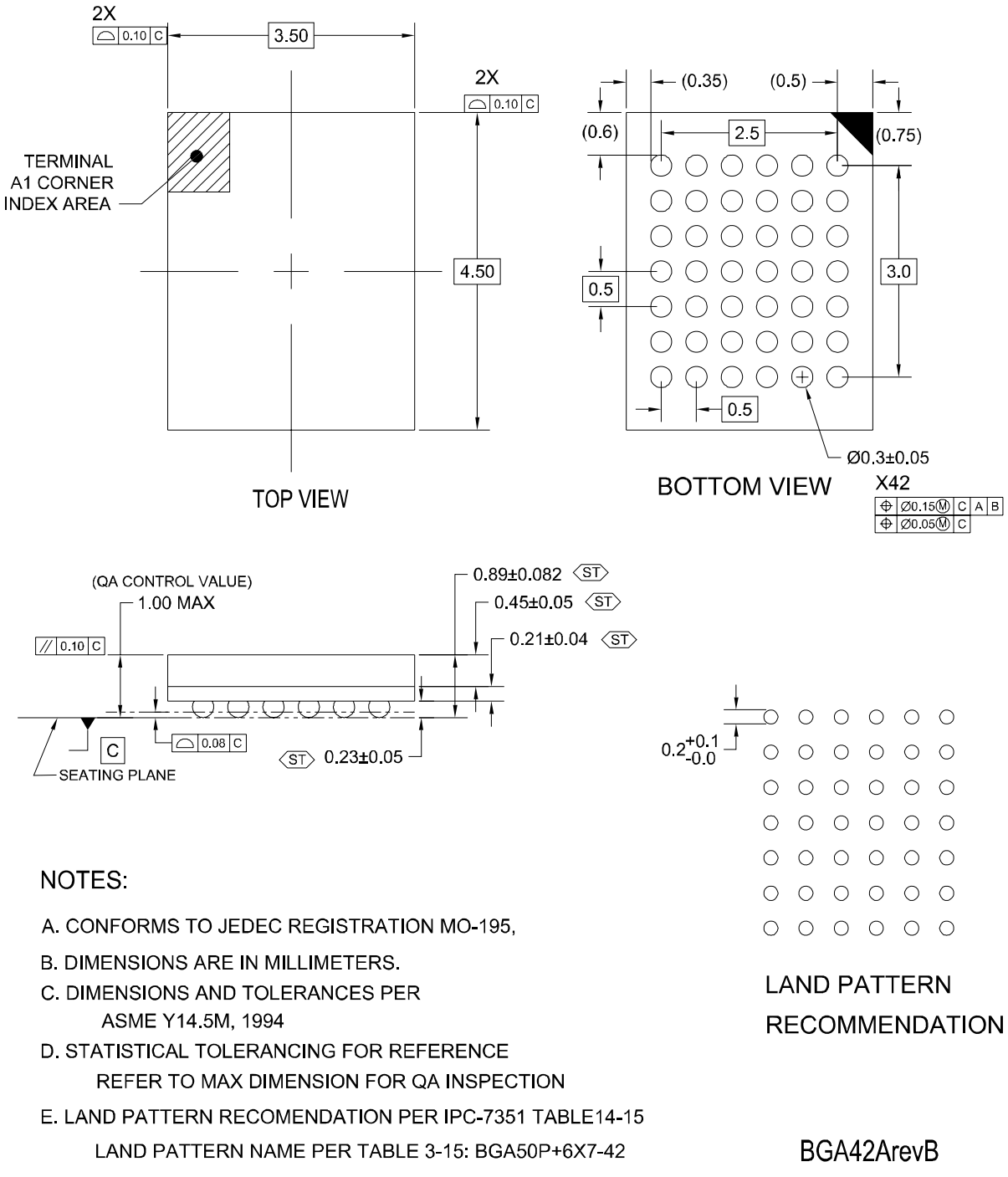
G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP40Arev2

Figure 21. 40-Lead, Molded Leadless Package (MLP)

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE
REFER TO MAX DIMENSION FOR QA INSPECTION

E. LAND PATTERN RECOMENDATION PER IPC-7351 TABLE14-15
LAND PATTERN NAME PER TABLE 3-15: BGA50P+6X7-42

BGA42ArevB

Figure 22. 42-Ball, Ball Grid Array (BGA) Package

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3

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Rev. I24