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FMS3818

Triple Video D/A Converters

3 x 8 bit, 180 Ms/s

Features

- ±2.5% gain matching
- ±0.5 LSB linearity error
- Internal bandgap voltage reference
- Low glitch energy
- Single 3.3 Volt power supply

Applications

- PC Graphics
- Video signal conversion
  - RGB
  - YC_BC_R
  - Composite, Y, C

Description

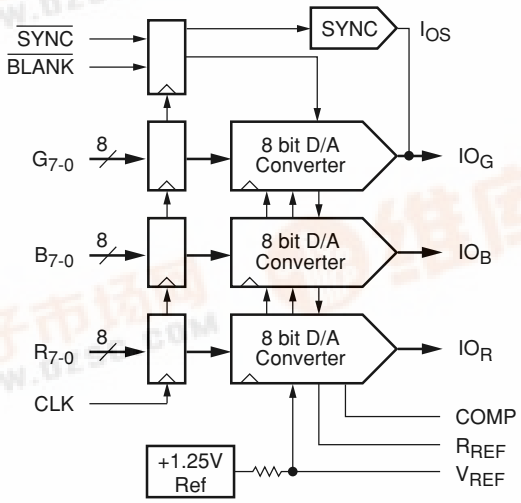
The FMS3818 is a low-cost triple D/A converter, tailored to fit graphics and video applications where speed is critical.

CMOS-level inputs are converted to analog current outputs that can drive 25–37.5Ω loads corresponding to doubly-terminated 50–75Ω loads. A sync current following $\overline{SYNC}$ input timing is added to the I_{OG} output. $\overline{BLANK}$ will override RGB inputs, setting I_{OG}, I_{OB} and I_{OR} currents to zero when $\overline{BLANK}$ = L. Although appropriate for many applications the internal 1.25V reference voltage can be overridden by the V_{REF} input.

Few external components are required, just the current reference resistor, current output load resistors, bypass capacitors and decoupling capacitors.

Package is a 48-lead LQFP. Fabrication technology is CMOS. Performance is guaranteed from 0 to 70°C.

Block Diagram



Functional Description

Within the FMS3818 are three identical 8-bit D/A converters, each with a current source output. External loads are required to convert these currents to voltage outputs. Data inputs RGB_{7-0} are overridden by the $\overline{BLANK}$ input. $\overline{SYNC}$ = H activates sync current from I_{OS} for sync-on-green video signals.

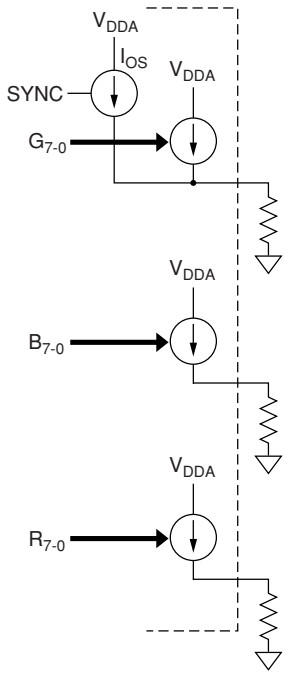


Figure 1. FMS3818 Current Source Structure

Digital Inputs

Incoming GBR data is registered on the rising edge of the clock input, CLK. Analog outputs follow the rising edge of CLK after a delay, t_{DO}.

$\overline{SYNC}$ and $\overline{BLANK}$

$\overline{SYNC}$ and $\overline{BLANK}$ inputs control the output level (Figure 1 and Table 1) of the D/A converters during CRT retrace intervals. $\overline{BLANK}$ forces the D/A outputs to the blanking level while $\overline{SYNC}$ = L turns off a current source, I_{OS} that is connected to the green D/A converter. $\overline{SYNC}$ = H adds a 112/256 fraction of full-scale current to the green output. $\overline{SYNC}$ = L extinguishes the sync current during the sync tip.

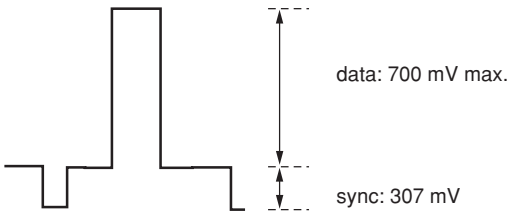


Figure 2. Nominal Output Levels

$\overline{BLANK}$ gates the D/A inputs. If $\overline{BLANK}$ = H, the D/A inputs control the output currents to be added to the output blanking level. If $\overline{BLANK}$ = L, data inputs and the pedestal are disabled.

D/A Outputs

Each D/A output is a current source from the V_{DDA} supply. Expressed in current units, the GBR transformation from data to current is as follows:

$G = G_{7-0}$ & $\overline{BLANK}$ + $\overline{SYNC}$ * 112
$B = B_{7-0}$ & $\overline{BLANK}$
$R = R_{7-0}$ & $\overline{BLANK}$

Typical LSB current step is 73.2 µA.

To obtain a voltage output, a resistor must be connected to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

To implement a doubly-terminated 75Ω transmission line, a shunt 75Ω resistor should be placed adjacent to the analog output pin. With a terminated 75Ω line connected to the analog output, the load on the FMS3818 current source is 37.5Ω.

The FMS3818 may also be operated with a single 75 Ohm terminating resistor. To lower the output voltage swing to the desired range, the nominal value of the R_{REF} resistor should be doubled.

Voltage Reference

Full scale current is a multiple of the current I_{SET} through an external resistor, R_{SET} connected between the R_{REF} pin and GND. Voltage across R_{SET} is the reference voltage, V_{REF}, which can be derived from either the 1.25 volt internal bandgap reference or an external voltage reference connected to V_{REF}. To minimize noise, a 0.1µF capacitor should be connected between V_{REF} and ground.

I_{SET} is mirrored to each of the GBR output current sources. To minimize noise, a 0.1µF capacitor should be connected between the COMP pin and the analog supply voltage V_{DDA}.

Power and Ground

Required power is a single +3.3 Volt supply. To minimize power supply induced noise, analog +3.3V should be connected to V_{DDD} and V_{DDA} pins with 0.1 and 0.01 µF decoupling capacitors placed adjacent to each V_{DD} pin or pin pair.

High slew-rate digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

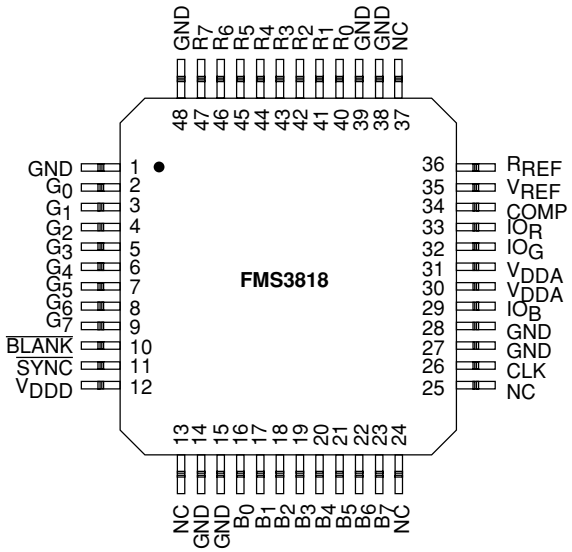
Table 1. Output Voltage Coding

V_{REF} = 1.25 V, R_{REF} = 348 Ω, R_L = 37.5 Ω

RGB7-0 (MSB…LSB)	$\overline{SYNC}$	$\overline{BLANK}$	V_{RED}, V_{BLUE} (mV)	V_{GREEN} (mV)
1111 1111	1	1	700	1,007
1111 1111	0	1	700	700
1111 1110	1	1	697	1,004
1111 1101	1	1	695	1,001
• •	• •	• •	• •	• •
1000 0000	1	1	351	658
0111 1111	1	1	349	656
0111 1111	0	1	349	349
• •	• •	• •	• •	• •
0000 0010	1	1	5	312
0000 0001	1	1	3	310
0000 0000	1	1	0	307
0000 0000	0	1	0	0
XXXX XXXX	1	0	0	307
XXXX XXXX	0	0	0	0

Pin Assignments

LQFP Package



Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
Clock and Data Inputs			
CLK	26	CMOS	**Clock Input.** Pixel data is registered on the rising edge of CLK. CLK should be driven by a dedicated buffer to avoid reflection induced jitter, overshoot, and undershoot.
R_{7-0} G_{7-0} B_{7-0}	47-40 9-2 23-16	CMOS	**Red, Green, and Blue Pixel Data Inputs.** RGB digital inputs are registered on the rising edge of CLK.
Controls			
$\overline{SYNC}$	11	CMOS	**Sync Pulse Input.** Bringing $\overline{SYNC}$ LOW, disables a current source which superimposes a sync pulse on the I_{OG} output. $\overline{SYNC}$ and pixel data are registered on the rising edge of CLK. $\overline{SYNC}$ does not override any other data and should be used only during the blanking interval. If sync pulses are not required, $\overline{SYNC}$ should be connected to GND.
$\overline{BLANK}$	10	CMOS	**Blanking Input.** When $\overline{BLANK}$ is LOW, pixel data inputs are ignored and the D/A converter outputs are driven to the blanking level. $\overline{BLANK}$ is registered on the rising edge of CLK.
Video Outputs			
I_{OR} I_{OG} I_{OB}	33 32 29	0.700 V_{p-p}	**Red, Green, and Blue Current Outputs.** Current source outputs can drive VESA VSIS, and RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines. Sync pulses can be added to the green output. When $\overline{SYNC}$ is HIGH, the current added to I_{OG} is: $IO_S = 2.33 (V_{REF} / R_{REF})$
Voltage Reference			
V_{REF}	35	+1.25 V	**Voltage Reference Input/Output.** Internal 1.25V voltage reference is available on this pin. An external +1.25 Volt reference may be applied to this pin to override the internal reference. Decoupling V_{REF} to GND with a 0.1µF ceramic capacitor is required.
R_{REF}	36	348 Ω	**Current-set Resistor Node.** Full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. Nominal value of R_{REF} is found from: $R_{REF} = 5.31 (V_{REF}/I_{FS})$ where I_{FS} is the full-scale output current (amps) from the D/A converter (without sync). Sync is 0.439 I_{FS}. D/A full-scale current may also be calculated from: $I_{FS} = V_{FS}/R_L$ Where V_{FS} is the full-scale voltage level and R_L is the total resistive load (ohms) on each D/A converter.
COMP	34	0.1 µF	**Compensation Capacitor Node.** A 0.1 µF ceramic capacitor must be connected between COMP and V_{DD} to stabilize internal bias circuitry.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
Power, Ground			
V_{DDA}	30, 31	+3.3V	**Analog Supply Voltage.**
V_{DDD}	12	+3.3V	**Digital Supply Voltage.**
GND	1, 14, 15, 27, 28, 38, 39, 48	0.0V	**Ground.**
NC	13, 24, 25, 37	—	**No Connect**

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage				
V_{DDA} (Measured to GND)	-0.5		4	V
V_{DDD} (Measured to GND)	-0.5		4	V
Digital Inputs				
Applied Voltage (Measured to GND)[2]	-0.5		V_{DDD} + 0.5	V
Forced Current[3,4]	-5.0		5.0	mA
Analog Inputs				
Applied Voltage (Measured to GND)[2]	-0.5		V_{DDA} + 0.5	V
Forced Current[3,4]	-10.0		10.0	mA
Analog Outputs				
Applied Voltage (Measured to GND)[2]	-0.5		V_{DDA} + 0.5	V
Forced Current[3,4]	-60.0		60.0	mA
Short Circuit Duration (single output in HIGH state to ground)			unlimited	sec.
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{REF}	Reference Voltage, External	1.0	1.25	1.5	V
C_C	Compensation Capacitor		0.1		µF
R_L	Output Load		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C

Test Rank Definitions

Rank	
P	Production tested at 25°C.
D	Guaranteed by design over full temperature range.
C	Guaranteed by characterization and design over full temperature range.
T	Target specification, pending characterization.

Electrical Characteristics[1]

Parameter			Temp	Test Rank	Min	Typ	Max	Unit
Power Supply Currents								
I_{DD}	Supply Current	FMS3818	25°C	P		80		mA
		FMS3818	Full	C			90	
	Power Dissipation		Full	D			300	mW
Digital Inputs								
V_{IH}	Input Voltage, HIGH		Full	PC	2.5			V
V_{IL}	Input Voltage, LOW		Full	PC			0.8	V
I_{IH}	Input Current, HIGH		Full	PC	-1		+1	µA
I_{IL}	Input Current, LOW		Full	PC	-1		+1	µA
C_I	Input Capacitance		25°C	D		4		pF
Analog Outputs								
	Output Current		25°C	PC			30	mA
R_O	Output Resistance		25°C	C		40		kΩ
C_O	Output Capacitance		25°C	D		7		pF
Reference Output								
V_{REF}	Output Voltage		Full	PC	1.135	1.25	1.365	V
	Temperature Coefficient		Full	CT				ppm/°C

Note:

1. Specified under normal operation conditions: $V_{DDA} = V_{DDD} = 3.3V$ with external 1.25V reference.

Switching Characteristics[1]

Parameter			Temp	Test Rank	Min	Typ	Max	Unit
Clock Input								
	Conversion rate	FMS3818	Full	C			180	Ms/s
t_{PWH}	Pulse-width HIGH		Full	C	2			ns
t_{PWL}	Pulse-width LOW		Full	C	2			ns
Data Inputs								
t_S	Setup	FMS3818	25°C	P	1.5			ns
		FMS3818	Full	C	2			ns
t_H	Hold	FMS3818	25°C	P			0.6	ns
		FMS3818	Full	C			0.6	ns
Data Outputs[2]								
t_D	Clock to Output Delay		Full	C		1.6		ns
t_R	Rise Time		Full	C		0.6		ns
t_F	Fall Time		Full	C		0.4		ns
t_{SET}	Settling Time			C		2.5		ns
t_{SKEW}	Skew			C		0.3		ns

Notes:

1. Specified under normal operation conditions: $V_{DDA} = V_{DDD} = 3.3V$ with external 1.25V reference.
2. With 50Ω doubly terminated load with internal 1.25V reference.

DC Performance[1]

Parameter		Temp	Test Rank	Min	Typ[1]	Max	Unit
	Resolution	Full	D	8			bits
DNL	Differential Non-Linearity Error	25°C	P	-0.5		+0.5	LSB
		Full	C	-0.5		+0.5	
INL	Integral Non-Linearity Error	25°C	P	-0.5		+0.5	LSB
		Full	C	-0.5		+0.5	
	Offset Error	Full	PC			0.01	%FS
	Gain Matching Error	Full	PC	-2.5		+2.5	%FS
	Absolute Gain Error[1]	Full	PC	-3.5		+3.5	%FS
	Full-scale Output Current[1]	Full	C	18.0	18.7	19.4	mA
		25°C	P				
	Full-scale Output Current[2]	Full	PC		18.7		mA
PSRR	Power Supply Rejection Ratio (DC)	Full	C	-0.01	0	+0.01	%/%
Thermal							
θ_{JC}	Resistance, Junction-to-Case						°C/W
θ_{JA}	Resistance, Junction-to-Ambient		D		91		°C/W

Notes:

1. Specified under normal operation conditions: $V_{DDA} = V_{DDD} = 3.3V$ with external 1.25V reference. $R_{REF} = 348\Omega$.
2. With internal reference. Trim R_{SET} to calibrate full-scale current.

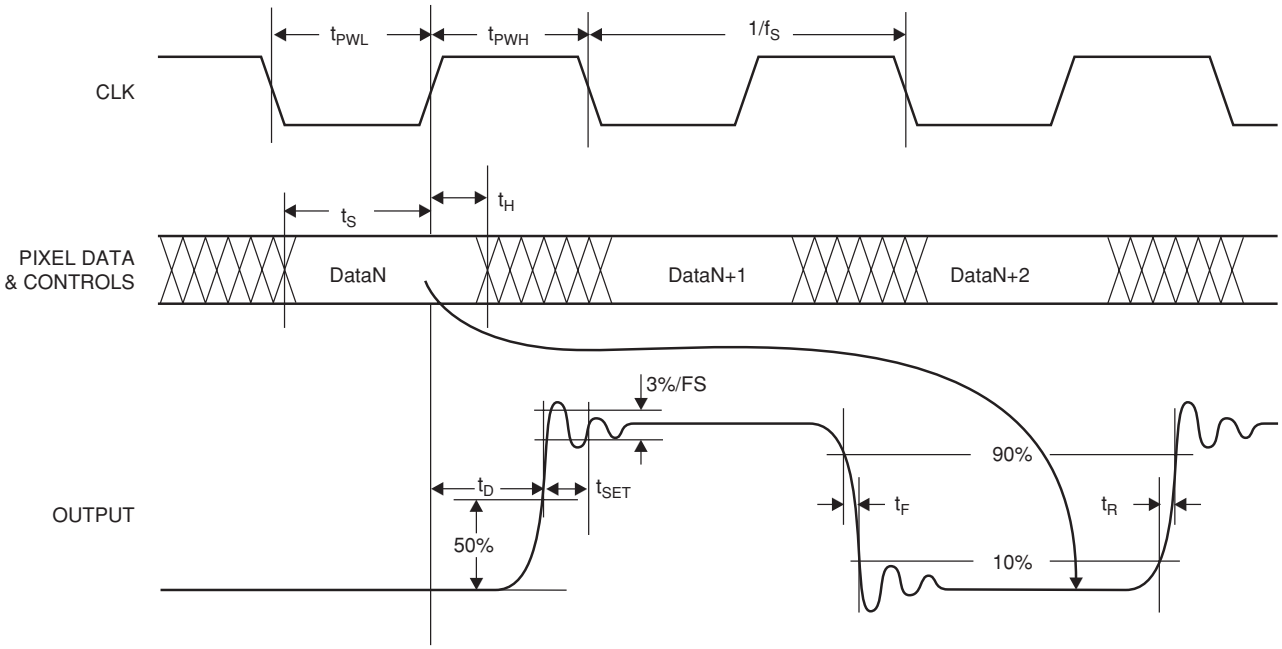
AC Performance[1]

Parameter	Temp	Test Rank	Min	Typ[1]	Max	Unit
Analog Outputs						
Glitch Energy	7	C		20		pVsec
DAC-to-DAC Crosstalk	25°C	C		30		dB
Data Feedthrough	25°C	C		50		dB
Clock Feedthrough	25°C	C		60		dB

Note:

1. Specified under normal operation conditions: $V_{DDA} = V_{DDD} = 3.3V$ with external 1.25V reference.

Timing Diagram



Applications Information

Figure 4 illustrates a typical FMS3818 interface circuit. In this example, an optional 1.2 Volt bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the FMS3818 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The FMS3818 has separate analog and digital circuits. To keep digital system noise away from the D/A converter, it is recommended that power supply voltages come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_S, IO_R, IO_G) as short as possible and as far as possible from all digital signals. The FMS3818 should be located near the board edge, close to the analog output connectors.

2. The power plane for the FMS3818 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the FMS3818 is the same as that of the system's digital circuitry, power to the FMS3818 should be decoupled with 0.1µF and 0.01µF capacitors and isolated with a ferrite bead.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. If the digital power supply has a dedicated power plane layer, it should not be placed under the FMS3818, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the FMS3818 and its related analog circuitry can have an adverse effect on performance.

5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Improved Transition Times

Output shunt capacitance dominates slowing of output transition times, whereas series inductance causes a small amount of ringing that affects overshoot and settling time. With a doubly terminated 75Ω load, transition times can be improved by matching the capacitive impedance output of the FMS3818. Output capacitance can be matched with a 220 nH inductor in series with the 75Ω source termination.

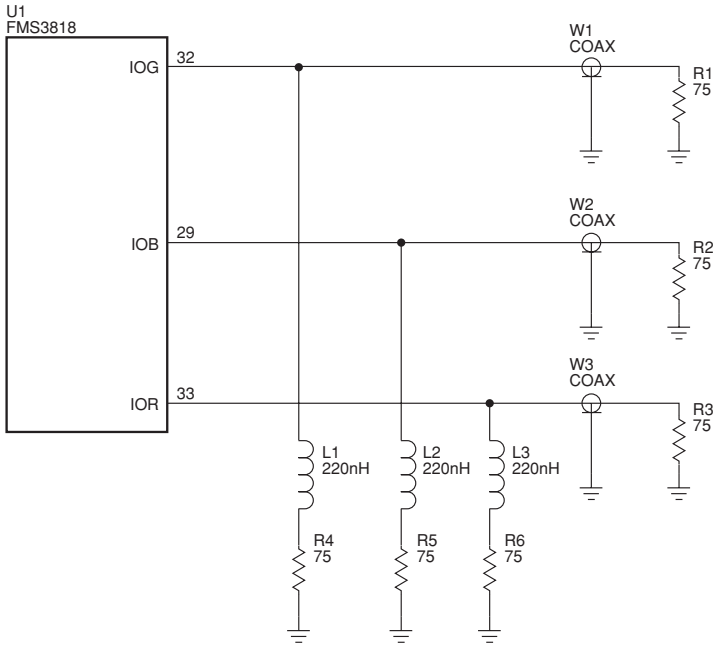


Figure 3. Schematic, FMS3818 Transition Time Sharpening Circuit

A 220 nH inductor trims the performance of a 4 ft cable, quite well. In Figures 4 through 7, the glitch at 12.5 ns, is due to a reflection from the source. Not shown, are smaller glitches at 25 and 37.5 ns, corresponding to secondary and tertiary reflections. Inductor values should be selected to match the length and type of the cable.

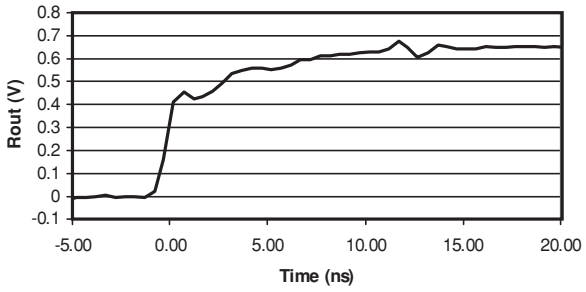


Figure 4. Unmatched t_R.

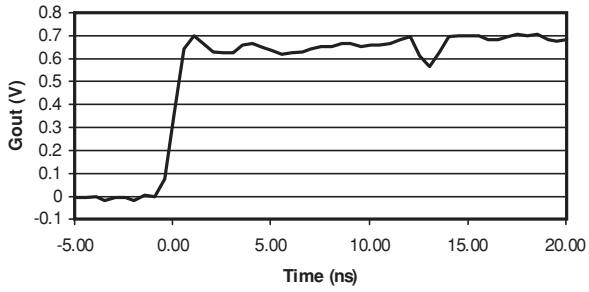


Figure 5. Matched t_R.

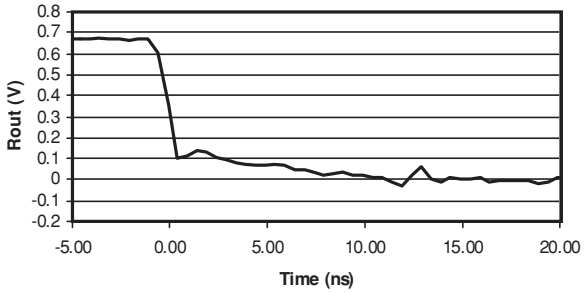


Figure 6. Unmatched t_F.

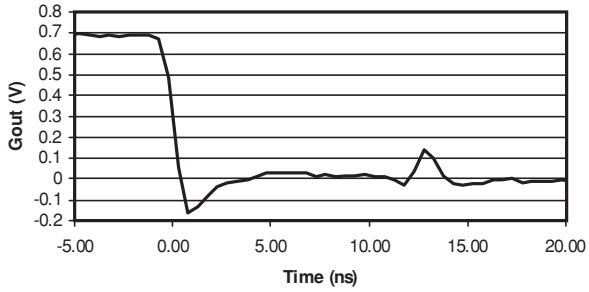


Figure 7. Matched t_F.

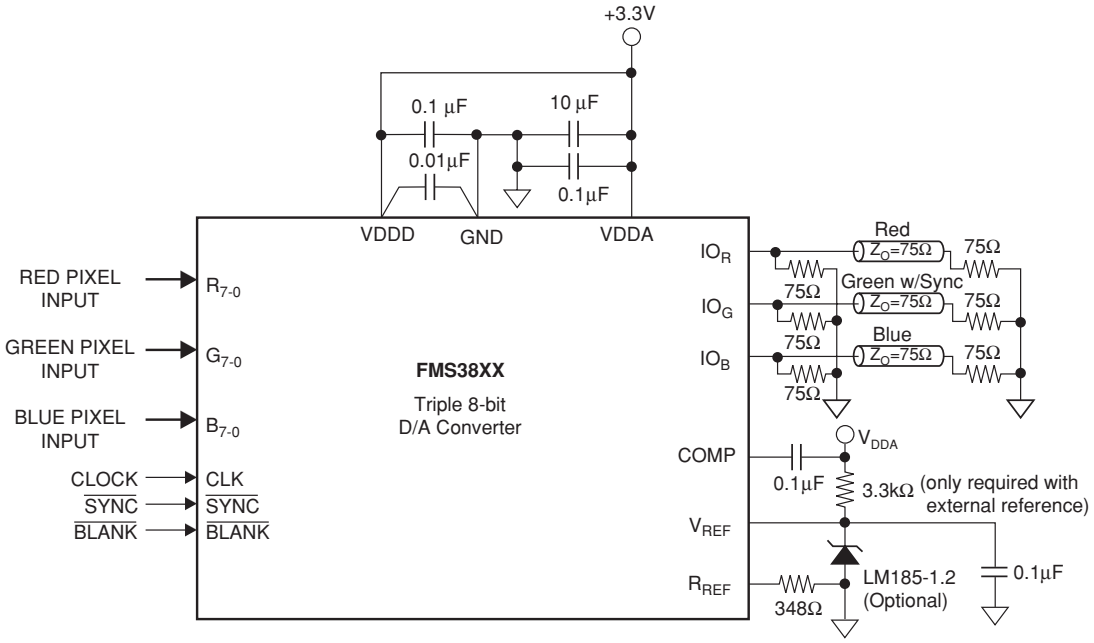


Figure 8. Typical Interface Circuit

Related Products

- FMS3110/3115 Triple 10-bit 150 Msps D/A Converters
- FMS9884A 3 x 8 bit 140 Ms/s A/D Converter

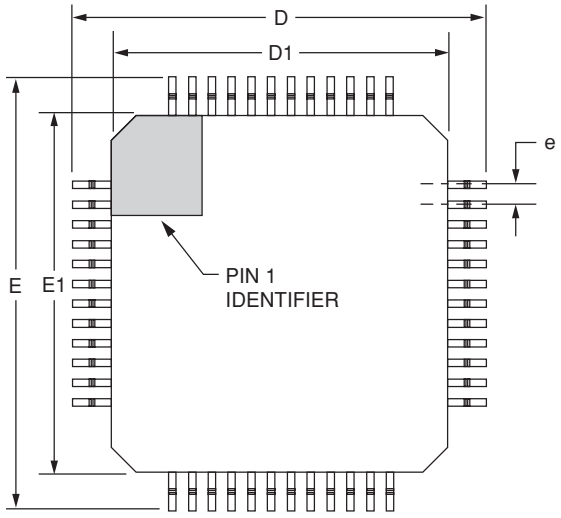
Mechanical Dimensions

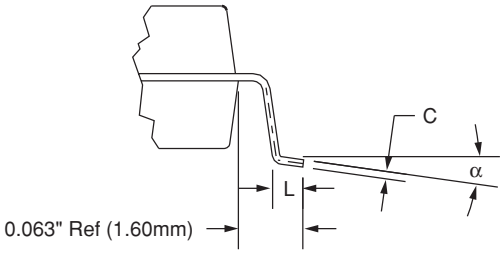
48-Lead LQFP Package

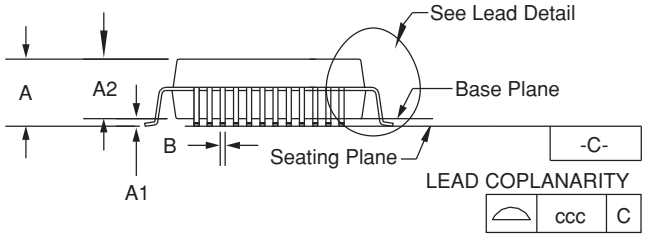
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.055	.063	1.40	1.60	
A1	.001	.005	.05	.15	
A2	.053	.057	1.35	1.45	
B	.006	.010	.17	.27	7
D/E	.346	.362	8.8	9.2	
D1/E1	.268	.284	6.8	7.2	2
e	.019 BSC		.50 BSC		
L	.017	.029	.45	.75	6
N	48		48		4
ND	12		12		5
α	0°	7°	0°	7°	
ccc	.004		0.08		

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Pin 1 identifier is optional.
4. Dimension N: Number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm.







Ordering Information

Product Number	Conversion Rate	Lead Free	Temperature Range	Screening	Package	Package Marking
FMS3818KRC	180 Ms/s		0°C to 70°C	Commercial	48-Lead LQFP	3818KRC
FMS3818KRC_NL	180 Ms/s	Yes	0°C to 70°C	Commercial	48-Lead LQFP	3818KRC NL