



January 2006

# QFET™

## FQB3N60C

### 600V N-Channel MOSFET

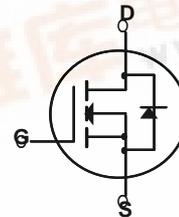
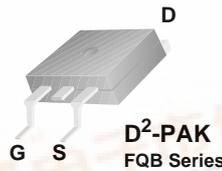
#### Features

- 3A, 600V,  $R_{DS(on)} = 3.4\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 10.5 nC)
- Low  $C_{rss}$  ( typical 5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



#### Absolute Maximum Ratings

Symbol	Parameter	FQB3N60C	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	3 1.8	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	12	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	150	mJ
$I_{AR}$	Avalanche Current (Note 1)	3	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ ) - Derate above $25^\circ C$	75 0.62	W W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

#### Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.67	$^\circ C/W$
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	--	40	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ C/W$

\* When mounted on the minimum pad size recommended (PCB Mount)



## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB3N60C	FQB3N60CTM	D2-PAK	330mm	24mm	800

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	600	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.6	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 480V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.5A	--	2.8	3.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 1.5A (Note 4)	--	3.5	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	435	565	pF
C <sub>oss</sub>	Output Capacitance		--	45	60	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	5	8	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 3A R <sub>G</sub> = 25Ω  (Note 4, 5)	--	12	34	ns
t <sub>r</sub>	Turn-On Rise Time		--	30	70	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	35	80	ns
t <sub>f</sub>	Turn-Off Fall Time		--	35	80	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 3A V <sub>GS</sub> = 10V  (Note 4, 5)	--	10.5	14	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2.1	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	4.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	3	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 3A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 3A di <sub>F</sub> /dt = 100A/μs  (Note 4)	--	260	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.6	--	μC

### NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 3A, V<sub>DD</sub> = 50V, L=30mH, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 3A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

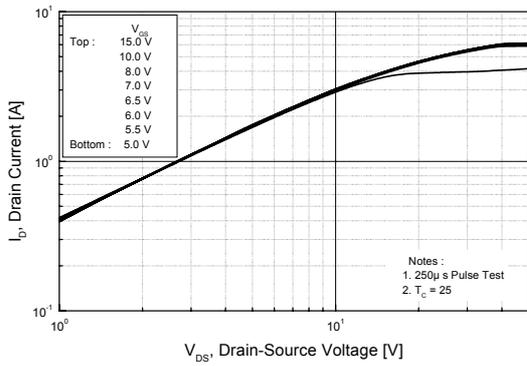


Figure 2. Transfer Characteristics

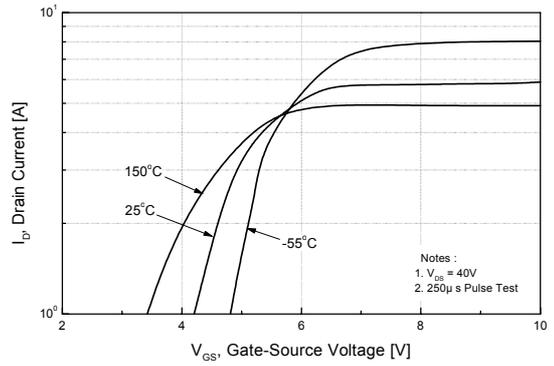


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

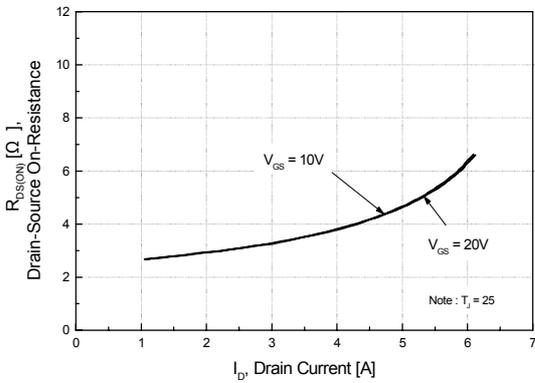


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

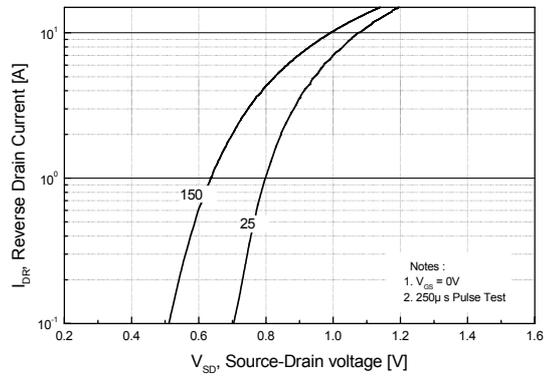


Figure 5. Capacitance Characteristics

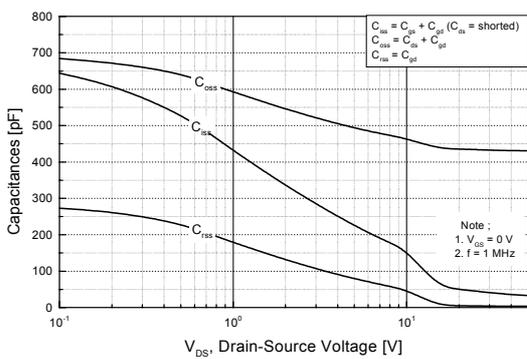
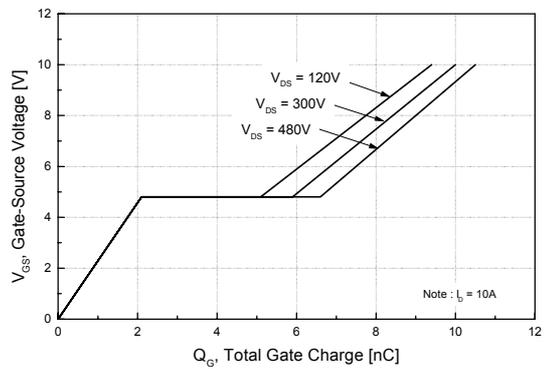
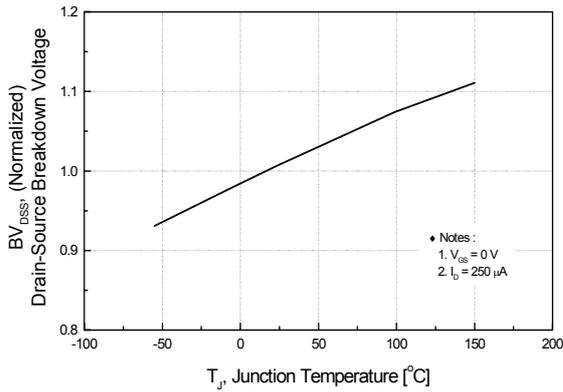


Figure 6. Gate Charge Characteristics

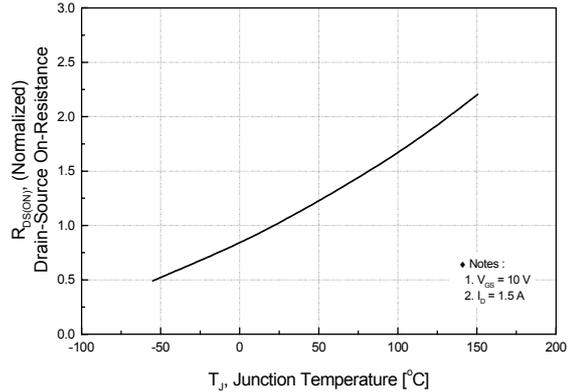


### Typical Performance Characteristics (Continued)

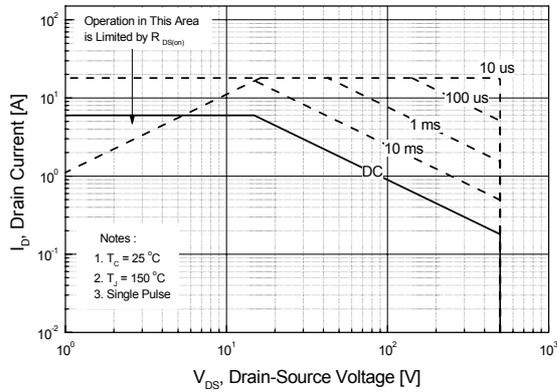
**Figure 7. Breakdown Voltage Variation vs. Temperature**



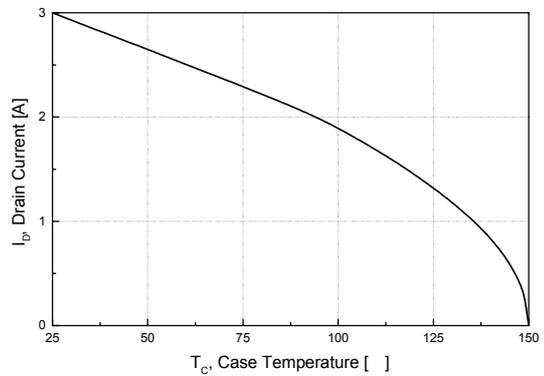
**Figure 8. On-Resistance Variation vs. Temperature**



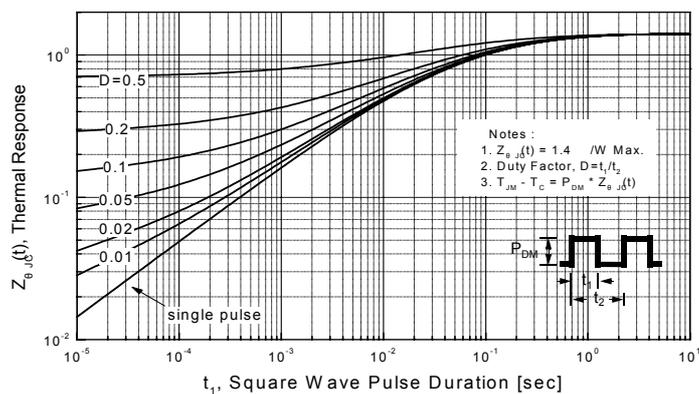
**Figure 9. Maximum Safe Operating Area**



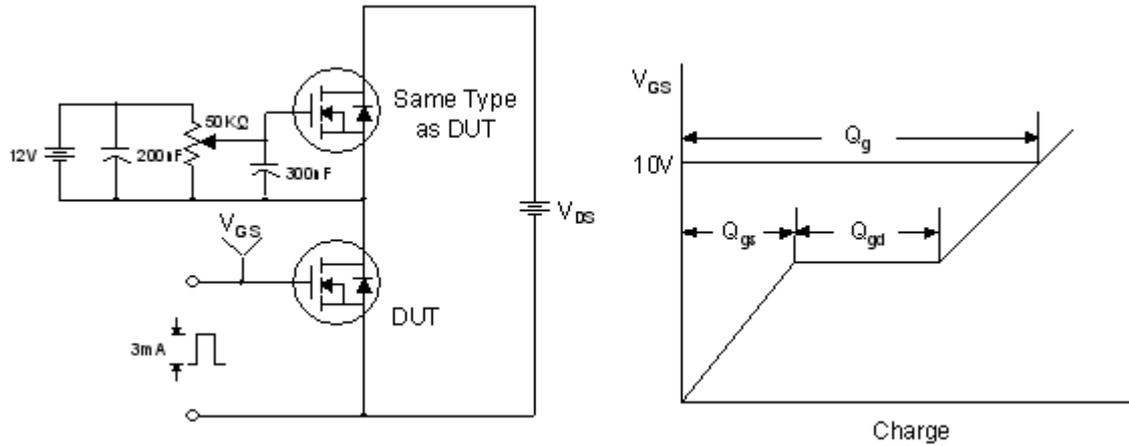
**Figure 10. Maximum Drain Current vs. Case Temperature**



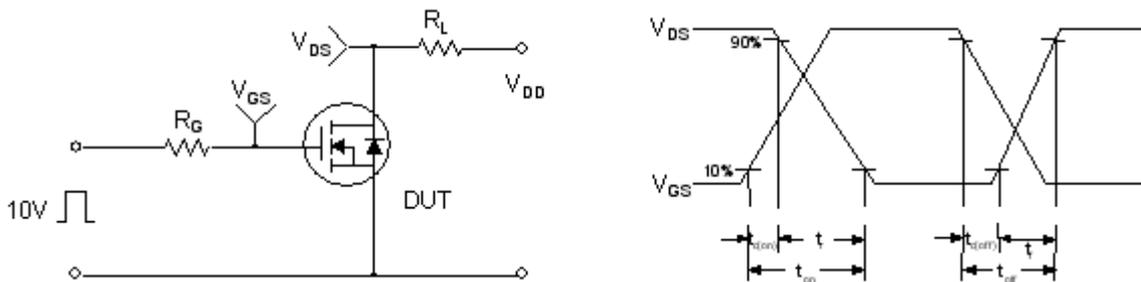
**Figure 11. Transient Thermal Response Curve**



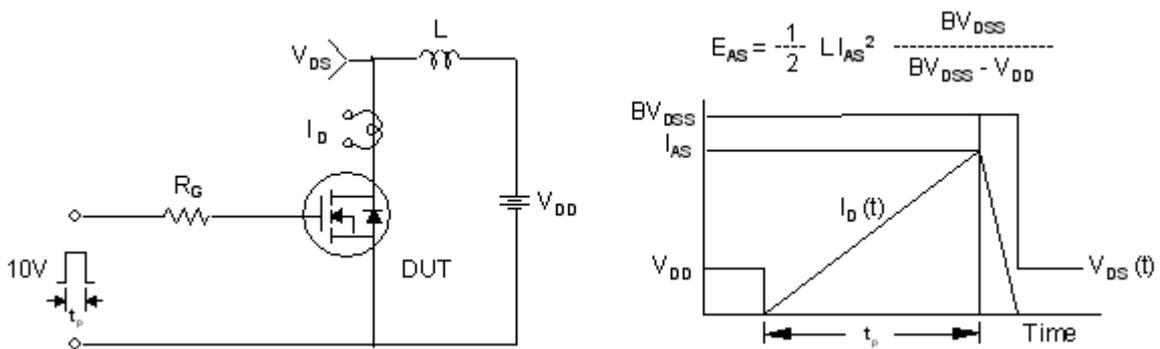
Gate Charge Test Circuit & Waveform



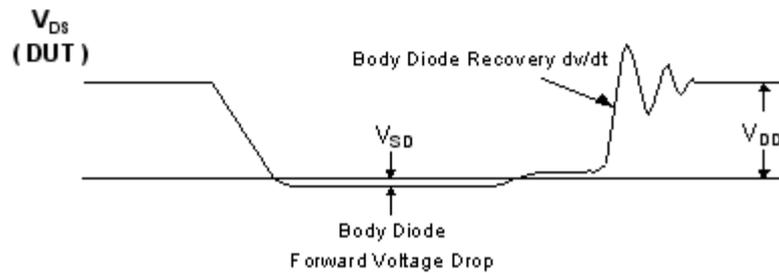
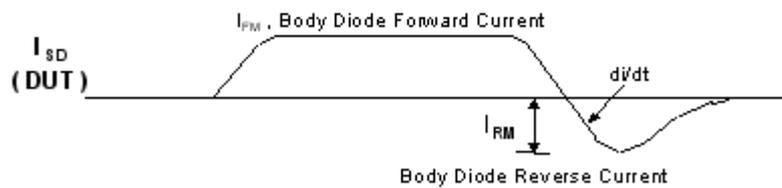
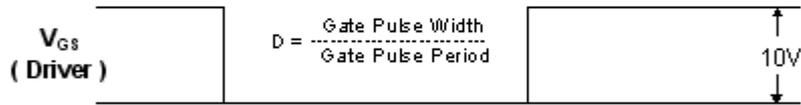
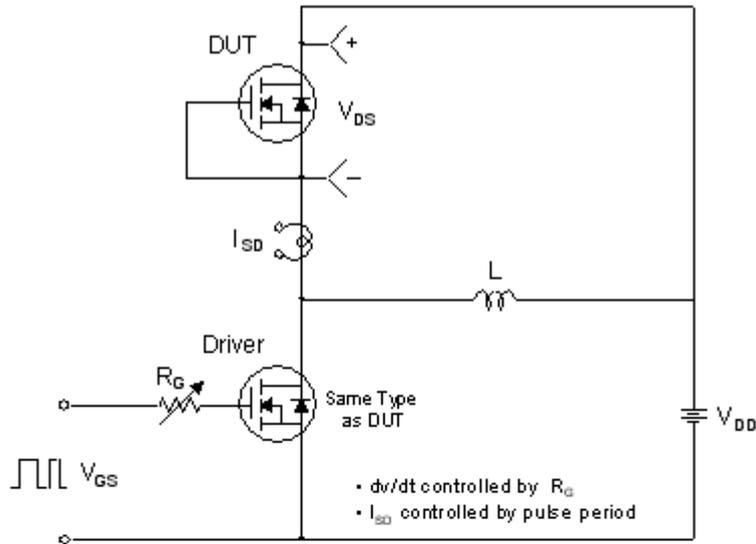
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

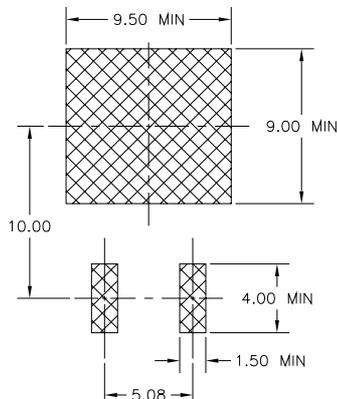
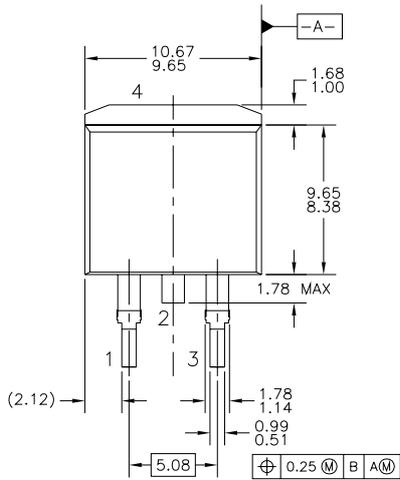


Peak Diode Recovery dv/dt Test Circuit & Waveforms

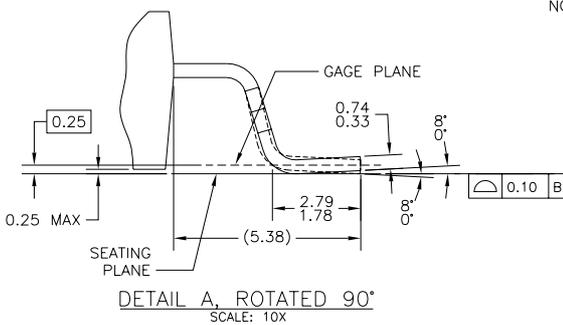
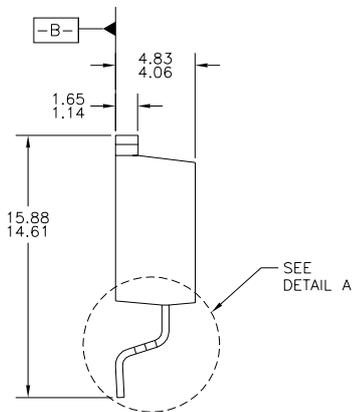
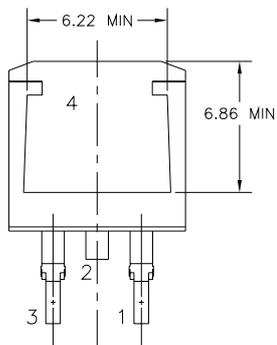


Mechanical Dimensions

D2-PAK



LAND PATTERN RECOMMENDATION



DETAIL A, ROTATED 90°  
SCALE: 10X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
  - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
  - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

TO263A02REVD

Dimensions in Millimeters

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CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOMETM	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I <sup>2</sup> C™	MSXPro™	RapidConnect™	UHC™
E <sup>2</sup> C MOS™	i-Lo™	OCX™	μSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
The Power Franchise®		POP™	Stealth™	
Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

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Datasheet Identification	Product Status	Definition
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