Quad High Speed ±90V 2.2A Ultrasound Pulser

Features

- HVCMOS technology for high performance
- High density integration ultrasound transmitter
- 0 to ±90V output voltage
- ±2.2A source and sink current in PW mode
- ±580mA source and sink current in CW mode
- Up to 20MHz operating frequency
- Matched delay times
- 1.2V to 5.0V CMOS logic interface
- Built-in output drain bleed resistors

Application

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- NDT ultrasound transmission
- Pulse waveform generator

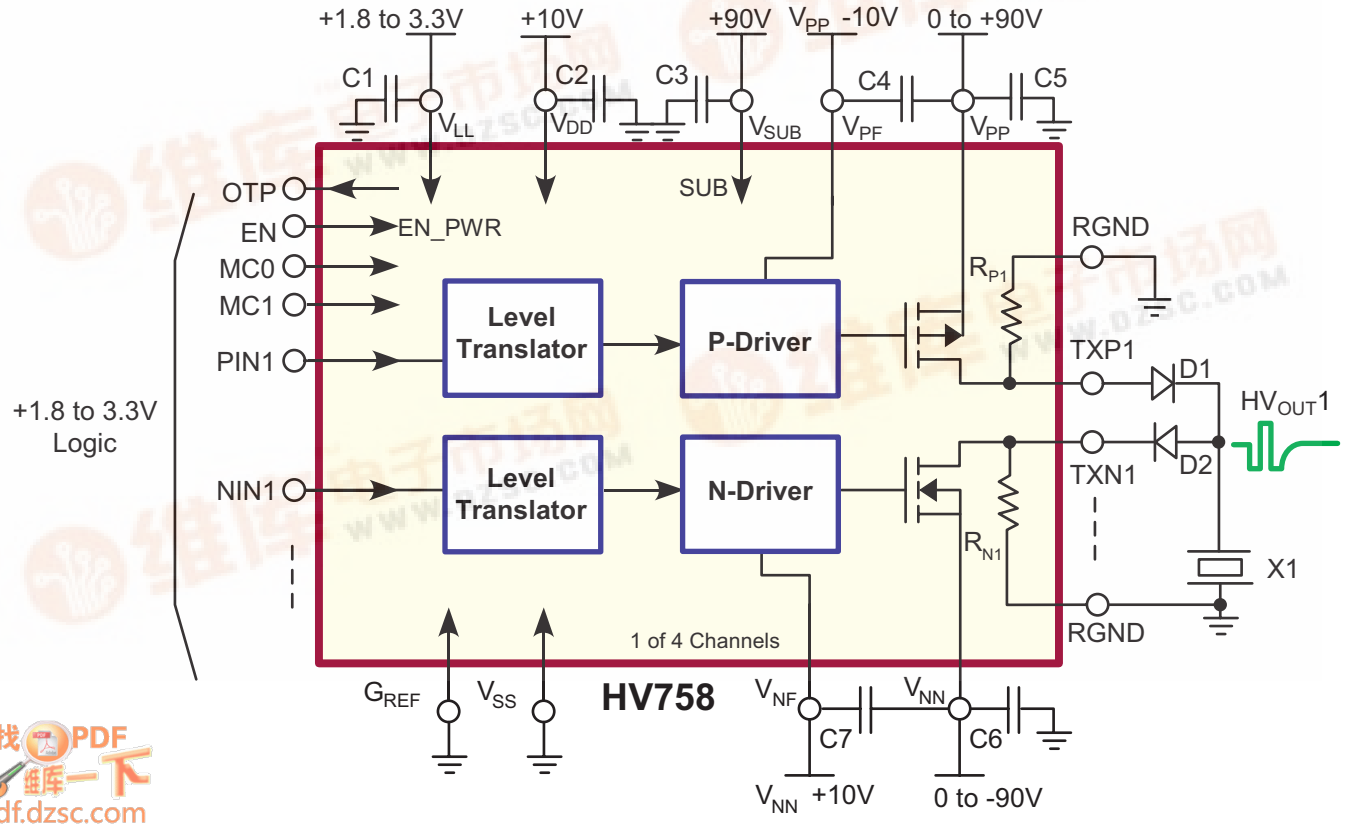
General Description

The Supertex HV758 is a four-channel, monolithic high voltage, high-speed pulse generator. It is designed for medical ultrasound applications. This high voltage and high-speed integrated circuit can also be used for other piezoelectric, capacitive or MEMS transducers in ultrasonic nondestructive detection and sonar ranger applications.

The HV758 comprises a controller logic interface circuit, level translators, MOSFET gate drives and high current power P-channel and N-channel MOSFETs as the output stage for each channel.

The output current limit can be set to one of four levels by using two mode control inputs. The output stages of each channel are designed to provide peak output currents over ±2.5A when in mode 4, with up to 180V swings. When in mode 1, the output stages reduce the peak current to ±580mA for CW mode operation, which reduces the power dissipation of the IC. The power MOSFET gate drivers are supplied by two floating 10VDC power supplies referenced to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

Typical Application Circuit



Ordering Information

Device	Package Options	
	64-Ball FCBGA *8x8mm body, 2.45mm height (max), 0.8mm pitch*	
HV758	HV758FB	HV758FB-G

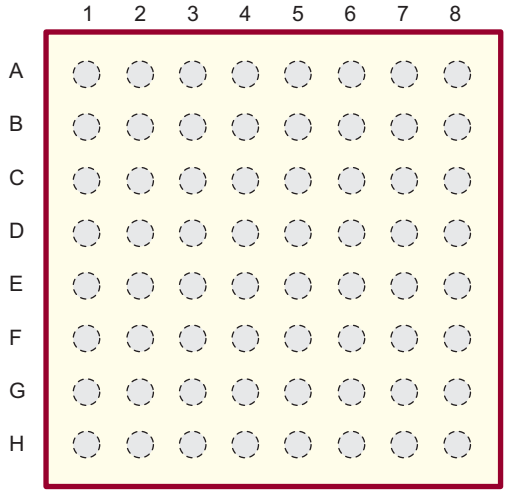
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{SS}, Power supply reference	0V
V_{LL}, Positive logic supply	-0.5V to +7.0V
V_{DD}, Positive logic and level translator supply	-0.5V to +14V
(V_{PP} - V_{PF}) Positive floating gate drive supply	-0.5V to +14V
(V_{NF} - V_{NN}) Negative gate floating drive supply	-0.5V to +14V
(V_{PP} - V_{NN}) Differential high voltage supply	+190V
V_{PP}, High voltage positive supply	-0.5V to +95V
V_{NN}, High voltage negative supply	+0.5V to -95V
OTP, Over Temperature Protection output	-0.5V to +7.0V
All logic input PIN_X, NIN_X and EN voltages	-0.5V to +7.0V
(V_{SUB} - V_{PP}) Substrate to V_{PP} voltage difference	+190V
(V_{PP} - TXP_X) V_{PP} to TXP_X voltage difference	+190V
(V_{SUB} - TXP_X) Substrate to TXP_X voltage difference	+190V
(TXN_X - V_{NN}) TXN_X to V_{NN} voltage difference	+190V
Operating temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C
Thermal resistance, θ_{JA}, *(4 layer, 1oz., 4x3", 36-via PCB)*	12.8°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



64-Ball FCBGA
(top view)

Package Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

64-Ball FCBGA

Power-Up Sequence

1	V_{SUB}
2	V_{LL} with logic signal low
3	V_{DD}
4	(V_{PP} - V_{PF}) and (V_{NF} - V_{NN})
5	V_{PP} and V_{NN}
6	Logic control signals

Power-Down Sequence

1	All logic signals go to low
2	V_{PP} and V_{NN}
3	(V_{PP} - V_{PF}) and (V_{NF} - V_{NN})
4	V_{DD}
5	V_{LL}
6	V_{SUB}

Operating Supply Voltages and Current (4 Channel Active)

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +10V, V_{PP}-V_{PF} = +10V, V_{NN}-V_{NF} = -10V, V_{PP} =+90V, V_{NN} = -90V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic voltage reference	1.2	2.5	5.0	V	---
V_{DD}	Internal voltage supply	7.5	12	12.6	V	---
V_{PF}	Positive gate driver supply	(V_{PP}-12.6)	(V_{PP}-12)	(V_{PP}-7.5)	V	Floating driver voltage supplies equals V_{DD}.
V_{NF}	Negative gate drive supply	(V_{NN}+7.5)	(V_{NN}+12)	(V_{NN}+12.6)	V	
V_{SUB}	IC substrate voltage	V_{DD}	V_{PP}	+90	V	Must be the most positive potential of the IC.
V_{PP}	Positive HV supply	0	-	+90	V	---
V_{NN}	Negative HV supply	-90	-	0	V	---
SR_{max}	Allowable slew rate on $V_{PP,}$ V_{NN}	-	-	25	V/µs	---
I_{LL}	V_{LL} Current EN = Low	-	125	250	µA	---
I_{DDQ}	V_{DD} Current EN = Low	-	100	-	µA	---
I_{DDEN}	V_{DD} Current EN = High	-	1.1	2.0	mA	f = 0MHz
I_{DDEN}	V_{DD} Current MODE = 4	-	3.2	-	mA	f = 5.0MHz, continuous, no loads
I_{DDENCW}	V_{DD} Current MODE = 1	-	3.1	-	mA	
I_{PPQ}	V_{PP} Current EN = Low	-	74	90	µA	f = 0MHz
I_{PPEN}	V_{PP} Current MODE = 4	-	258	-	mA	f = 5.0MHz, continuous, no loads
I_{PPENCW}	V_{PP} Current MODE = 1	-	215	-	mA	
I_{NNQ}	V_{NN} Current EN = Low	-	78	90	µA	f = 0MHz
I_{NNEN}	V_{NN} Current MODE = 4	-	258	-	mA	f = 5.0MHz, continuous, no loads
I_{NNENCW}	V_{NN} Current MODE = 1	-	215	-	mA	
I_{PFQ}	V_{PF} Current EN = Low	-	37	70	µA	f = 0MHz
I_{PFEN}	V_{PF} Current MODE = 4	-	70	-	mA	f = 5.0MHz, continuous, no loads
I_{PFENCW}	V_{PF} Current MODE = 1	-	9.0	-	mA	
I_{NFQ}	V_{NF} Current EN = Low	-	35	70	µA	f = 0MHz
I_{NFEN}	V_{NF} Current MODE = 4	-	42	-	mA	f = 5.0MHz, continuous, no loads
I_{NFENCW}	V_{NF} Current MODE = 1	-	6.0	-	mA	

Note: *All supply current values are for reference only.*

Under Voltage and Over Temperature Protection

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PULL_UP}	Open drain pull-up voltage	-	-	5.0	V	---
V_{UVDD}	V_{DD} threshold	3.5	5.7	7.0	V	---
V_{UVLL}	V_{LL} threshold	0.8	0.9	1.0	V	---
V_{UVVF}	V_{PF}, V_{NF} threshold	2.7	4.0	5.4	V	---
V_{OL_OTP}	OTP flag output low voltage	-	-	1.0	V	V_{LL} = 2.5V, OTP = Active, I_{PULL_UP} = 1.0mA.
I_{OTP}	Max. open drain output current	-	1.0	-	mA	---
T_{OTP}	Over-temperature threshold	95	110	125	°C	If over-temperature occurred, OTP low and all TX outputs will be HiZ.
T_{HYS}	OTP output reset hysteresis	-	7.0	-		

Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +10V, V_{PP}-V_{PF} = +10V, V_{NN}-V_{NF} = -10V, V_{PP} =+90V, V_{NN} = -90V, T_A = 25°C)

Output P-Channel MOSFET, TXP (Mode 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	2.2	2.5	-	A	---
R_{ON}	Channel resistance	-	11	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	215	-	pF	V_{DS} = 25V, f = 1.0MHz

Output N-Channel MOSFET, TXN (Mode 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	2.1	2.2	-	A	---
R_{ON}	Channel resistance	-	11	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	90	-	pF	V_{DS} = 25V, f = 1.0MHz

MOSFET Drain Bleed Resistor

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{P/N1\sim4}$	Output bleed resistance	10	15	20	kΩ	---
P_{RO}	Bleed resistors power limit	-	-	40	mW	---

Logic Inputs

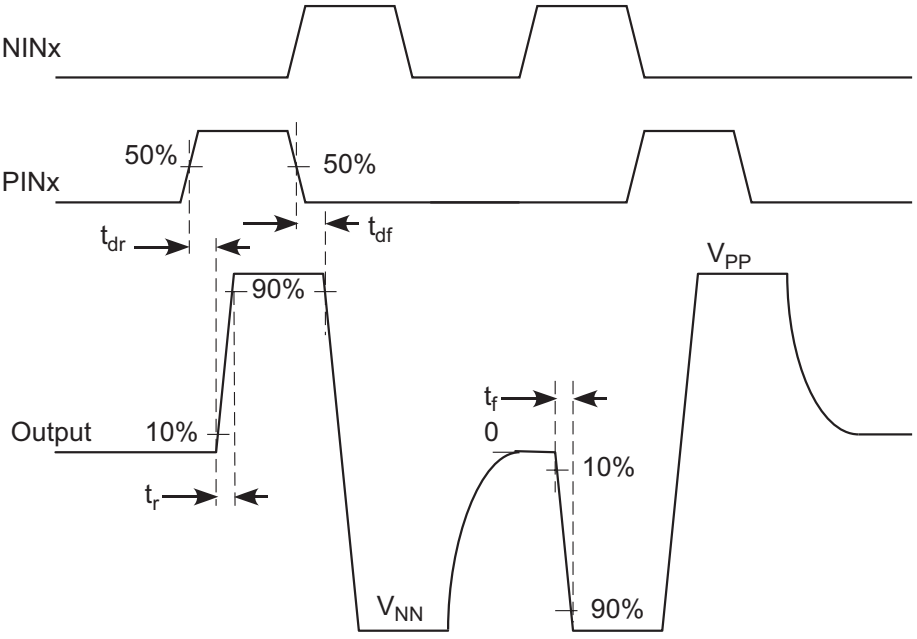
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	(V_{LL}-0.4)	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	0.4	V	---
I_{IH}	Input logic high current	-	-	10	µA	---
I_{IL}	Input logic low current	-10	-	-	µA	---
C_{IN}	Input logic capacitance	-	-	5.0	pF	---

AC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +10V, V_{PP}-V_{PF} = +10V, V_{NN}-V_{NF} = -10V, V_{PP} =+90V, V_{NN} = -90V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_r	Output rise time	-	32	-	ns	330pF//2.5kΩ load
t_f	Output fall time	-	32	-	ns	
f_{OUT}	Output frequency range	20	-	-	MHz	100Ω resistor load
HD2	Second harmonic distortion	-	30	-	dB	
t_{EN}	Enable time	-	70	250	µs	
t_{dr}	Delay time on inputs rise	-	18	-	ns	
t_{df}	Delay time on inputs fall	-	18	-	ns	
t_{dm}	Delay on mode change	-	2.5	20	µs	
Δt_{DELAY}	$\lvert t_{dr}-t_{df} \rvert$ delay time matching	-	-	±3.0	ns	P to N, channel to channel
t_j	Delay jitter on rise or fall	-	15	-	ps	V_{PP}/V_{NN} = +/-25V, input t_r 50% to HV_{OUT} t_r or t_f 50%, with 330pF//2.5kΩ load

Switching Time Diagram



Truth Table (All Modes)

Logic Inputs			Output	
EN	PIN_x	NIN_x	TXP_x	TXN_x
1	0	0	OFF	OFF
1	1	0	ON	OFF
1	0	1	OFF	ON
1	1	1	ON*	ON*
0	X	X	OFF	OFF

***Note:** Not allowed, may damage IC*

Drive Mode Control Table

Mode	MC1	MC0	I_{SC} (A)	R_{ONP} (Ω)	R_{ONR} (Ω)
1	0	0	0.58	28	27
2	0	1	0.8	20	19.7
3	1	0	1.35	12	11.7
4	1	1	2.5	6.5	6.3

Notes:

1. V_{PP}/V_{NN} = +/-90V, $V_{DD} = (V_{PP} - V_{PF}) = (V_{NF} - V_{NN})$ = +10V

2. I_{SC} is current into 1.0Ω to GND

3. R_{ON} calculated from V_{OUT} into 100Ω load

Ball Description

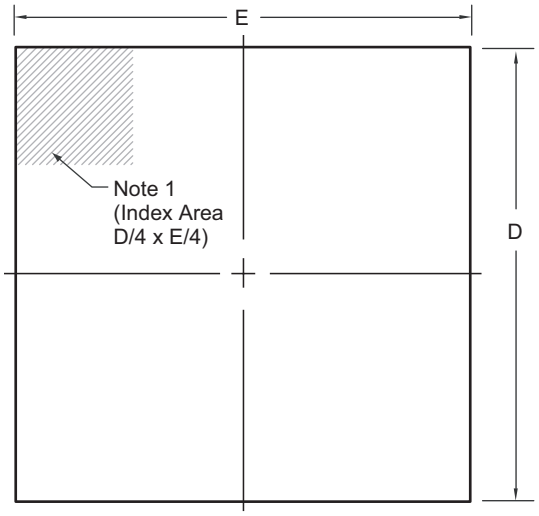
Name	Function
V_{DD}	Positive internal voltage supply (+10V).
V_{SS}	Power supply return (0V).
V_{LL}	Logic Hi voltage reference input (+3.3V).
G_{REF}	Logic Low reference, logic ground (0V).
V_{SUB}	Substrate of the IC, all V_{SUB} pins must connect externally to the most positive potential of the IC.
RGND	Bleed resistors common return ground.
V_{PP}	Positive high voltage power supply (+90V).
V_{NN}	Negative high voltage power supply (-90V).
V_{PF}	P-FET drive floating power supply, (V_{PP} - V_{PF}) = +10V.
V_{NF}	N-FET drive floating power supply, (V_{NF} - V_{NN}) = +10V.
TXP1	Output P-FET drain (open drain output) for channel 1.
TXN1	Output N-FET drain (open drain output) for channel 1.
TXP2	Output P-FET drain (open drain output) for channel 2.
TXN2	Output N-FET drain (open drain output) for channel 2.
TXP3	Output P-FET drain (open drain output) for channel 3.
TXN3	Output N-FET drain (open drain output) for channel 3.
TXP4	Output P-FET drain (open drain output) for channel 4.
TXN4	Output N-FET drain (open drain output) for channel 4.
PIN1	Input logic control of high voltage output P-FET of channel 1, Hi=on, Low=off.
NIN1	Input logic control of high voltage output N-FET of channel 1, Hi=on, Low=off.
PIN2	Input logic control of high voltage output P-FET of channel 2, Hi=on, Low=off.
NIN2	Input logic control of high voltage output N-FET of channel 2, Hi=on, Low=off.
PIN3	Input logic control of high voltage output P-FET of channel 3, Hi=on, Low=off.
NIN3	Input logic control of high voltage output N-FET of channel 3, Hi=on, Low=off.
PIN4	Input logic control of high voltage output P-FET of channel 4, Hi=on, Low=off.
NIN4	Input logic control of high voltage output N-FET of channel 4, Hi=on, Low=off.
EN	Chip power enable Hi=on, Low=off.
MC0, MC1	Output current mode control pins, see Drive Mode Control Table.
OTP	Over temperature protection output, open N-FET drain, active low if IC temperature >110°C.

Ball Configuration

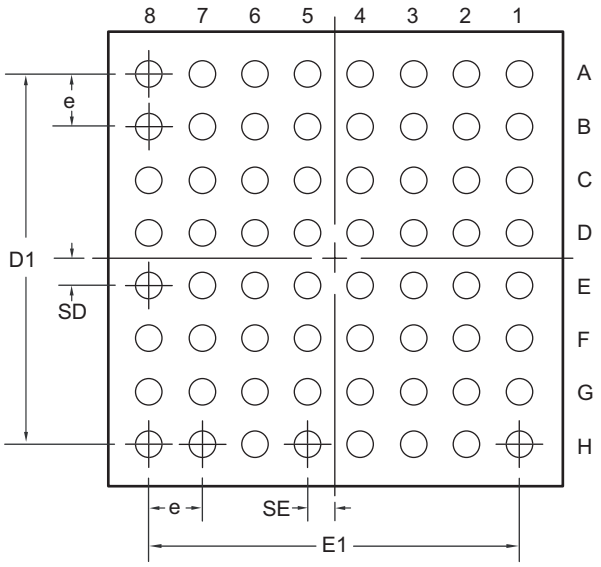
A1 Corner	1	2	3	4	5	6	7	8
A	V_{PF}	V_{PP}	V_{PP}	V_{NN}	V_{NN}	V_{NF}	TXN4	TXN4
B	V_{PF}	V_{PP}	V_{PP}	V_{NN}	V_{NN}	V_{NF}	TXP4	TXP4
C	V_{DD}	V_{SUB}	PIN4	NIN4	MC0	V_{SUB}	TXN3	TXN3
D	V_{SS}	OTP	PIN3	NIN3	MC1	RGND	TXP3	TXP3
E	V_{SS}	V_{LL}	PIN2	NIN2	EN	RGND	TXN2	TXN2
F	V_{DD}	V_{SUB}	PIN1	NIN1	G_{REF}	V_{SUB}	TXP2	TXP2
G	V_{PF}	V_{PP}	V_{PP}	V_{NN}	V_{NN}	V_{NF}	TXN1	TXN1
H	V_{PF}	V_{PP}	V_{PP}	V_{NN}	V_{NN}	V_{NF}	TXP1	TXP1

64-Ball FCBGA Package Outline (FB)

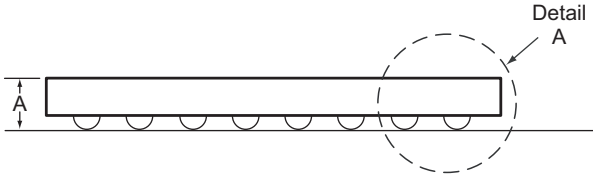
8x8mm body, 2.45mm height (max.), 0.80mm pitch



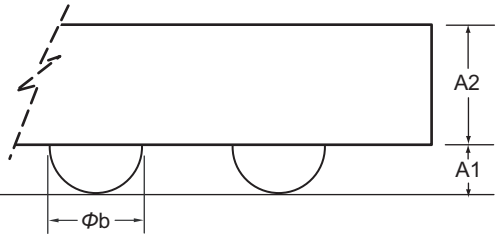
Top View



Bottom View



Side View



Detail A

Note 1:

Ball A1 identifier must be located in the index area indicated. Ball A1 corner identification can be used by ink or by metalized markings, or other features on package body. Shape of identifier is optional.

Symbol		A	A1	A2	Φb	D	D1	E	E1	e	SD	SE
Dimension (mm)	MIN	1.67	0.25	1.32	0.45	7.85	5.60 BSC	7.85	5.60 BSC	0.80 BSC	0.40 BSC	0.40 BSC
	NOM	1.82	0.40	1.42	0.50	8.00		8.00				
	MAX	2.45	0.45	2.20	0.55	8.15		8.15				

Drawings are not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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