High-Voltage Current-Mode PWM Controller

Features

- 10V to 120V Input Voltage Range
- Current-mode control
- High efficiency
- Up to 1.0MHz internal oscillator
- Internal start-up circuit
- Low internal noise

Applications

- DC/DC converters
- Distributed power systems
- ISDN equipment
- PBX systems
- Modems

General Description

The Supertex HV9112 is a BiCMOS/DMOS single-output, pulse width modulator IC intended for use in high-speed, high-efficiency switch mode power supplies. It provides all the functions necessary to implement a single-switch current mode PWM, in any topology, with a minimum of external parts.

Because the HV9112 utilizes Supertex's proprietary BiCMOS/DMOS technology, it requires less than one tenth of the operating power of conventional bipolar PWM ICs, and can operate at more than twice their switching frequency. The dynamic range for regulation is also increased, to approximately 8 times that of similar bipolar parts. It starts directly from any DC input voltage between 10 and 120VDC, requiring no external power resistor. The output stage is push-pull CMOS and thus requires no clamping diodes for protection, even when significant lead length exists between the output and the external MOSFET. The clock frequency is set with a single external resistor.

Accessory functions are included to permit fast remote shutdown (latching or nonlatching) and under voltage shutdown.

For similar ICs intended to operate directly from up to 450VDC input, please consult the data sheets for the HV9120 and HV9123.

For detailed circuit and application information, please refer to application notes AN-H13 and AN-H21 to AN-H24.

Ordering Information

Device	Package Option
	14-Lead Narrow Body SOIC (NG)
HV9112	HV9112NG-G

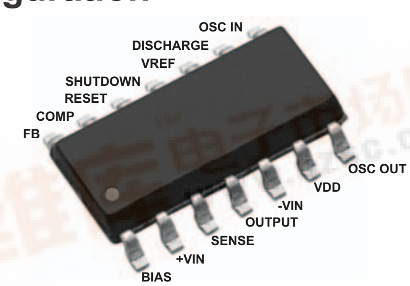
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Input voltage, V_{IN}	80V
Logic voltage, V_{DD}	15.5V
Logic linear input, FB and sense input voltage	-0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C
Power dissipation	750mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



14-Lead Narrow Body SOIC (NG)

Product Marking

Top Marking

HV9112NG
YWW LLLLLLLL

Bottom Marking

CCCCCCCCC AAA

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
—— = "Green" Packaging

**May be part of top marking*

14-Lead Narrow Body SOIC (NG)

Electrical Characteristics

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

Sym	Parameter	#	Min	Typ	Max	Units	Conditions
Reference							
V_{REF}	Output voltage	-	3.88	4.00	4.12	V	R_L = 10MΩ
Z_{OUT}	Output impedence	#	15	30	45	KΩ	---
I_{SHORT}	Short circuit current	-	-	125	250	µA	$V_{REF} = -V_{IN}$
ΔV_{REF}	Change in V_{REF} with temperature	#	-	0.25	-	mV/°C	T_A = -55°C to 125°C
Oscillator							
f_{MAX}	Oscillator frequency	-	1.0	3.0	-	MHz	R_{OSC} = 1.0MΩ
f_{OSC}	Initial accuracy[(1)]	-	80	100	120	KHz	R_{OSC} = 330KΩ
		-	160	200	240		R_{OSC} = 150KΩ
-	Voltage stability	-	-	-	15	%	V_{SYNC} = 0.1V
-	Temperature coefficient	#	-	170	-	ppm/°C	T_A = -55°C to 125°C
PWM							
D_{MAX}	Maximum duty cycle	-	49.0	49.4	49.6	%	---
D_{MIN}	Deadtime	#	-	-	-	ns	---
	Minimum duty cycle	-	-	-	0	%	---
	Maximum pulse width before pulse drops out	#	-	80	125	ns	---
Current Limit							
	Maximum input signal	-	1.0	1.2	1.4	V	V_{FB} = 0V
t_D	Delay to output	#	-	80	120	ns	V_{SENSE} = 1.5V, V_{COMP} ≤ 2.0V
Error Amplifier							
V_{FB}	Feedback voltage	-	3.92	4.00	4.08	V	V_{FB} shorted to comp
I_{IN}	Input bias current	-	-	25	500	nA	V_{FB} = 4.0V
V_{OS}	Input offset voltage	-	nulled during trim			-	---
A_{VOL}	Open loop voltage gain	#	60	80	-	dB	---
GB	Unity gain bandwidth	#	1.0	1.3	-	MHz	---
Z_{OUT}	Out impedance	#	see Fig. 1			Ω	---
I_{SOURCE}	Output source current	-	-1.4	-2.0	-	mA	V_{FB} = 3.4V
I_{SINK}	Output sink current	-	0.12	0.15	-	mA	V_{FB} = 4.5V
PSRR	Power supply rejection	#	see Fig. 2			dB	---

Notes:

 # Guaranteed by design. Not subject to production test.

(1) Stray capacitance on OSC In pin must be ≤5pF.

Electrical Characteristics *(cont.)*

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

Sym	Parameter		#	Min	Typ	Max	Units	Conditions
Pre-regulator/Startup								
$+V_{IN}$	Input voltage		-	9.0	-	80	V	I_{IN} < 10µA; V_{CC} > 9.4V
$+_{IIN}$	Input leakage current		-	-	-	10	µA	V_{DD} > 9.4V
V_{TH}	Vdd pre-regulator turn-off threshold voltage		-	8.0	8.7	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage lockout		-	7.0	8.1	8.9	V	---
Supply								
I_{DD}	Supply current		-	-	0.75	1.0	mA	C_L < 75pF
I_Q	Quiescent supply current		-	-	0.55	-	mA	Shutdown = $-V_{IN}$
I_{BIAS}	Nominal Bias current		-	-	20	-	µA	---
V_{DD}	Operating range		-	9.0	-	13.5	V	---
Shutdown Logic								
t_{SD}	Shutdown delay		#	-	50	100	ns	C_L = 500pF, V_{SENSE} = $-V_{IN}$
t_{SW}	Shutdown pulse width		#	50	-	-	ns	
t_{RW}	RESET pulse width		#	50	-	-	ns	---
t_{LW}	Latching pulse width		#	25	-	-	ns	Shutdown and reset low
V_{IL}	Input low voltage		-	-	-	2.0	V	---
V_{IH}	Input high voltage		-	7.0	-	-	V	---
I_{IH}	Input current, input high voltage		-	-	1.0	5.0	µA	V_{IN} = V_{DD}
I_{IL}	Input current, input low voltage		-	-	-25	-35	µA	V_{IN} = 0V
Output								
V_{OH}	Output high voltage		-	V_{DD} - 0.3	-	-	V	I_{OUT} = 10mA,
V_{OL}	Output low voltage		-	-	-	0.2	V	I_{OUT} = -10mA
R_{OUT}	Output resistance	Pull up	-	-	15	25	Ω	I_{OUT} = ±10mA
		Pull down	-	-	8.0	20	Ω	
		Pull up	-	-	20	30	Ω	I_{OUT} = ±10mA, T_A = -55°C to 125°C
		Pull down	-	-	10	30	Ω	
t_R	Rise time		#	-	30	75	ns	C_L = 500pF
t_F	Fall time		#	-	20	75	ns	C_L = 500pF

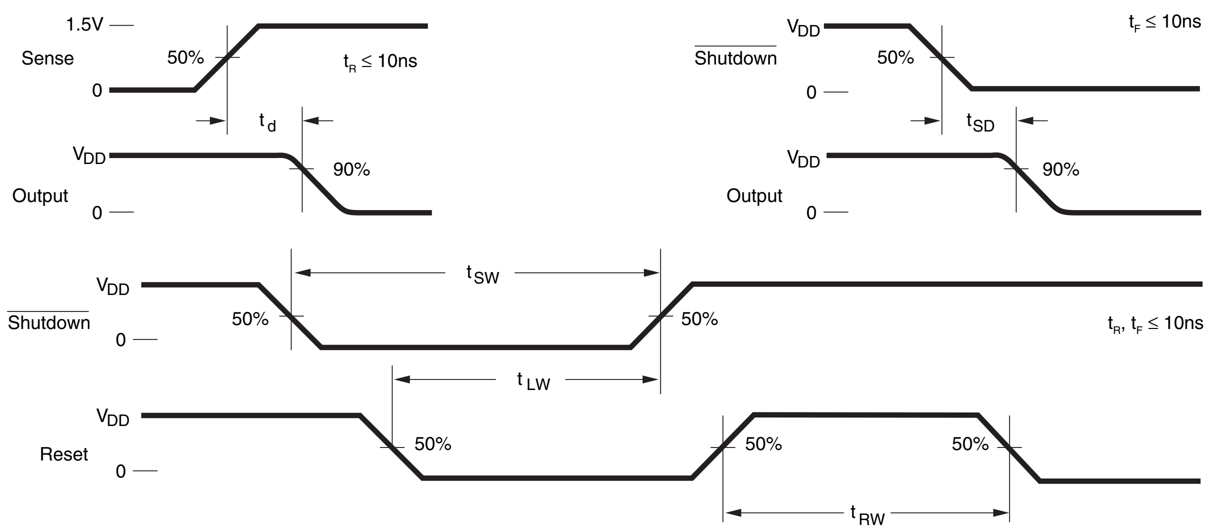
Notes:

Guaranteed by design. Not subject to production test.

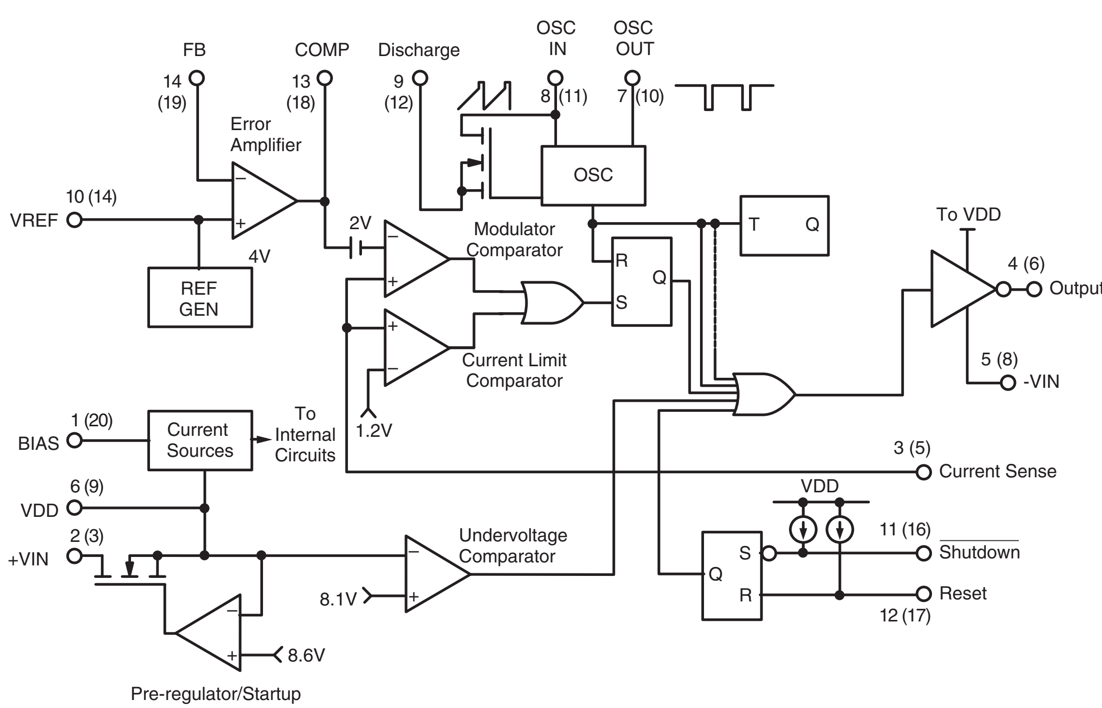
Truth Table

Shutdown	Reset	Output
H	H	Normal operation
H	H → L	Normal operation, no change
L	H	Off, not latched
L	L	Off, latched
L → H	L	Off, latched, no change

Shutdown Timing Waveforms



Functional Block Diagram



Typical Performance Curves

Fig. 1

Error Amplifier Output Impedance (Z_0)

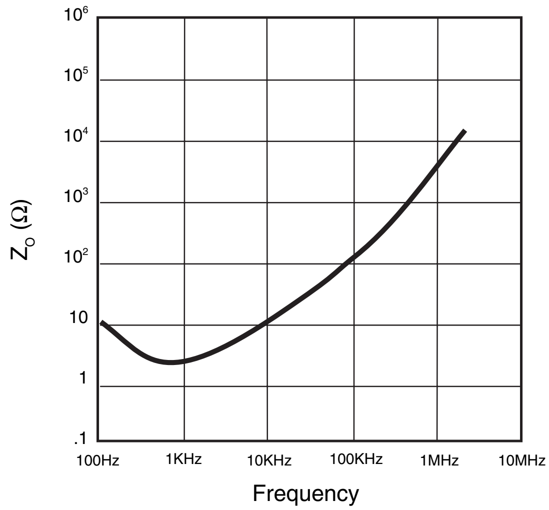


Fig. 4

Output Switching Frequency vs. Oscillator Resistance

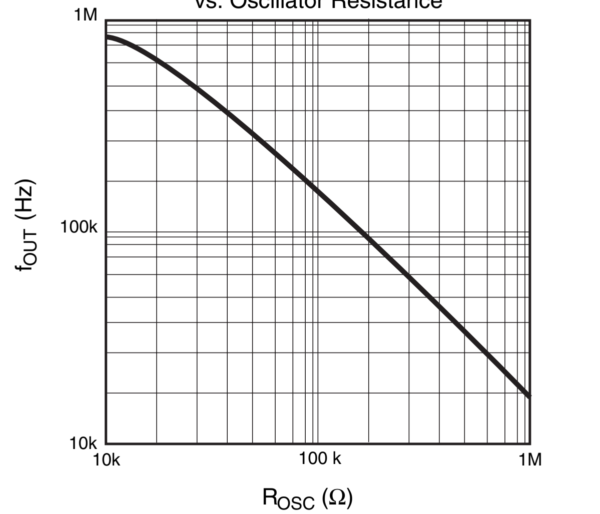


Fig. 2

PSRR — Error Amplifier and Reference

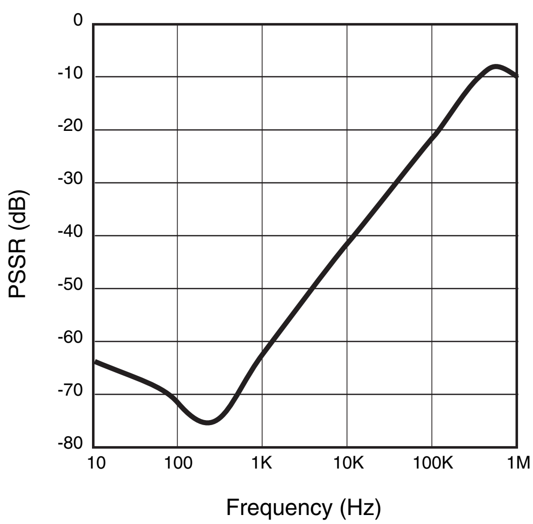


Fig. 5

Error Amplifier Open Loop Gain/Phase

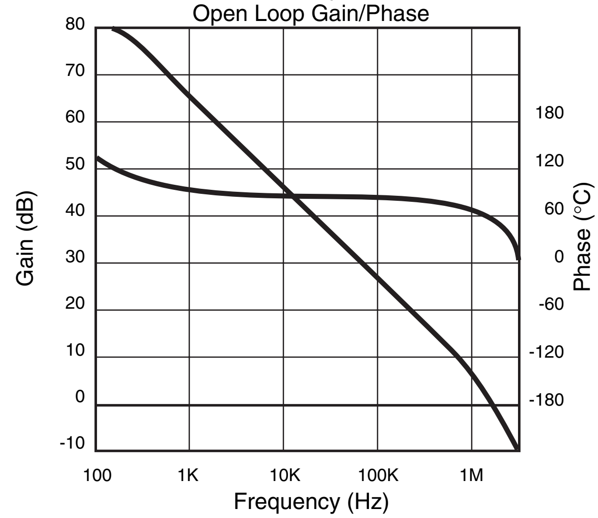


Fig. 3

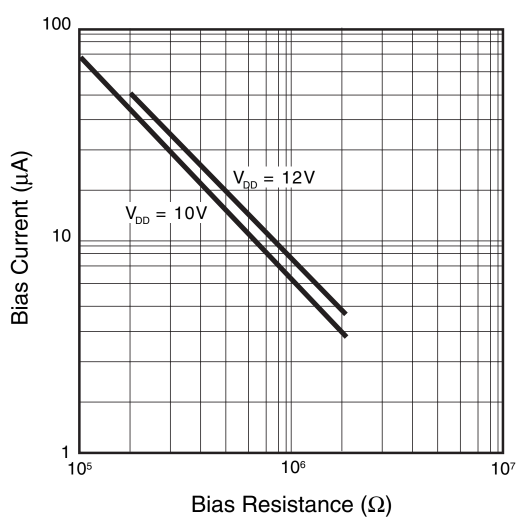
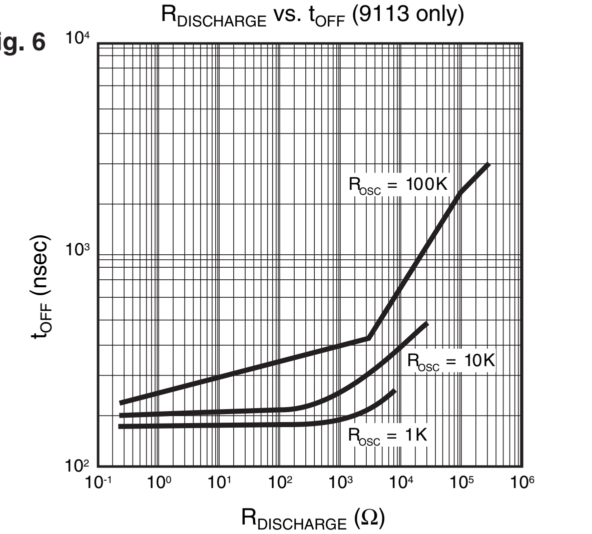


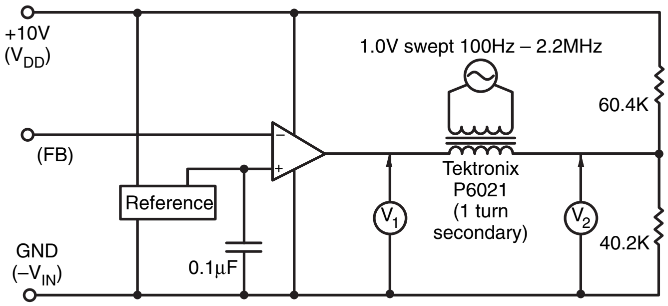
Fig. 6

$R_{DISCHARGE}$ vs. t_{OFF} (9113 only)



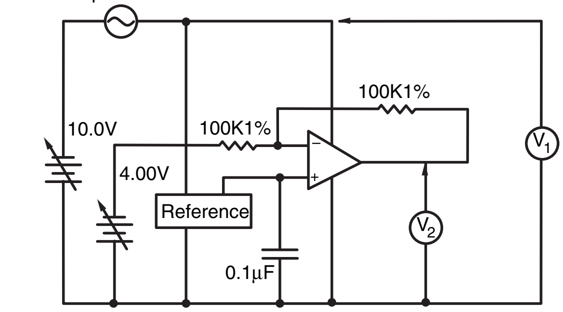
Test Circuits

Error Amp Z_{OUT}



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm$ 1mV before connecting transformer

PSRR



Detailed Description

Preregulator

The preregulator/startup circuit for the HV9112 consists of a high-voltage n-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the VIN terminal and the VDD terminal. The maximum current (about 20 mA) occurs when V_{DD} = 0, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source(generally the supply the chip is controlling). No current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between VDD and VSS is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the VDD supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the effective gate capacitance of the MOSFET being driven, i.e.,

$C_{STORAGE} \geq$ 100 x (gate charge of FET at 10V ÷ 10V)

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytic capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the under voltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the under voltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the under voltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the BIAS pin and VSS is required by the HV9112 to set currents in a series of current mirrors used by the analog sections of the chip. The nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510kΩ to 680KΩ resistor if V_{DD} will be 12V. A precision resistor is not required; ± 5% is fine.

Clock Oscillator

The clock oscillator of the HV9112 consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC IN and OSC OUT is required to set the oscillator frequency (see graph). For the 50% maximum duty cycle versions the Discharge pin is internally connected to GND. For the 99% duty cycle version, the Discharge pin can either be connected to VSS directly or connected to VSS through a resistor used to set a deadtime. One major difference exists between the Supertex HV9112 and competitive 9110's. On the Supertex part, the oscillator is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in the construction of power supplies that meet CCITT specification I-430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The Reference of the HV9112 consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier, when connected in a gain of –1 configuration, is as close to 4.0V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4.0V, the feedback voltage required for proper regulation will be.

A ≈ 50KΩ resistor is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low impedance voltage source ≤6.0V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. Because the reference of the HV9112 is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and VSS is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Error Amplifier

The error amplifier in the HV9112 is a true low-power differential input operational amplifier intended for around the amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity gain stable.

Current Sense Comparators

The HV9112 uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

Remote Shutdown

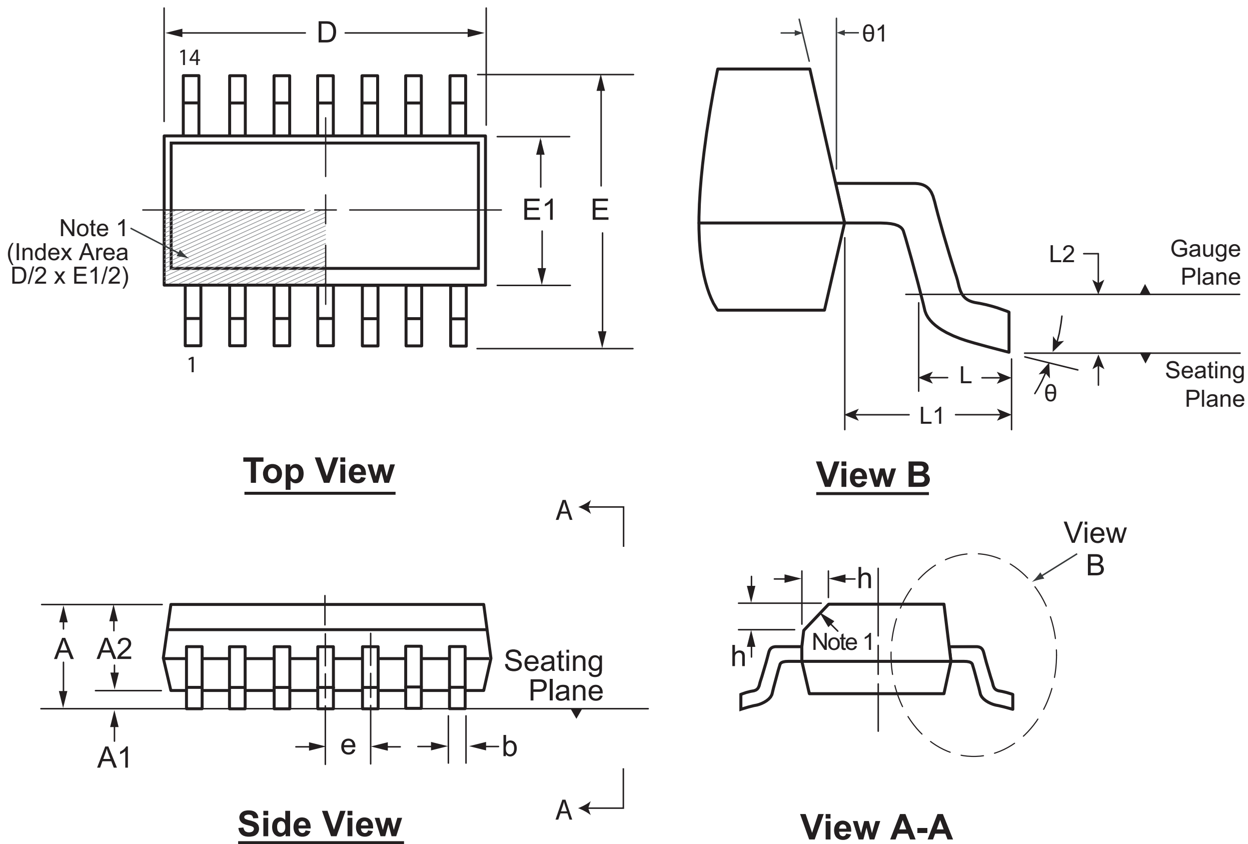
The shutdown and reset pins of the 9110 can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open drain logic. When not used they should be left open, or connected to VDD.

Output Buffer

The output buffer of the HV9112 is of standard CMOS construction (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

14-Lead SOIC (Narrow Body) Package Outline (NG)

8.65x3.90mm body, 1.27mm pitch



Note 1:
This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35	0.10	1.25	0.31	8.55	5.80	3.80	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	8.65	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65	0.51	8.75	6.20	4.00		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AB, Issue E, Sept. 2005.
Drawinngs not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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