



0.5 OHM, DUAL SPDT ANALOG SWITCH

IDTAS4684

Description

The IDTAS4684 low on-resistance (R_{ON}), low voltage, dual single-pole/double-throw (SPDT) analog switch operates from a single +1.8 V to +5.5 V supply. The IDTAS4684 features a 0.5Ω (max) R_{ON} for its NC switch and a 0.8Ω (max) R_{ON} for its NO switch at a +2.7 V supply. It also features break-before-make switching action (2 ns) with $t_{ON} = 50$ ns and $t_{OFF} = 40$ ns at +3 V. The digital logic inputs are 1.8 V logic-compatible with a +2.7 V to +3.3 V supply. Comes in 3 x 3 DFN, or 12-bump CSP packages.

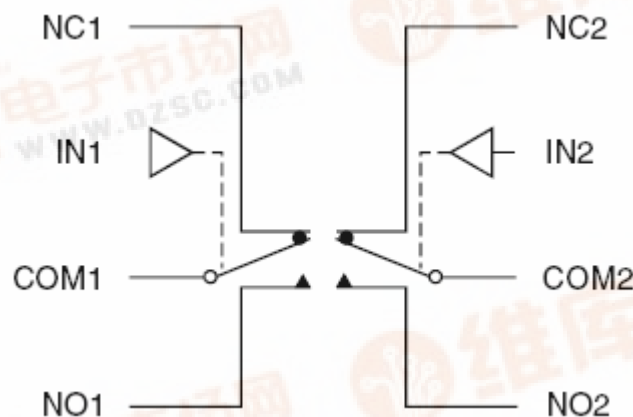
Applications

- Speaker headset switching
- MP3 players
- Battery-operated equipment
- Audio and video signal routing
- PCMCIA cards
- Cellular phones
- Modems

Features

- +1.8 V to +5.5 V single-supply operation
- Rail-to-rail signal handling
- 1.8 V logic compatibility
- R_{ON} match between channels: 0.06Ω (max)
- R_{ON} flatness over signal range: 0.15Ω (max)
- NCx Switch R_{ON} : 0.5Ω max (+2.7 V Supply) (ICSAS4684)
- NOx Switch R_{ON} : 0.8Ω max (+2.7 V Supply)
- Low crosstalk: -68dB (100 kHz)
- High Off-isolation: -64dB (100 kHz)
- THD: 0.03%
- 50 nA (max) supply current
- Low leakage currents: 1 nA (max) at $T_A = +25^\circ\text{C}$
- 12-bump, 0.5 mm-Pitch UCSP
- Available in 10-pin DFN and CSP packages

Block Diagram



Pin Assignment (DFN)

V+	1	10	NO2
NO1	2	9	COM2
COM1	3	8	IN2
IN1	4	7	NC2
NC1	5	6	GND

Pin Assignment (CSP)

	A	B	C
1	NC1	GND	NC2
2	IN1	NC	IN2
3	COM1	NC	COM2
4	NO1	V+	NO2

Truth Table

IN	NO	NC
0	OFF	ON
1	ON	OFF

Note: Switches shown for logic “0” input.

Pin Descriptions

Pin Numbers		Pin Name	Pin Description
DFN	CSP		
1	B4	V+	Positive supply voltage input.
2	A4	NO1	Analog switch. Normally open terminal 1.
3	A3	COM1	Analog switch. Common terminal 1.
4	A2	IN1	Digital control input 1.
5	A1	NC1	Analog switch. Normally closed terminal 1.
6	B1	GND	Ground.
7	C1	NC2	Analog switch. Normally closed terminal 2.
8	C2	IN2	Digital control input 2.
9	C3	COM2	Analog switch. Common terminal 2.
10	C4	NO2	Analog switch. Normally open terminal 2.
—	B2	NC	No connect.
—	B3	NC	No connect.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDTAS4684. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range. All voltages referenced to ground.

Symbol	Rating	Min	Max	Unit
V+, IN		-0.3	+6	V
COM, NO, NC		-0.3	(V+ + 0.3)	V
NO, NC, COM	Continuous current		±300	mA
	Peak current (pulsed at 1ms, 50% duty cycle)		±400	
	Peak current (pulsed at 1ms, 10% duty cycle)		±500	
	Continuous power dissipation (TA = +70°C) and 12-bump UCSP (derate 11.4mW/°C above +70°C)		+909	mW
	Operating temperature range	0	+70	°C
TSTG	Storage temperature range	-65	+150	°C
	Lead temperature (soldering, 10s)		+300	°C
	Bump temperature (soldering, infrared, 15s)		+200	°C
	Vapor phase (60s)		+215	°C

Electrical Characteristics

Unless stated otherwise, $V_+ = 2.7\text{ V to }3.3\text{ V}$, $V_{IH} = 1.4\text{ V}$, $V_{IL} = 0.5\text{ V}$, $T_A = T_{MIN}\text{ to }T_{MAX}$. Typical values are at +3 V and 25°C

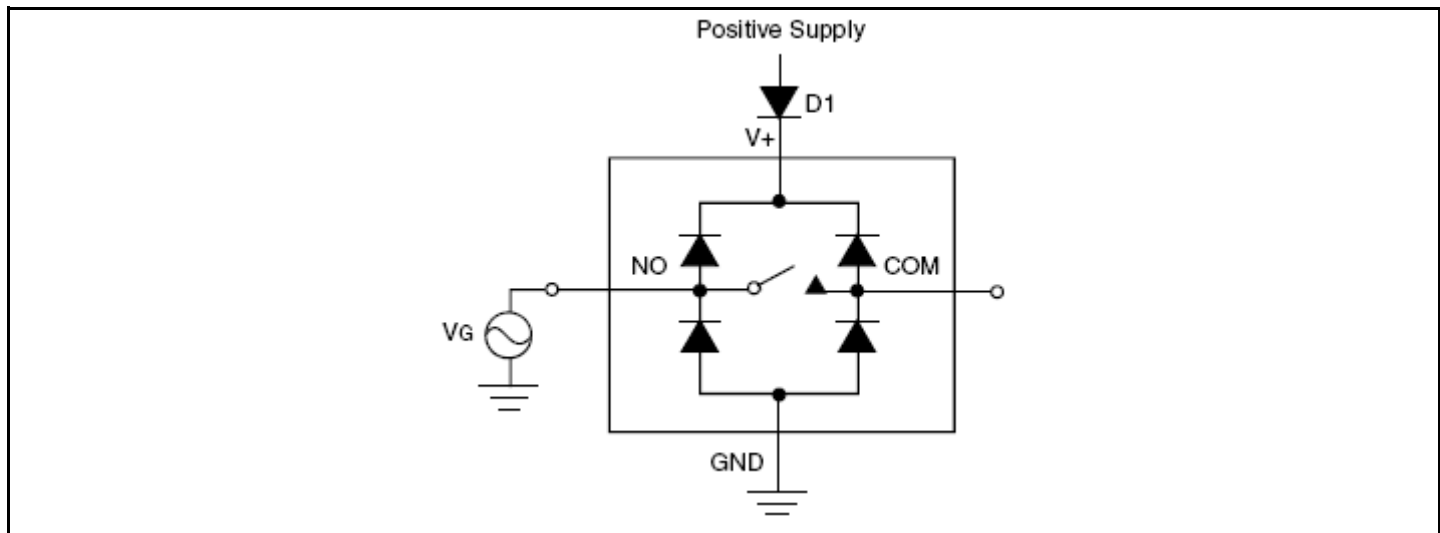
Parameter	Symbol	Conditions	T _A	Min.	Typ.	Max.	Units
Analog Switch							
Analog Signal Range	V _{NO} , V _{NC} , V _{COM}		T _{MIN} to T _{MAX}	0		V+	V
NC On-Resistance	R _{ON(NC)}	V+ = 2.7 V, I _{COM} = 100 mA, V _{NC} = 0 to V+; Note 3	+25°C		3.0	0.5	Ω
			T _{MIN} to T _{MAX}			0.5	
NO On-Resistance	R _{ON(NO)}	V+ = 2.7 V, I _{COM} = 100 mA, V _{NO} = 0 to V+; Note 3	+25°C		0.45	0.8	Ω
			T _{MIN} to T _{MAX}			0.8	
On-Resistance Match between channels	ΔR _{ON}	V+ = 2.7 V, I _{COM} = 100 mA, V _{NO} or V _{NC} = 1.5 V; Notes 3, 4	+25°C		0	0.6	Ω
			T _{MIN} to T _{MAX}			0.6	
NC On-Resistance Flatness	R _{FLAT(NC)}	V+ = 2.7 V, I _{COM} = 100 mA, V _{NC} = 0 to V+; Note 5	T _{MIN} to T _{MAX}			0.15	Ω
NO On-Resistance Flatness	R _{FLAT(NO)}	V+ = 2.7 V, I _{COM} = 100 mA, V _{NO} = 0 to V+; Note 5	T _{MIN} to T _{MAX}			0.35	Ω
NO or NC Off-leakage Current	I _{NO} (OFF) or I _{NC} (OFF)	V+ = 3.3 V, V _{NO} or V _{NC} = 3 V, 0.3 V V _{COM} = 0.3 V, 3 V	+25°C	-1		+1	nA
			T _{MIN} to T _{MAX}	-10		+10	
COM On-leakage Current	I _{COM} (ON)	V+ = 3.3 V, V _{NO} or V _{NC} = 3 V, 0.3 V, or floating V _{COM} = 0.3 V, 3 V, or floating	+25°C	-2		+2	nA
			T _{MIN} to T _{MAX}	-20		+20	
Dynamic Characteristics							
Turn-on Time	t _{ON}	V+ = 2.7 V, V _{NO} or V _{NC} = 1.5 V, R _L = 50Ω, C _L = 35 pF	+25°C		30	50	ns
			T _{MIN} to T _{MAX}			60	ns
Turn-off Time	t _{OFF}	V+ = 2.7 V, V _{NO} or V _{NC} = 1.5 V, R _L = 50Ω, C _L = 35 pF	+25°C		25	30	ns
			T _{MIN} to T _{MAX}			40	ns
Break-Before-Make-Delay	t _{BBM}	V+ = 2.7 V, V _{NO} or V _{NC} = 1.5 V, R _L = 50Ω, C _L = 35 pF	T _{MIN} to T _{MAX}	2	15		ns
Charge Injection	Q	COM = 0, RS = 0, C _L = 1 nF	+25°C		200		pC
Off-Isolation	V _{ISO}	C _L = 5 pF; R _L = 50Ω, f = 100 kHz, V _{COM} = 1 V _{RMS} , Note 6	+25°C		-64		dB
Crosstalk	V _{CT}	f = 100 kHz, R _L = 50Ω, C _L = 5 pF, V _{COM} = 1 V _{RMS}	+25°C		-68		dB
Total Harmonic Distortion	THD	R _L = 600Ω, IN = 2 V p-p, f = 20Hz to 20 kHz	+25°C		0.03		%
NC Off-Capacitance	C _{NC} (OFF)	f = 1 MHz	+25°C		84		pF
NC Off-Capacitance	C _{NO} (OFF)	f = 1 MHz	+25°C		37		pF
NC On-Capacitance	C _{NC} (ON)	f = 1 MHz	+25°C		190		pF
NC On-Capacitance	C _{NO} (ON)	f = 1 MHz	+25°C		150		pF

Parameter	Symbol	Conditions	T _A	Min.	Typ.	Max.	Units
Digital I/O							
Input Logic HIGH	V _{IH}		T _{MIN} to T _{MAX}	1.4			V
Input Logic LOW	V _{IL}		T _{MIN} to T _{MAX}			0.5	V
IN Input Leakage Current	I _{IN}	V _{IN} = 0 or V+	T _{MIN} to T _{MAX}	-1		1	μA
Power Supply							
Power Supply Range	V+		T _{MIN} to T _{MAX}	1.8		5.5	V
Supply Current	I+	V+ = 5.5 V, V _{IN} = 0 or V+, Note 3	+25°C	-50	+0.04	+50	nA
			T _{MIN} to T _{MAX}	-200		+200	

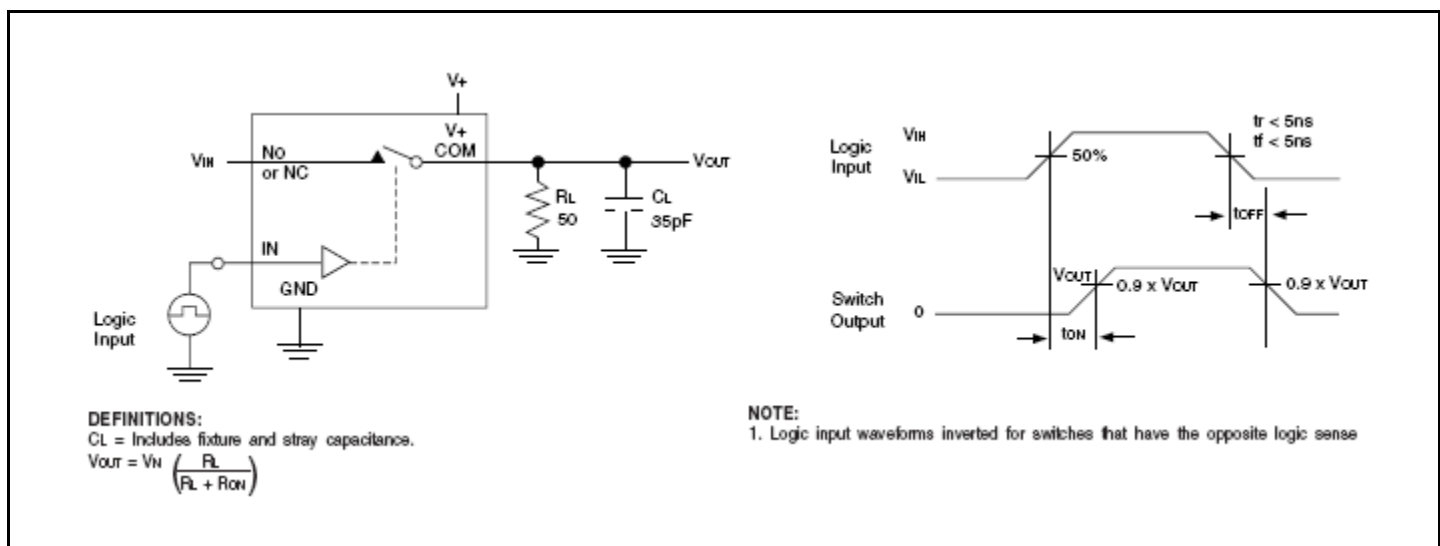
Notes:

1. The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value a maximum.
2. UCSP parts are 100% tested at +25°C only and guaranteed by design and correlation at the full hot-rated temperature.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$, between NC1 and NC2 or between NO1 and NO2.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal ranges.
6. Off-isolation = $20\log_{10}(V_{COM} / V_{CO})$, V_{COM} = output, V_{CO} = input to off switch.

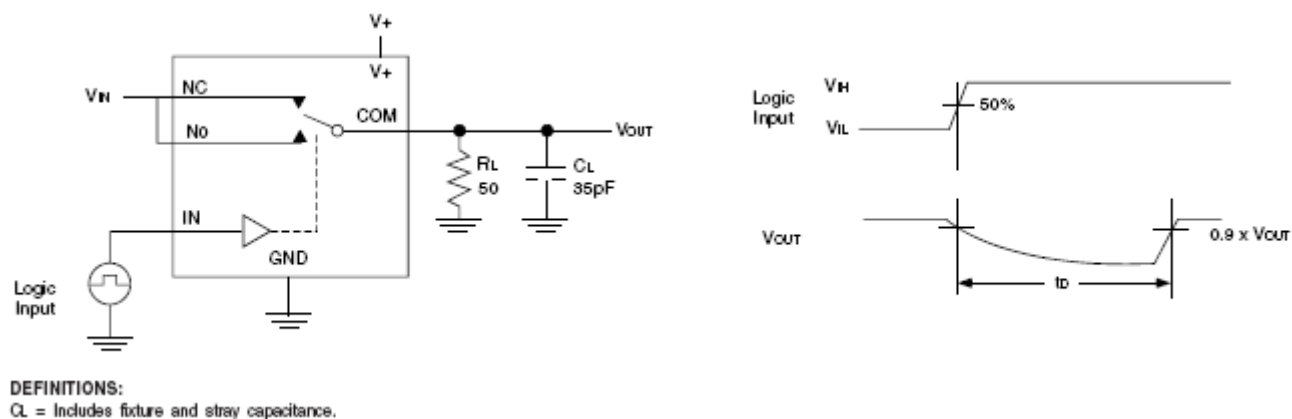
Test Circuits and Timing Diagrams



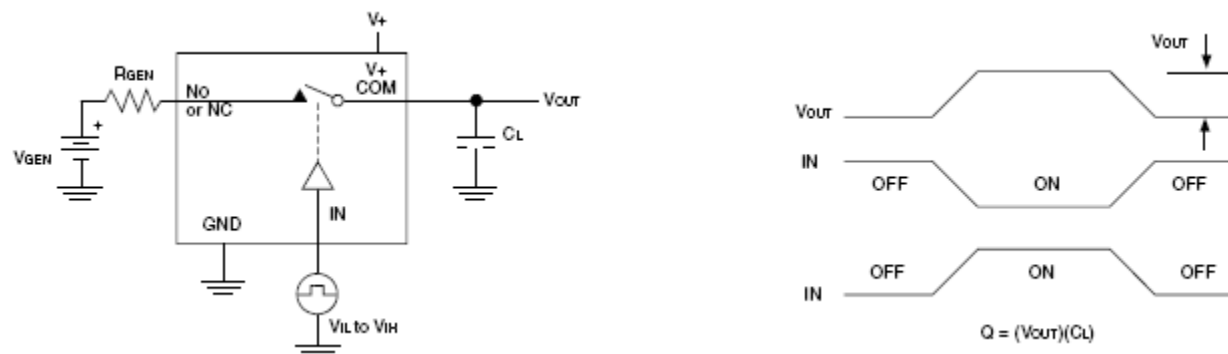
Overvoltage Protection Using Two External Blocking Diodes



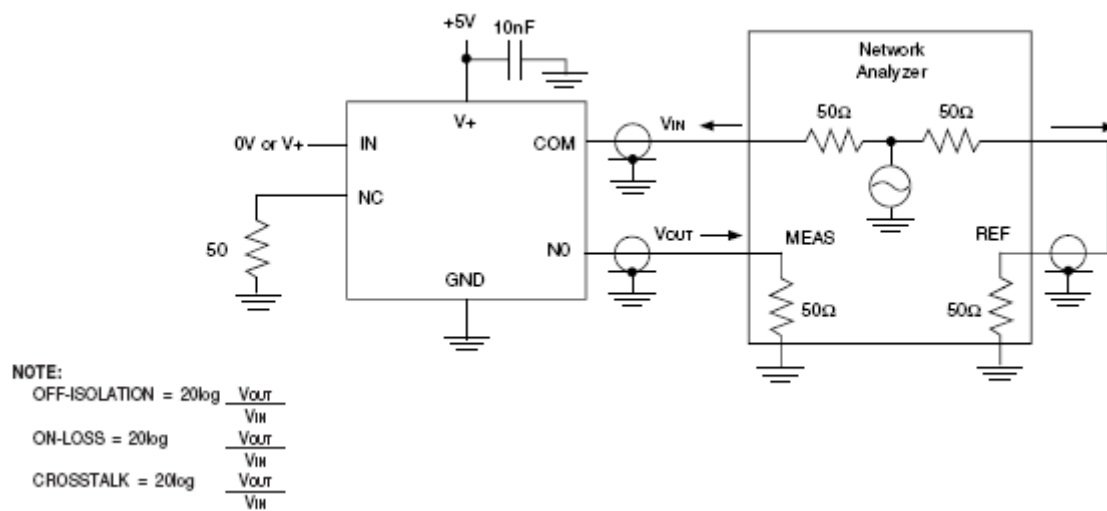
Switching Time



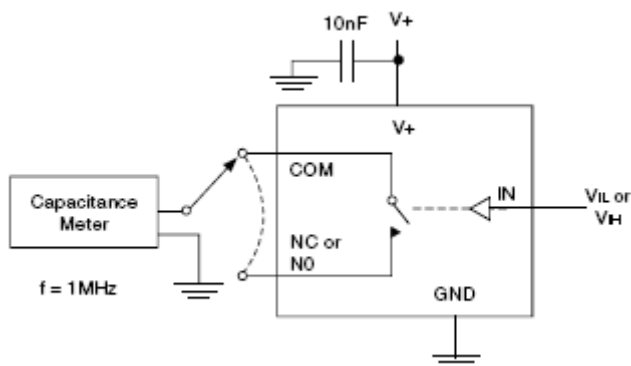
Break-Before-Make Interval



Charge Injection

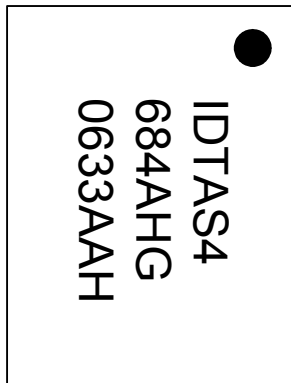


On-Loss, Off-Isolation, and Crosstalk

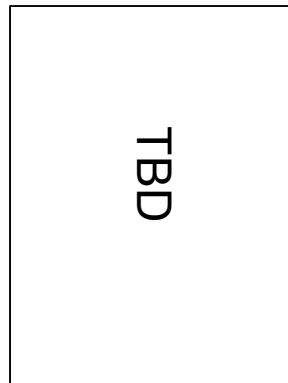


Channel Off/On Capacitance

Marking Diagram (CSP)



Marking Diagram (DFN)

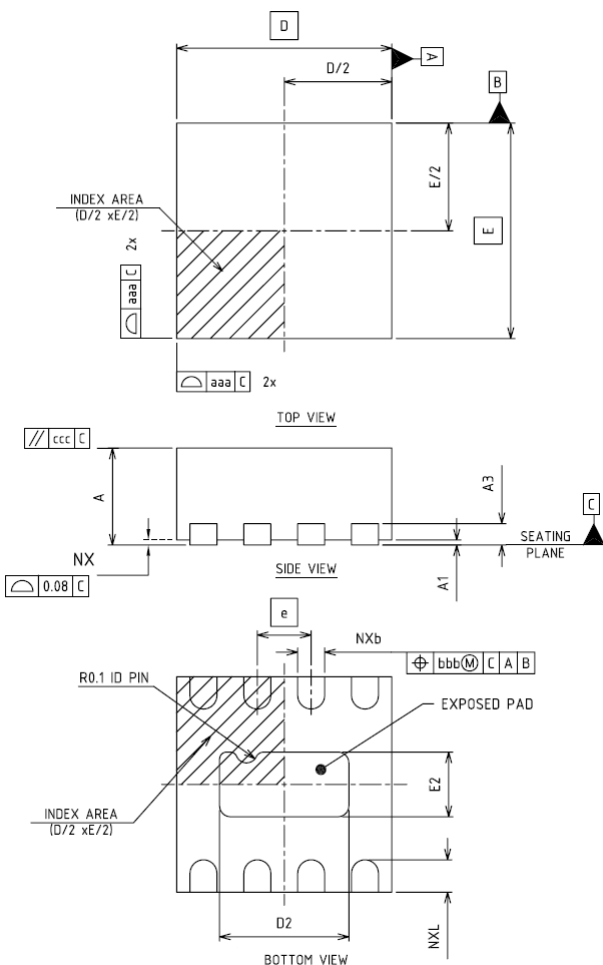


Notes:

1. "Z" is the device step (1 to 2 characters).
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "\$" is the assembly mark code.
4. "G" after the two-letter package code designates RoHS compliant package.
5. "I" at the end of part number indicates industrial temperature range.
6. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (10-pin DFN 3x3mm)

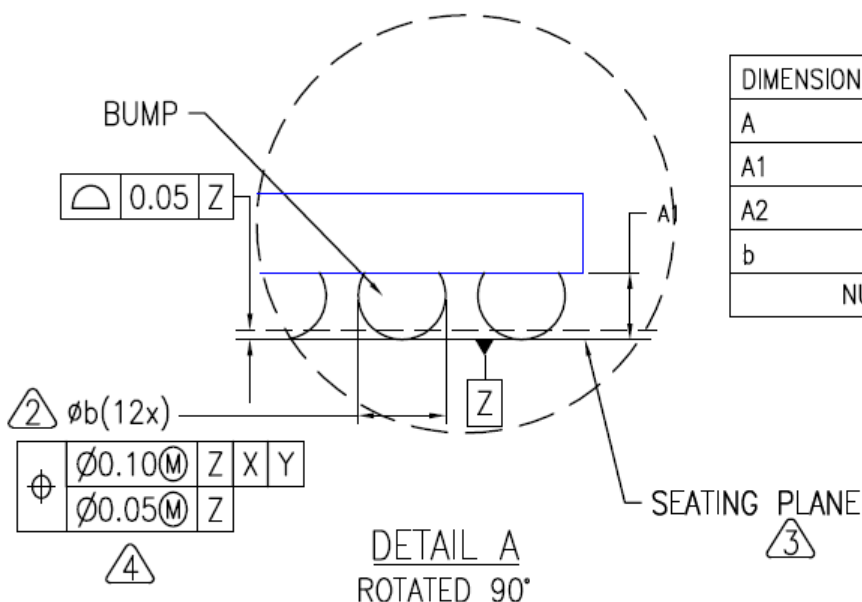
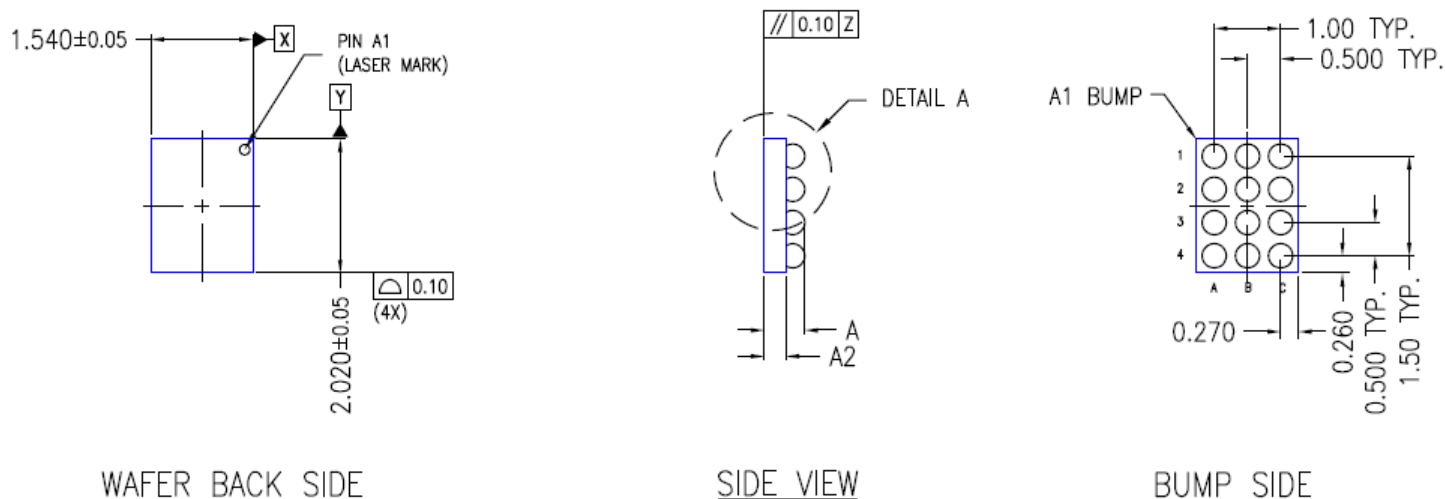
Package dimensions are kept current with JEDEC Publication No. 95,



Symbol	Millimeters	
	Min	Max
A	0.80	1.00
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.30
N	10	
N _D	5	
N _E	0	
D	3.00 BASIC	
E	3.00 BASIC	
e	0.50 BASIC	
D2	2.20	2.70
E2	1.40	1.75
L	0.30	0.50
aaa	0.15	
bbb	0.10	
ccc	0.10	

Package Outline and Package Dimensions (12-bump CSP)

Package dimensions are kept current with JESD Publication No. 95-1,



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.555	0.61	0.665
A1	0.25	0.28	0.31
A2	0.305	0.33	0.355
b	0.316	0.366	0.416
NUMBER OF BUMPS 12			

NOTES:

1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M – 1994.

2. DIMENSION IS MEASURED AT THE MAXIMUM BUMP DIAMETER PARALLEL TO PRIMARY DATUM Z

3. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BUMP.

4. BUMP POSITION DESIGNATION PER JESD 95-1, SPP-010.

5. THERE SHALL BE A MINIMUM CLEARANCE OF 0.10mm BETWEEN THE EDGE OF THE BUMP AND THE BODY EDGE.

Ordering Information

IDT	XXXXXX Device Type	XXX Package	X Temp. Range	X Shipping Carrier	
				8 Blank	Tape and Reel Tray
				Blank	Commercial (0 to +70°C)
				AHG NBG	Chip Scale Package 3mm x 3mm DFN
				AS4684	0.5Ω Low Voltage, Dual SPDT Analog Switch

Revision History

Rev.	Originator	Date	Description of Change
B		10/31/06	created datasheet in new template; added marking diagram.

IDTAS4684

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ANALOG SWITCH

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