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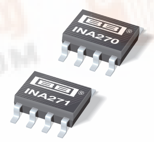


INA270
INA271

SBOS381A–FEBRUARY 2007–REVISED APRIL 2007

Voltage Output, Unidirectional Measurement Current-Shunt Monitor

FEATURES

- WIDE COMMON-MODE RANGE: –16V to +80V
- CMRR: 120dB
- ACCURACY:
  ±2.5mV offset (max)
  ±1% gain error (max)
  20µV/°C offset drift (max)
  55ppm/°C gain drift (max)
- BANDWIDTH: Up to 130kHz
- TWO TRANSFER FUNCTIONS AVAILABLE:
  14V/V (INA270)
  20V/V (INA271)
- QUIESCENT CURRENT: 900µA (max)
- POWER SUPPLY: +2.7V to +18V
- PROVISION FOR FILTERING

APPLICATIONS

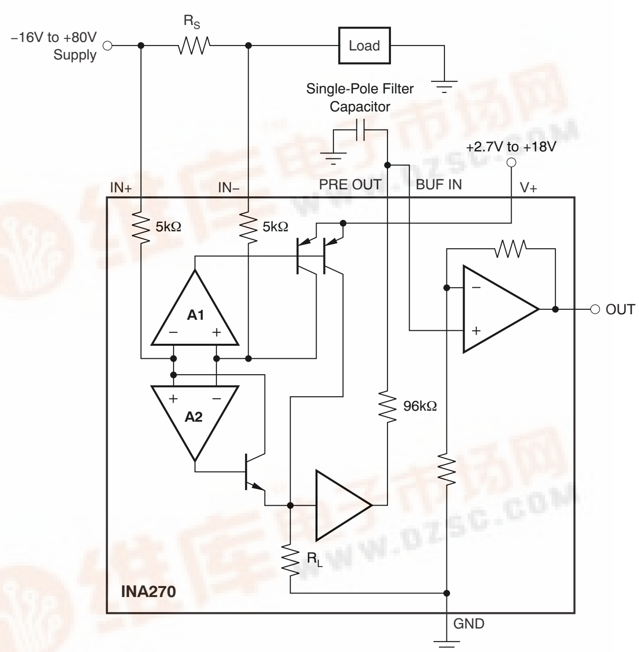
- POWER MANAGEMENT
- AUTOMOTIVE
- TELECOM EQUIPMENT
- NOTEBOOK COMPUTERS
- BATTERY CHARGERS
- CELL PHONES
- WELDING EQUIPMENT

DESCRIPTION

The INA270 and INA271 family of current-shunt monitors with voltage output can sense drops across current shunts at common-mode voltages from –16V to +80V, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two output voltage scales: 14V/V and 20V/V. The 130kHz bandwidth simplifies use in current-control loops.

The INA270 and INA271 operate from a single +2.7V to +18V supply, drawing a maximum of 900µA of supply current. They are specified over the extended operating temperature range of –40°C to +125°C and are offered in an SO-8 package.



DEVICE COMPARISON

DEVICE	GAIN
INA270	14V/V
INA271	20V/V

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	GAIN	PACKAGE MARKING
INA270	SO-8	D	14	I270A
INA271	SO-8	D	20	I271A

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

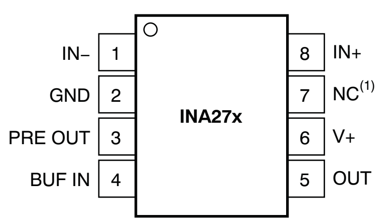
ABSOLUTE MAXIMUM RATINGS(1)

	INA270, INA271	UNIT
Supply Voltage (V_S)	+18	V
Analog Inputs, V_{IN+}, $V_{IN–}$:		
Differential, (V_{IN+}) – ($V_{IN–}$)	–18 to +18	V
Common-Mode	–16 to +80	V
Analog Output:		
OUT and PRE OUT Pins	GND – 0.3 to (V+) + 0.3	V
Input Current Into Any Pin	5	mA
Operating Temperature	–55 to +150	°C
Storage Temperature	–65 to +150	°C
Junction Temperature	+150	°C
ESD Ratings:		
Human Body Model	3000	V
Charged-Device Model	750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

PIN CONFIGURATION

SO-8
Top View



NOTE (1): NC denotes no internal connection.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +5V, V_{CM} = +12V, V_{SENSE} = 100mV, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		CONDITIONS	INA270, INA271			UNIT
			MIN	TYP	MAX	
INPUT						
Full-Scale Input Voltage	V_{SENSE}	$V_{SENSE} = (V_{IN+}) + (V_{IN–})$		0.15	$(V_S – 0.2)$/Gain	V
Common-Mode Input Range	**V_{CM}**		**–16**		**+80**	**V**
Common-Mode Rejection Ratio	CMRR	V_{IN+} = –16V to +80V	80	120		dB
Over Temperature		**V_{IN+} = +12V to +80V**	**100**	**120**		**dB**
Offset Voltage, RTI(1)	V_{OS}			±0.5	2.5	mV
Over Temperature					**±3**	**mV**
vs Temperature	**dV_{OS}/dT**			**2.5**	**20**	**µV/°C**
vs Power-Supply	**PSR**	**V_S = +2.7V to +18V, V_{CM} = +18V**		**5**	**100**	**µV/V**
Input Bias Current, $V_{IN–}$ Pin	**I_B**			**±8**	**±16**	**µA**
PRE OUT Output Impedance(2)				96		kΩ
Buffer Input Bias Current				–50		nA
Buffer Input Bias Current Temperature Coefficient				±0.03		nA/°C
OUTPUT (V_{SENSE} ≥ 20mV)(3)						
Gain: INA270 Total Gain	G			14		V/V
Gain: INA271 Total Gain	G			20		V/V
Output Buffer Gain	G_{BUF}			2		V/V
Total Gain Error		V_{SENSE} = 20mV to 100mV		±0.2	±1	%
Over Temperature					**±2**	**%**
vs Temperature					**50**	**ppm/°C**
Total Output Error(4)		V_{SENSE} = 20mV to 100mV		±0.75	±2.2	%
Total Output Error				**±1.0**	**±3.0**	**%**
Nonlinearity Error		V_{SENSE} = 20mV to 100mV		±0.002		%
Output Impedance, Pin 5	R_O			1.5		Ω
Maximum Capacitive Load		No Sustained Oscillation		10		nF
VOLTAGE OUTPUT(5)		**R_L = 10kΩ to GND**				
Swing to V+ Power-Supply Rail				**(V+) – 0.05**	**(V+) – 0.2**	**V**
Swing to GND(6)				**V_{GND} + 0.003**	**V_{GND} + 0.05**	**V**
FREQUENCY RESPONSE						
Bandwidth	BW	C_{LOAD} = 5pF		130		kHz
Phase Margin		C_{LOAD} < 10nF		40		degrees
Slew Rate	SR			1		V/µs
Settling Time (1%)	t_S	V_{SENSE} = 10mV to 100mV_{PP}, C_{LOAD} = 5pF		2		µs

(1) RTI means *Referred-to-Input*.
(2) Initial resistor variation is ±30% with an additional –2200ppm/°C temperature coefficient.
(3) For output behavior when V_{SENSE} < 20mV, see the Application Information section *Accuracy Variations as A Result of V_{SENSE} and Common-Mode Voltage*.
(4) Total output error includes effects of gain error and V_{OS}.
(5) See typical characteristic curve *Output Swing vs Output Current* and Application Information section *Accuracy Variations as A Result of V_{SENSE} and Common-Mode Voltage*.
(6) Ensured by design; not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +5V, V_{CM} = +12V, V_{SENSE} = 100mV, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		CONDITIONS	INA270, INA271			UNIT
			MIN	TYP	MAX	
NOISE, RTI(7)						
Voltage Noise Density	e_n			40		nV/√Hz
POWER SUPPLY						
Operating Range	**V_S**		**+2.7**		**+18**	**V**
Quiescent Current	I_Q	V_{OUT} = 2V		700	900	μA
Over Temperature		**V_{SENSE} = 0mV**		**350**	**950**	**μA**
TEMPERATURE RANGE						
Specified Temperature Range			–40		+125	°C
Operating Temperature Range			–55		+150	°C
Thermal Resistance	θ_{JA}					
SO-8				+150		°C/W

(7) RTI means *Referred-to-Input*.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +12V, V_{CM} = 12V, and V_{SENSE} = 100mV, unless otherwise noted.

GAIN vs FREQUENCY

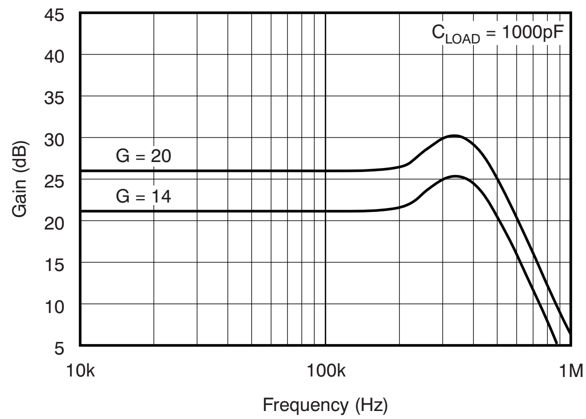


Figure 1.

GAIN vs FREQUENCY

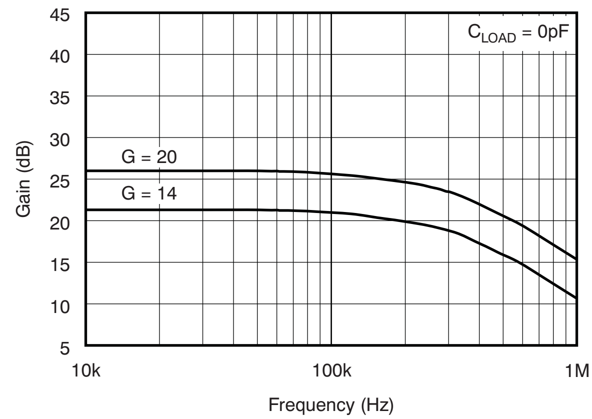


Figure 2.

GAIN PLOT

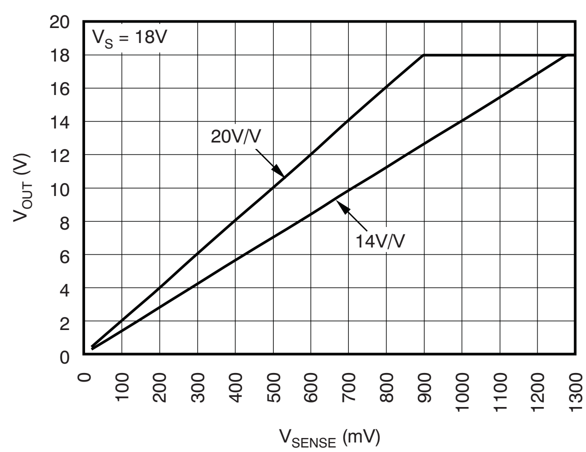


Figure 3.

COMMON-MODE AND POWER-SUPPLY REJECTION vs FREQUENCY

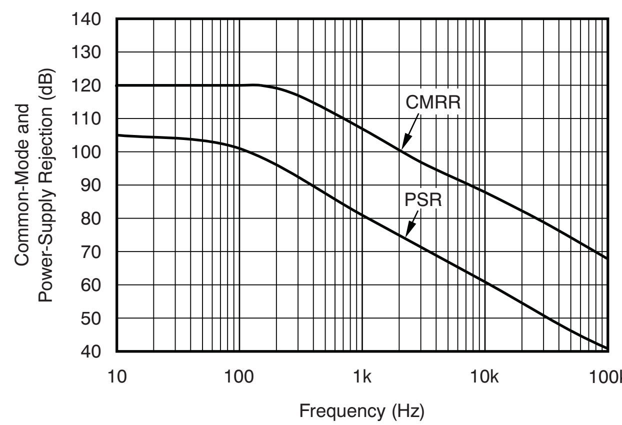


Figure 4.

TOTAL OUTPUT ERROR vs V_{SENSE}

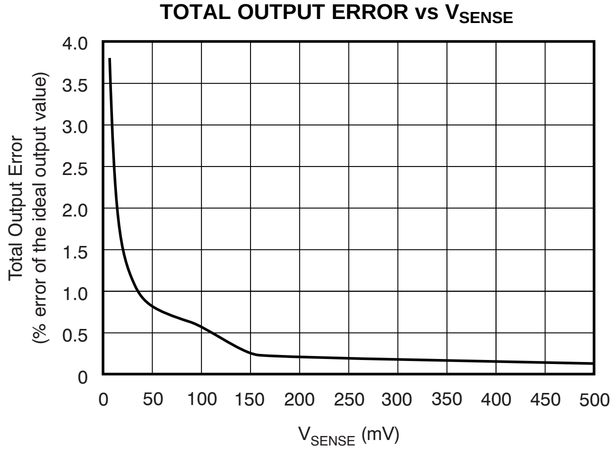


Figure 5.

OUTPUT ERROR vs COMMON-MODE VOLTAGE

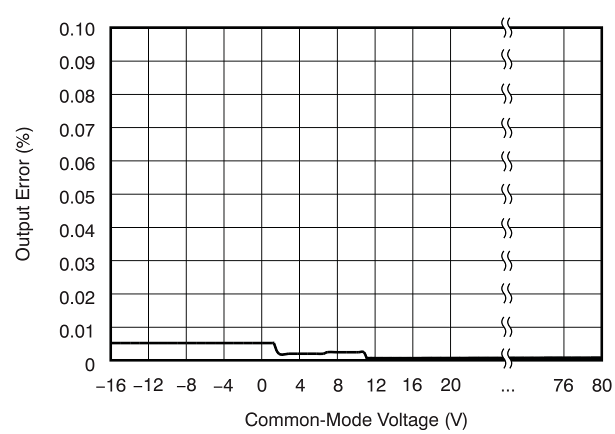


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +12V, V_{CM} = 12V, and V_{SENSE} = 100mV, unless otherwise noted.

POSITIVE OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

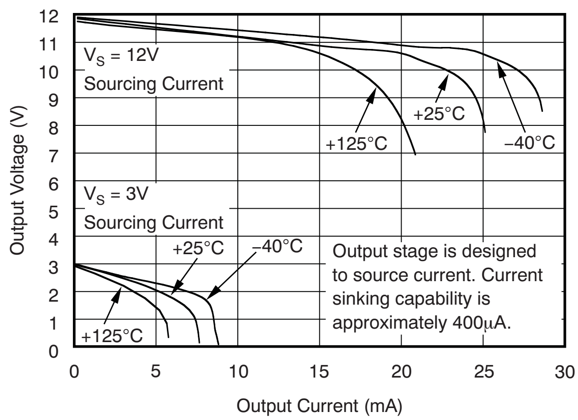


Figure 7.

QUIESCENT CURRENT vs OUTPUT VOLTAGE

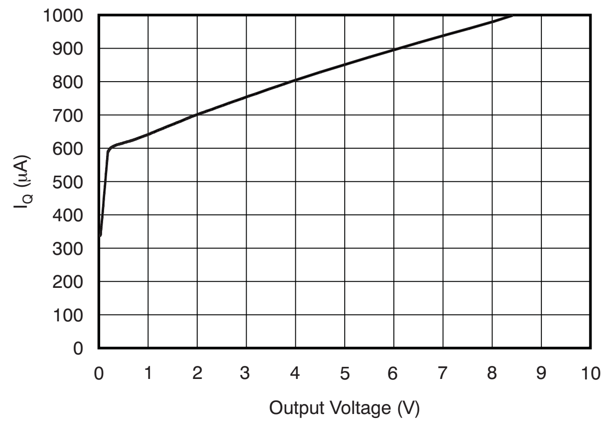


Figure 8.

QUIESCENT CURRENT vs COMMON-MODE VOLTAGE

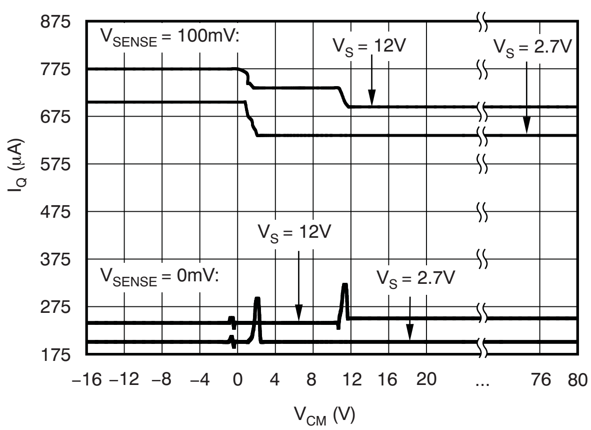


Figure 9.

OUTPUT SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

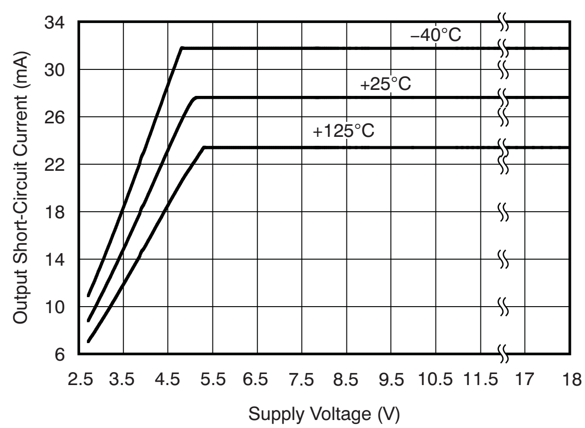


Figure 10.

PREOUT OUTPUT RESISTANCE PRODUCTION DISTRIBUTION

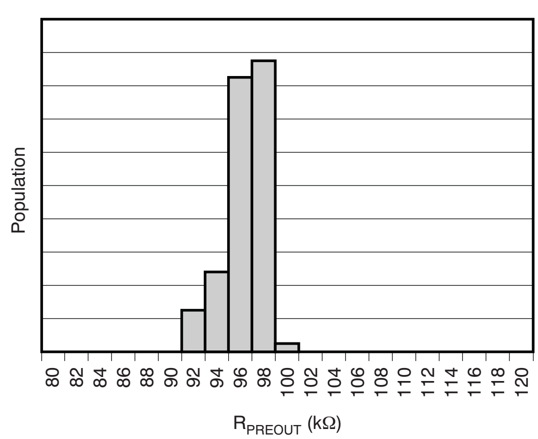


Figure 11.

BUFFER GAIN vs FREQUENCY

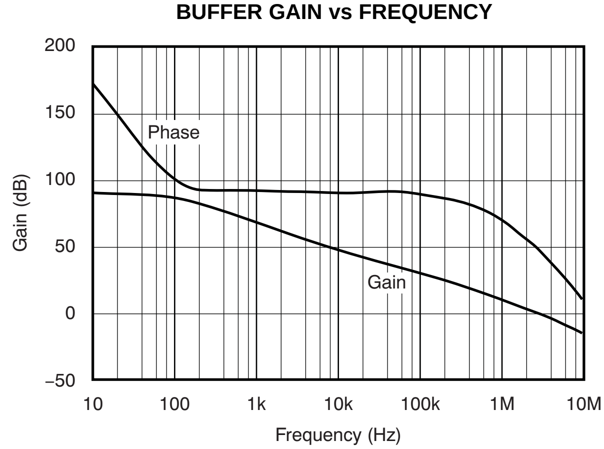


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +12V, V_{CM} = 12V, and V_{SENSE} = 100mV, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE 10mV TO 20mV INPUT

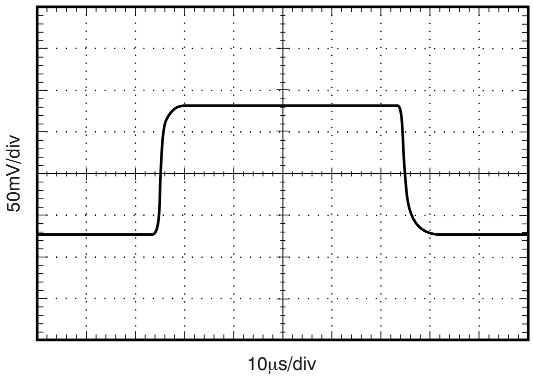


Figure 13.

LARGE-SIGNAL STEP RESPONSE 10mV TO 100mV INPUT

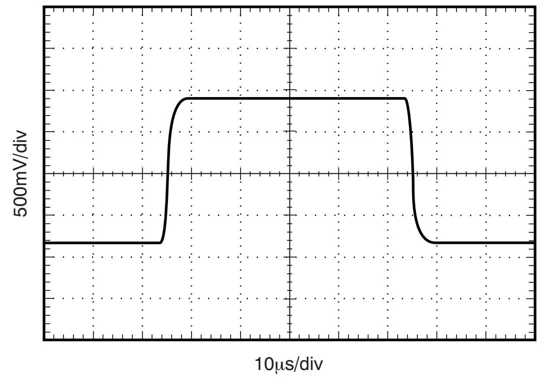


Figure 14.

APPLICATIONS INFORMATION

BASIC CONNECTION

Figure 15 shows the basic connection of the INA270 and INA271. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Minimum bypass capacitors of 0.01μF and 0.1μF in value should be placed close to the supply pins. Although not mandatory, an additional 10mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

POWER SUPPLY

The input circuitry of the INA270 and INA271 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5V, whereas the load power-supply voltage is up to +80V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

SELECTING R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50mV to 100mV. Maximum input voltage for accurate measurements is (V_S – 0.2)/Gain.

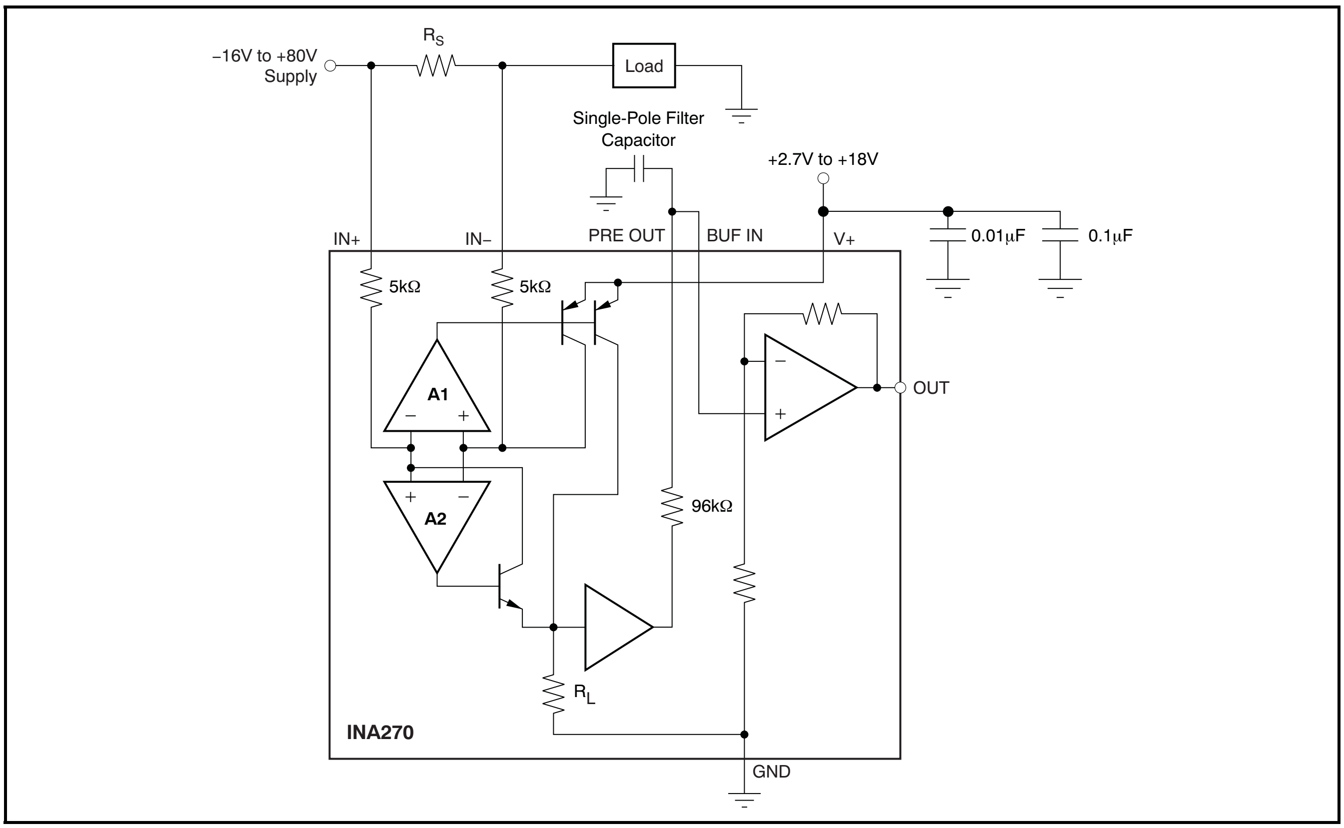


Figure 15. INA270 Basic Connections

TRANSIENT PROTECTION

The –16V to +80V common-mode range of the INA270 and INA271 is ideal for withstanding automotive fault conditions ranging from 12V battery reversal up to +80V transients, since no additional protective components are needed up to those levels. In the event that the INA270 and INA271 are exposed to transients on the inputs in excess of their ratings, external transient absorption with semiconductor transient absorbers (zeners or Transzorbs) will be necessary.

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA270 and INA271 to be exposed to transients greater than 80V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance).

Despite the use of internal zener-type ESD protection, the INA270 and INA271 are not suited to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30%, but are tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA270 and INA271 inputs with two equal resistors on each input).

OUTPUT VOLTAGE RANGE

The output of the INA270 and INA271 is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA270 and INA271 readily enable the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96kΩ output impedance at PRE OUT on pin 3, as shown in Figure 16a.

The INA270 and INA271 readily lend themselves to second-order Sallen-Key configurations, as shown in Figure 16b. When designing these configurations consider that the PRE OUT 96kΩ output impedance exhibits an initial variation of ±30% with the addition of a –2200ppm/°C temperature coefficient.

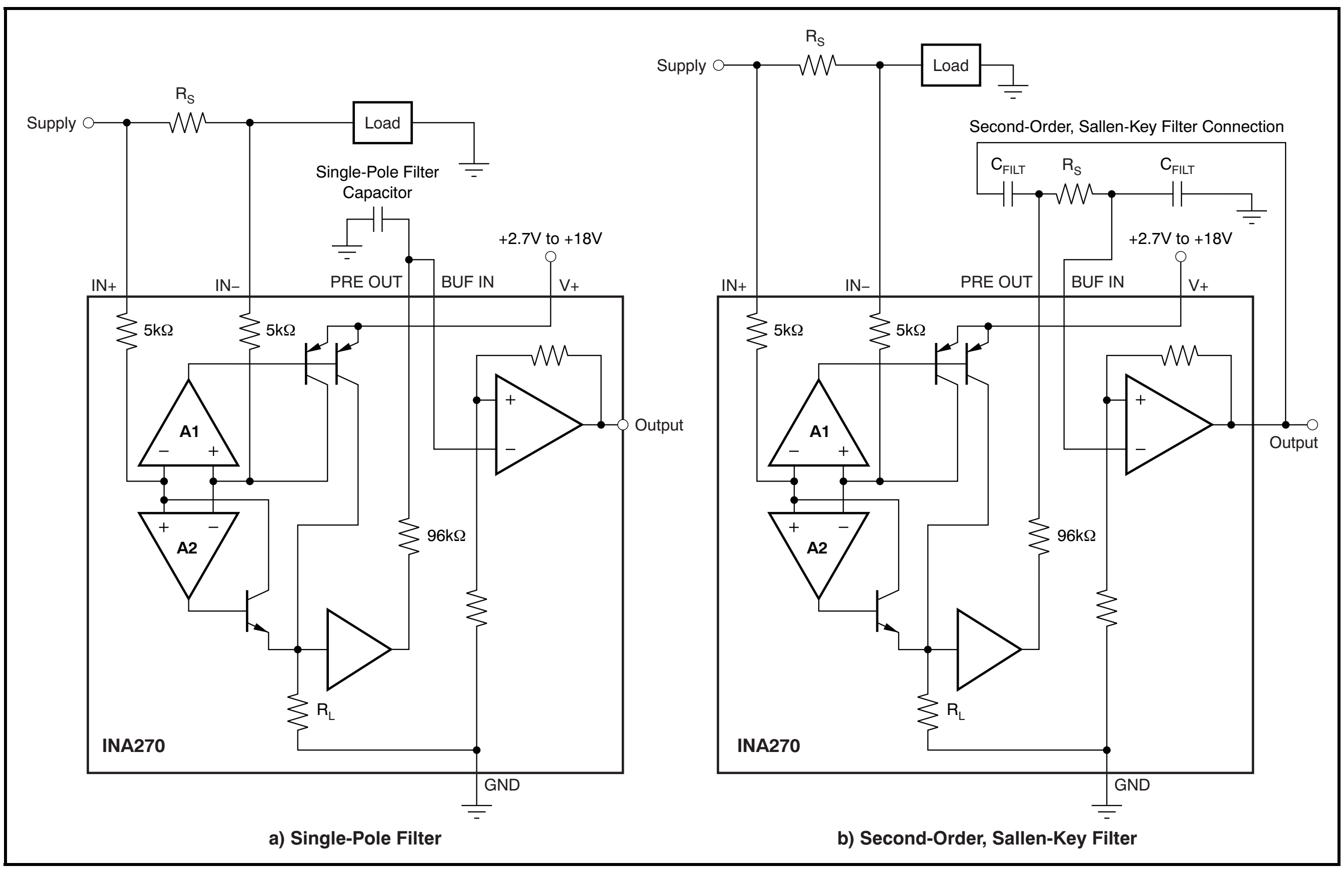


Figure 16. The INA270–INA271 can be easily connected for first- or second-order filtering. Remember to use the appropriate buffer gain (INA270 = 1.4, INA271 = 2) when designing Sallen-Key configurations.

ACCURACY VARIATIONS AS A RESULT OF V_{SENSE} AND COMMON-MODE VOLTAGE

The accuracy of the INA270 and INA271 current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} - V_{IN-}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as $(V_{IN+} + V_{IN-})/2$; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20mV$, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20mV$, $V_{CM} < V_S$
- Low V_{SENSE} Case 1:
  - $V_{SENSE} < 20mV$, $-16V \leq V_{CM} < 0$
- Low V_{SENSE} Case 2:
  - $V_{SENSE} < 20mV$, $0V \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3:
  - $V_{SENSE} < 20mV$, $V_S < V_{CM} \leq 80V$

Normal Case 1: $V_{SENSE} \geq 20mV$, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV} \quad (1)$$

where:

V_{OUT1} = Output Voltage with V_{SENSE} = 100mV
V_{OUT2} = Output Voltage with V_{SENSE} = 20mV

Then the offset voltage is measured at V_{SENSE} = 100mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{OS}RTI \text{ (Referred-To-Input)} = \left[\frac{V_{OUT1}}{G}\right] - 100mV \quad (2)$$

In the Typical Characteristics, the *Output Error vs Common-Mode Voltage* curve (Figure 6) shows the highest accuracy for the this region of operation. In this plot, V_S = 12V; for $V_{CM} \geq 12V$, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20mV$ output specifications in the Electrical Characteristics table.

Normal Case 2: $V_{SENSE} \geq 20mV$, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the *Output Error vs Common-Mode Voltage* curve (Figure 6). As noted, for this graph V_S = 12V; for V_{CM} < 12V, the Output Error increases as V_{CM} becomes less than 12V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16V.

Low V_{SENSE} Case 1: $V_{SENSE} < 20mV$, $-16V \leq V_{CM} < 0$; and Low V_{SENSE} Case 3: $V_{SENSE} < 20mV$, $V_S < V_{CM} \leq 80V$

Although the INA270 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA270 or INA271, it is important to know what the behavior of the devices will be in these regions.

As V_{SENSE} approaches 0mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 60mV for V_{SENSE} = 0mV. As V_{SENSE} approaches 20mV, V_{OUT} returns to the expected output value with accuracy as specified in the Electrical Characteristics. Figure 17 shows this effect using the INA271 (Gain = 20).

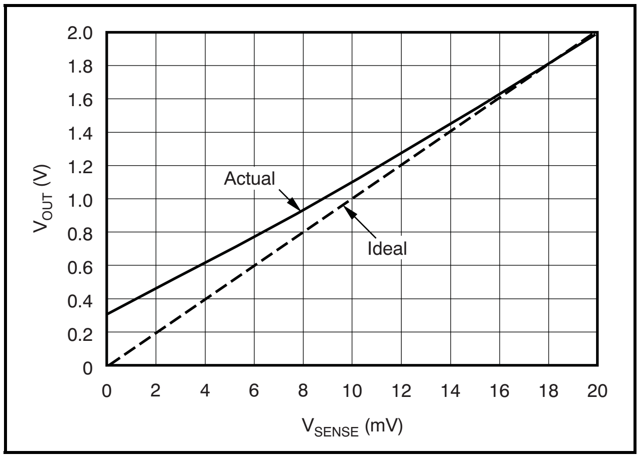


Figure 17. Example for Low V_{SENSE} Cases 1 and 3 (INA271, Gain = 20)

Low V_{SENSE} Case 2: V_{SENSE} < 20mV, 0V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA270 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0V. Within this region, as V_{SENSE} approaches 20mV, device operation is closer to that described by Normal Case 2. Figure 18 illustrates this behavior for the INA271. The V_{OUT} maximum peak for this case is determined by maintaining a constant V_S, setting V_{SENSE} = 0mV, and sweeping V_{CM} from 0V to V_S. The exact V_{CM} at which V_{OUT} peaks during this case varies from part to part. The maximum peak voltage for the INA270 is 0.28V; for the INA271, the maximum peak voltage is 0.4V.

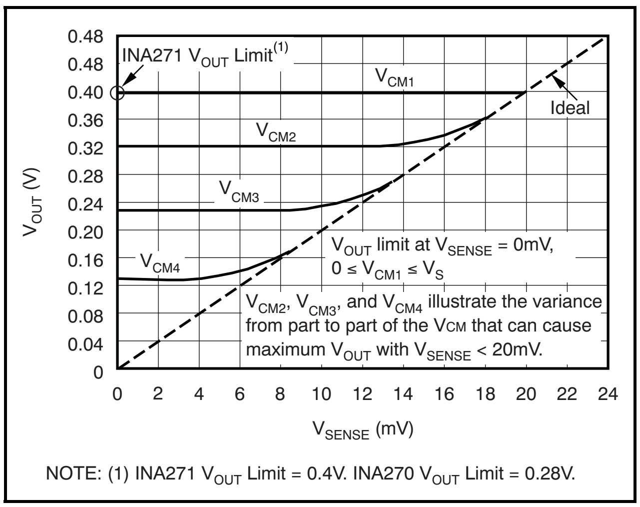


Figure 18. Example for Low V_{SENSE} Case 2 (INA271, Gain = 20)

SHUTDOWN

The INA270 and INA271 do not provide a shutdown pin; however, because they consume a quiescent current less than 1mA, they can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA270–INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with 0.1μF bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate should have a supply voltage of 3V or greater because the INA270 and INA271 require a minimum supply greater than 2.7V. In addition to eliminating quiescent current, this gate also turns off the 10μA bias current present at each of the inputs. Note that the IN+ and IN– inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is illustrated in Figure 19.

RFI/EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI/EMI sensitivity. PCB layout should locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA270 and INA271 versus the INA193–INA198 may provide different EMI performance.

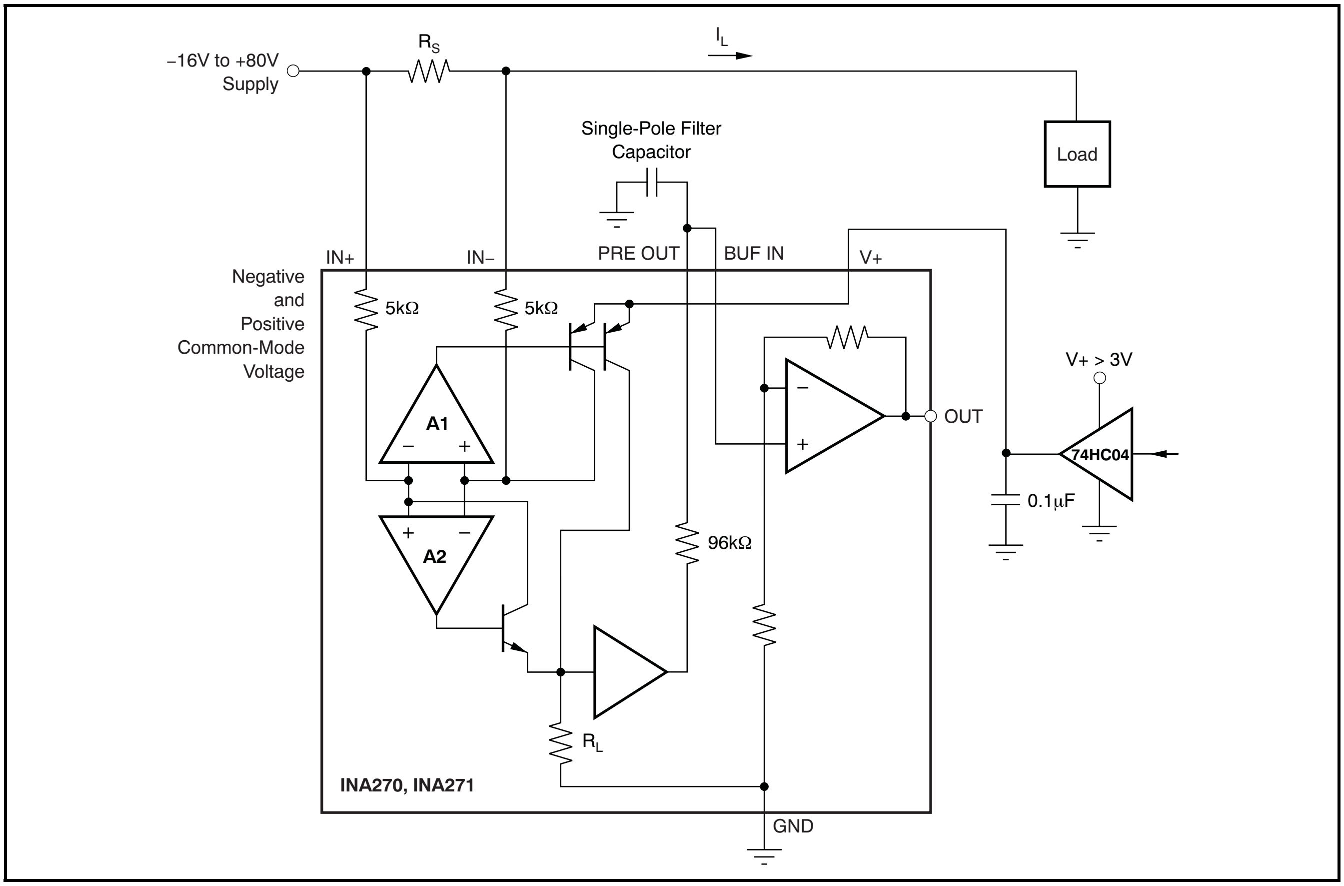


Figure 19. INA270–INA271 Example Shutdown Circuit

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
INA270AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA270AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA270AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA270AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA271AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA271AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA271AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA271AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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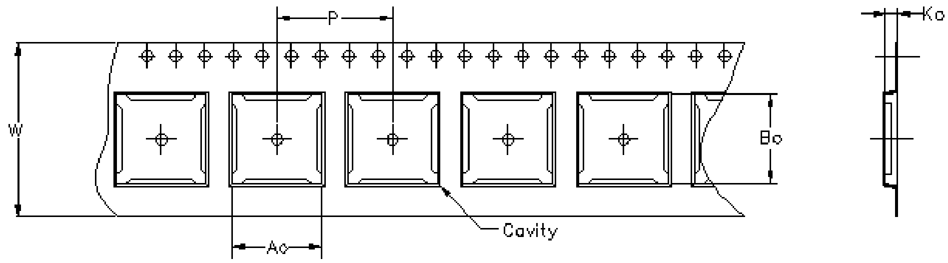
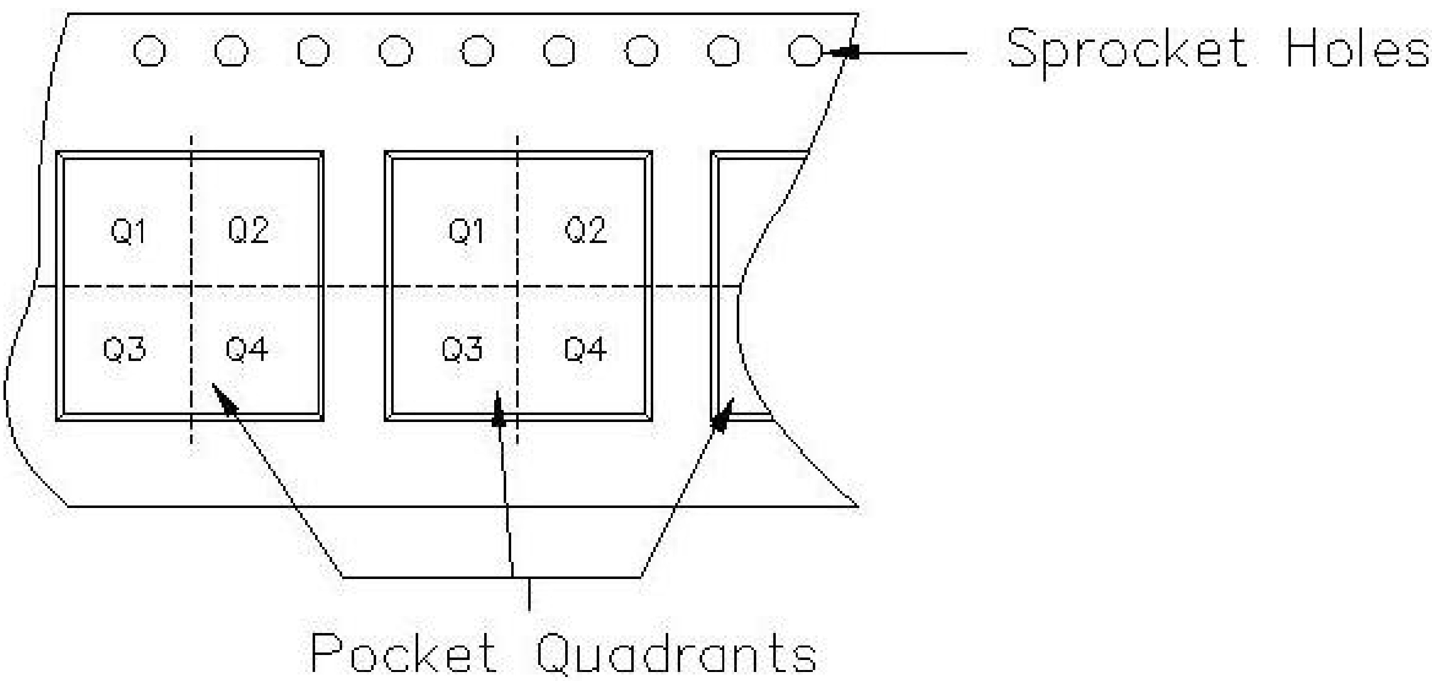
PACKAGE MATERIALS INFORMATION



Carrier tape design is defined largely by the component lentgh, width, and thickness.

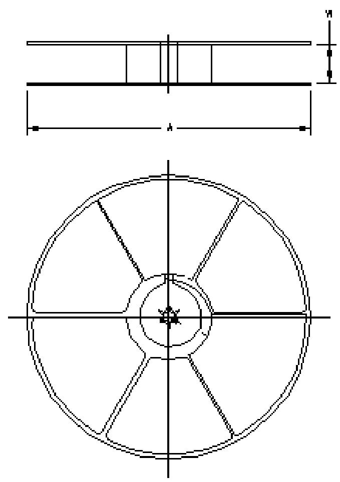
Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

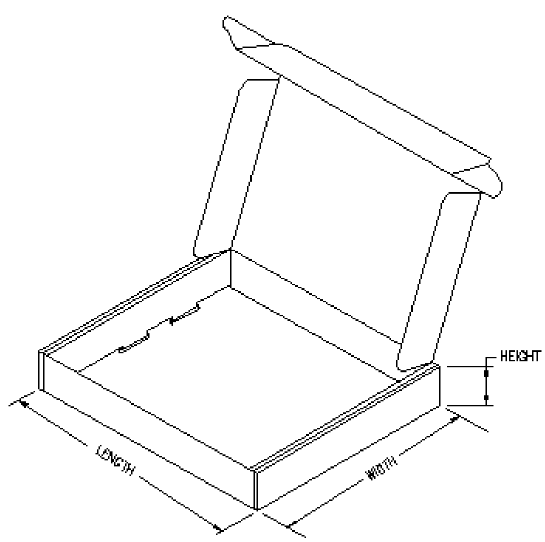
PACKAGE MATERIALS INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA270AIDR	D	8	TAI	330	12	6.4	5.2	2.1	8	12	NONE
INA271AIDR	D	8	TAI	330	12	6.4	5.2	2.1	8	12	NONE

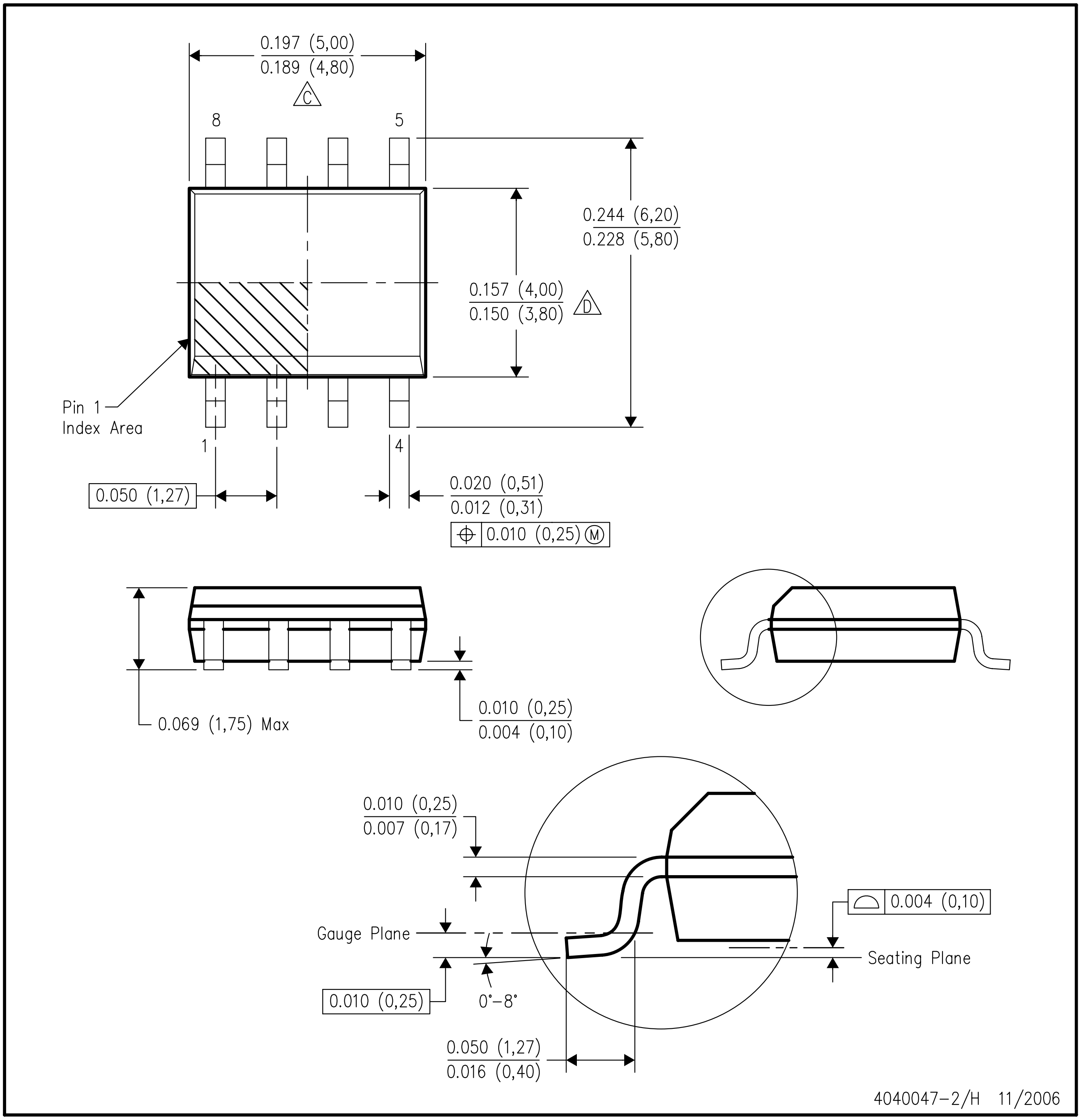


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
INA270AIDR	D	8	TAI	346.0	346.0	29.0
INA271AIDR	D	8	TAI	346.0	346.0	29.0



D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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